# P1838

This PAR is valid until 31-Dec-2018. It was extended on 05-Dec-2015.
**PAR Extension Request Date:** 23-Jul-2018
**Extension Request Submitter Email:** a.cron@ieee.org
**Number of Previous Extensions Requested:** 1
**1. Number of years that the extension is being requested:** 1
**2. Why an Extension is Required (include actions to complete):** Recently approved Standards (1687 and to a lesser extent 1149.1) led to some P1838 adjustments, requiring additional time to refine the standard. Ballot group is scheduled to be formed during the 4th quarter of 2018, and plans to submit to RevCom by July 2019.

**3.1. What date did you begin writing the first draft:** 15-Apr-2015
**3.2. How many people are actively working on the project:** 25
**3.3. How many times a year does the working group meet?**
**In person:** 1
**Via teleconference:** 30
**3.4. How many times a year is a draft circulated to the working group:** 6
**3.5. What percentage of the Draft is stable:** 95%
**3.6. How many significant work revisions has the Draft been through:** 4
**4. When will/did initial sponsor balloting begin:** 01-Jan-2019
**When do you expect to submit the proposed standard to RevCom:** 01-Aug-2019
**Has this document already been adopted by another source? (if so please identify):** No

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For an extension request, the information on the original PAR below is not open to modification.

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**Submitter Email:**
**Type of Project:** New IEEE Standard
**PAR Request Date:** 23-Nov-2010
**PAR Approval Date:** 02-Feb-2011
**PAR Expiration Date:** 31-Dec-2018
**Status:** PAR for a New IEEE Standard

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**1.1 Project Number:** P1838
**1.2 Type of Document:** Standard
**1.3 Life Cycle:** Full Use

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**2.1 Title:** Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits

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**3.1 Working Group:** 3D-Test Working Group (C/TT/3DT-WG)
**Contact Information for Working Group Chair**
**Name:** Adam Cron
**Email Address:**
**Phone:**
**Contact Information for Working Group Vice-Chair**
**Name:** Erik Jan Marinissen
**Email Address:**
**Phone:**

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**3.2 Sponsoring Society and Committee:** IEEE Computer Society/Test Technology (C/TT)
**Contact Information for Sponsor Chair**
**Name:** Adam Cron
**Email Address:**
**Phone:**
**Contact Information for Standards Representative**
None

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**4.1 Type of Ballot:** Individual
**4.2 Expected Date of submission of draft to the IEEE-SA for Initial Sponsor Ballot:** 09/2012
**4.3 Projected Completion Date for Submittal to RevCom**

**Note: Usual minimum time between initial sponsor ballot and submission to Revcom is 6 months.:** 02/2013

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**5.1 Approximate number of people expected to be actively involved in the development of this project:** 25
**5.2 Scope:** The proposed standard is a 'die-centric' standard; it applies to a die that is intended to be part of a multi-die stack. The proposed standard defines die-level features, that, when compliant dies are brought together in a stack, comprise a stack-level architecture that enables transportation of control and data signals for the test of (1) intra-die circuitry and (2) inter-die interconnects in both (a) pre-stacking and (b) post-stacking situations, the latter for both partial and complete stacks in both pre-packaging, post-packaging, and board-level situations. The primary focus of inter-die interconnect technology addressed by this standard is Through-Silicon Vias (TSVs); however, this does not preclude its use with other interconnect technologies such as wire-bonding.
The standard will consist of two related items.
1. 3D Test Wrapper Hardware
On-die hardware features that enable transportation of test (control and data) signals in the following configurations.
* Pre-stacking: From on-die I/Os to die-internal DfT/test features, and vice versa. These on-die I/Os might be functional I/Os; however, if they are not present or not accessible, it might be necessary to add additional test I/Os.
* Post-stacking
o 'Turn' mode: From on-die I/Os to die-internal DfT/test features, and vice versa. These on-die I/Os might be external I/Os on the die itself, and/or inter-die interconnections coming from (or going to) an adjacent die in the stack.
o 'Elevator' mode: From on-die I/Os, through THIS DIE, to the inter-die interconnections to an adjacent die, and vice versa. These on-die I/Os might be external I/Os on the die itself and/or inter-die interconnections coming from (or going to) another adjacent die in the stack.
2. Description + Description Language
A description of the Test Wrapper features in a standardized human- and computer-readable language. This description should allow the usage of the die within a multi-die stack for test and test access purposes.
The proposed standard does not mandate specific defect or fault models, test generation methods, nor die-internal design-for-test, but instead focuses on generic test access to and between dies in a multi-die stack. The proposed standard is based on and works with digital scan-based test access and should leverage existing test access ports (such as based on IEEE Std 1149.x) and on-chip design-for-test (such as IEEE Std 1500) and design-for-debug (IEEE P1687) infrastructure wherever applicable and appropriate.
The proposed standard is 'die-centric', and hence does not aim at 'stack/product-centric' challenges, solutions, and standards, such as the inclusion of Boundary Scan features for board-level interconnect testing. However, the proposed standard should not prohibit the application of such solutions.

**5.3 Is the completion of this standard dependent upon the completion of another standard:** No
**5.4 Purpose:** For 3D-SICs, three parties are involved: Die Maker(s), Stack Maker(s), and Stack User(s). All circuit features of the stack are included in the individual die designs. Design and integration of test access features needs to be done by the Die Maker(s), not only to serve their own (pre-stacking) test objectives, but also to serve test objectives of Stack Maker and Stack User. After stacking, test (control and data) signals need to be able to travel from the stack's external I/Os up and down through the stack. Hence, the test access features in the various dies of the stack need to function in a concerted and interoperable fashion.
Different dies might have their own technologies, design set-up, and test and design-for-test approaches; the standard should not modify those. The standard defines test access features for a die that enable the transportation of test stimuli and responses both for testing THIS DIE and its inter-die connections, as well as for testing OTHER DIES in the stack and their inter-die connections.

**5.5 Need for the Project:** The semiconductor industry is preparing itself for three-dimensional stacked integrated circuits (3D-SICs), especially fueled by the advent of technologies based on Through-Silicon Vias (TSVs). TSVs are conducting nails which extend out of the backside of a thinned-down die and enable the vertical interconnection to another die. TSVs enable high-density, low-capacitance interconnects compared to traditional wire-bonds, and hence allow for many more interconnections between stacked dies, while operating at higher speeds and consuming less power. TSV-based 3D technologies enable the creation of a new generation of 'super chips' by opening up new architectural opportunities. 3D-SICs combine a smaller form factor and lower overall manufacturing cost with many other compelling benefits, and hence their technology is quickly gaining ground.
Like all micro-electronic products, 3D-SICs need to be tested for manufacturing defects, to filter out bad products and only deliver good products to the customer. A test access architecture transports test (data and control) signals for die and interconnect tests. In a post-bond stack situation, the external I/Os will typically be located on a single die, e.g. the bottom die, and hence the transportation of test stimuli and responses for a middle or top die has to propagate through all dies below it. This requires that the test access features integrated in each individual die are inter-operable and compatible with each other. This is even more true for an interconnect test,which by definition requires the two dies on either side of the interconnects to operate in a concerted way.
This standard will bring the following benefits to its various users.
* IP Providers creating content (e.g. hard cores) will know what to supply in terms of test access architecture and documentation in order to satisfy a diverse set of customers.
* 3D-SIC Die Makers will know what to supply in terms of test access architecture and documentation in order to satisfy a diverse set of customers.
* 3D-SIC Stack Makers who stack compliant dies will benefit from guarantees with respect to testability access of their stacks; it allows them a

certain freedom in 'second sourcing' and mixing-and-matching of compliant dies.
* Stack Users that utilize 3D-SIC stacks with compliant dies will benefit from guarantees with respect to testability access of their products.
* Vendors of Electronic Design Automation (EDA) tools will be able to provide tools that generate and utilize this test access architecture and the necessary documentation.

**5.6 Stakeholders for the Standard:** The semiconductor industry at large, including Integrated Device Manufacturers (IDMs), foundries, fab-light and fab-less semiconductor companies, design houses, Intellectual Property (IP) core providers, vendors of Electronic Design Automation (EDA) tools, OutSourced Assembly & Test (OSAT) houses, companies in the IC test industry, board and system manufacturers.

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**Intellectual Property**
**6.1.a. Is the Sponsor aware of any copyright permissions needed for this project?:** No
**6.1.b. Is the Sponsor aware of possible registration activity related to this project?:** No

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**7.1 Are there other standards or projects with a similar scope?:** No
**7.2 Joint Development**
**Is it the intent to develop this document jointly with another organization?:** No

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**8.1 Additional Explanatory Notes:** None.