Status Report April 2010

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Leuven, Belgium

SSG on 3D-Test

- **Charter**
  - Inventorize need for and timeliness of standards in 3D test and DfT
  - If appropriate, formulate Project Authorization Requests (PARs) for starting up an IEEE Standard Development Working Group (SDWG)
- **Organization & Participation**
  - 52+2 participants from companies/institutes around the globe
  - Chair: Erik Jan Marinissen (IMEC)
- **Activities to date**
  - Active per January 2010
  - Public web site: http://grouper.ieee.org/groups/3Dtest/
  - Private web site and e-mail reflector for internal communication
  - Weekly WebEx conference calls (provided by Cisco Systems)

Members

Saman Adham
Neetu Agrawal
Lorena Anghel
Patrick Y Au
Paolo Bernardi
Sandeep Bhatia
Craig Bullock
Krishnendu Chakrabarty
Ji-Jan Chen
Vivek Chickermane
CJ Clark
Eric Cormack
Adam Cron
Al Crouch
Shinichi Domae
Ted Eaton
Bill Eklow
Klaus Förster
Jan Olaf Gaudestad
Michelangelo Grosso
Said Hamdioui
Klaus Helmreich
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Gert Jervan
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Jochen Rivoir
Volker Schöber
Eric Strid
Thomas Thaerigen
Jouke Verbree
Ioannis Voyiatzis
Michael Wahl
Min-Jer Wang
Lee Whetsel
Yervant Zorian
+ Frans de Jong
+ Frank Pöhl

Participating Companies


Agilent Technologies

AMD

ANALOG DEVICES
ARM

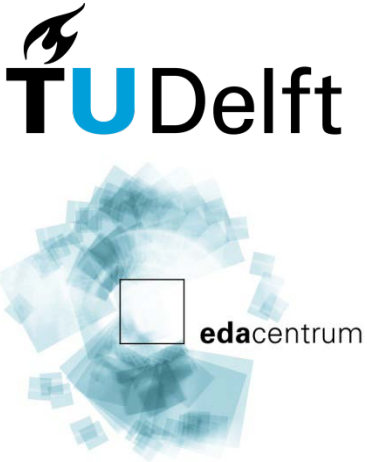

Panasonic



SYNOPSYS®



Institutes, Universities, and Consultants



ITRI
Industrial Technology
Research Institute

TTSC Standardization Study Group on 3D Test

Identified Standardization Needs

During the SSG discussions,
the following standardization needs were identified:

- **Die and Stack Test**
  1. DfT test access architecture
  2. Wafer probe interface

- **Access for Board-Level Users**
  3. Board-level interconnect test
  4. Access to embedded instruments

- **Test Data Formats**
  5. Wafer map and device tracking
  6. Standard Test Data Format (STDF)

1. DfT Architecture for Manufacturing Test

- **Motivation**
  - Die makers need to provide DfT, also for stack- and board makers
  - Interoperability between various dies required
- **Requirements**
  - Support (1) pre-bond die test and (2) post-bond stack test
  - Support modular test approach
  - Generic and scalable
  - Low cost
    - Few extra product pins
    - Leverage of existing DfT and DfT standards
- **Status**
  - One proposal by IMEC,
    based 3D extension of (2D) IEEE Std 1500

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2. Wafer Probe Interface

Wafer Probing on TSVs / Micro-Bumps is Challenging

- Small pitch; small probe area
- Probe damage might impair downstream bonding

Wafer Probe Industry Would be Helped by Standardization

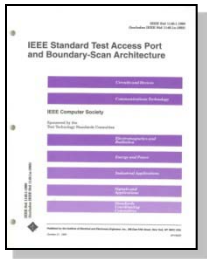
- Standard pad pitches
- Standard pad footprints
- Standard pad materials and designs

Benefits also for design, assembly, second sourcing, …

Status

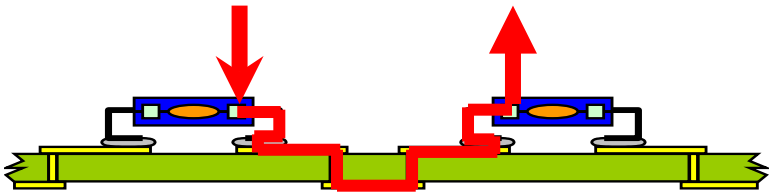
- Idea only, no proposals yet

3. Board-Level Interconnect Test



Board-Level Interconnect Test

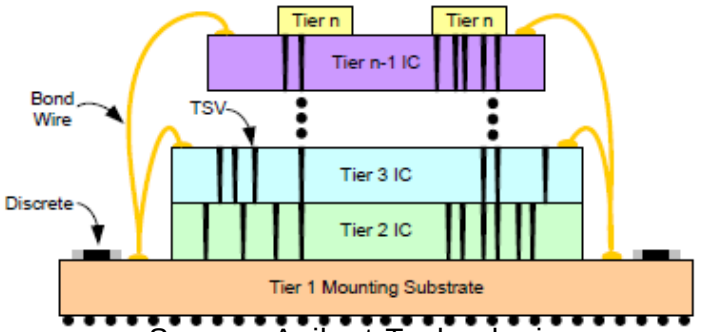
- Via on-chip DfT, a.k.a. “JTAG”:
  IEEE Std 1149.1 Test Access Port (TAP)



Source: Philips Electronics

Worry: Stacks with TSVs + Wire-Bonds

- External I/Os distributed over multiple dies
- JTAG distributed over multiple dies
- Board-level test needs to know this
  in a standardized view

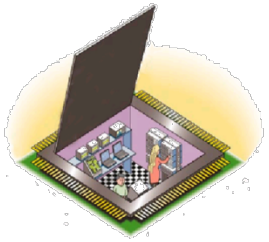


Source: Agilent Technologies

Status

- Idea only, no proposals yet
- Discussion in SSG how likely this would happen in products

4. Access to Embedded Instruments



For Today's 2D Chips and Boards

- JTAG TAP reused for alternative purposes
  - BIST, diagnosis, silicon debug, FPGA progr., SW debug, etc.
  - Access to *'embedded instruments'*: monitors, sensors, etc. (IEEE P1687, a.k.a. "Internal-JTAG")

Extension to 3D-SICs

- Purpose: enable this type of usage also for 3D-SICs
- Stack might contain multiple TAP Controllers
- Status: three proposals so far
  - Mix of Existing Standards: 1149.7 (stack), 1149.1/6 (die), 1500 (core) (Asset-Intertech)
  - TAP Linking Module (Texas Instruments)
  - iMajik (Intellitech)

5+6. Test Data Formats

- **Wafer Maps**
  - Pass/fail information per die
- **Inkless Assembly and Single-Device Tracking**
  - Die to wafer location and wafer processing
  - Die to assembly, packaging, and test processes
  - All dies in multi-chip package
- **Standard Test Data Format (STDF)**
  - File format for (diagnostic) IC test data collection
  - Currently at STDF-v4 (2007), developing JTDF

Standards

SEMI G81/G85
- obsolete

SEMI E142
- Already handles 3D?

SEMI STDF-v4
- Requires extension to 3D