Status Report May 2010

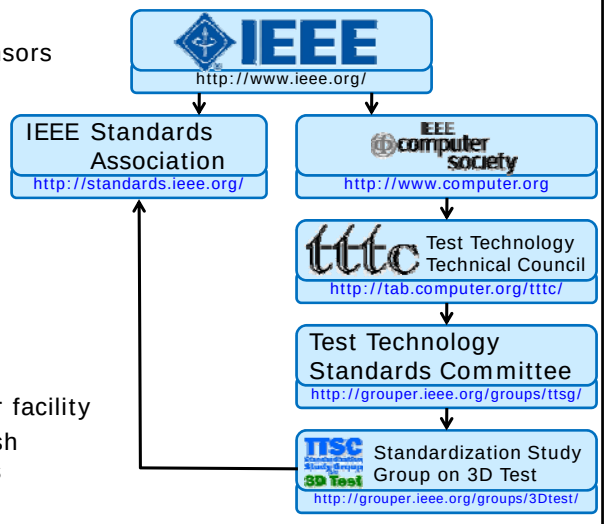
Erik Jan Marinissen
IMEC
Leuven, Belgium

SSG on 3D-Test

- **Charter**
  - Inventorize need for and timeliness of standards in 3D test and DfT
  - If appropriate, formulate Project Authorization Requests (PARs) for starting up an IEEE Standard Development Working Group (SDWG)
- **Organization & Participation**
  - 54+2 participants from companies/institutes around the globe
  - Chair: Erik Jan Marinissen (IMEC)
- **Activities to date**
  - Active per January 2010
  - Public web site: http://grouper.ieee.org/groups/3Dtest/
  - Private web site and e-mail reflector for internal communication
  - Weekly WebEx conference calls (provided by Cisco Systems)

Organization Chart + URLs

- IEEE sponsors
  Computer Society sponsors
  TTTC sponsors
  TTSC sponsors
  SSG on 3D-Test
- SSG membership is open to professionals
- IEEE-SA
  - Provides facilities
    - Web hosting
    - E-mail reflector facility
  - Will own and publish resulting standards



SSG Members

Saman Adham
Neetu Agrawal
Lorena Anghel
Patrick Y Au
Paolo Bernardi
Sandeep Bhatia
Craig Bullock
Krishnendu Chakrabarty
Ji-Jan Chen
Vivek Chickermane
CJ Clark
Eric Cormack
Adam Cron
Al Crouch
Shinichi Domae
Ted Eaton
Heiko Ehrenberg
Bill Eklow
Klaus Förster
Jan Olaf Gaudestad
Michelangelo Grosso
Said Hamdioui
Klaus Helmreich
Michael Higgins
Gert Jervan
Hongshin Jun
Rohit Kapur
Ajay Khoche
Santosh J Kulkarni
Michael Laisne
Philippe Lebourg
Stephane Lecomte
Hans Manhaeve
Erik Jan Marinissen
Teresa McLaurin
Brandon Noia
Jay Orbon
Ken Parker
John Potter
Bill Price
Herb Reiter
Mike Ricchetti
Andrew Richardson
Daniel Rishavy
Jochen Rivoir
Volker Schöber
Eric Strid
Thomas Thaerigen
Jouke Verbree
Ioannis Voyiatzis
Michael Wahl
Min-Jer Wang
Lee Whetsel
Yervant Zorian

+ Frans de Jong
+ Frank Pöhl

SSG Participating Companies

Agilent Technologies, AMD, ANALOG DEVICES, ARM, ASSET, cadence, CASCADE MICROTECH, CISCO, GOPEL electronics, IBM, infineon, Intellitech, NXP, Oasys The Chip Synthesis Company, Panasonic, NECCERA, Q-STAR The Current Test Company, QUALCOMM, ST ERICSSON, SYNOPSYS, TEL, TEXAS INSTRUMENTS, tsmc, VERIGY, VIRAGE LOGIC Accelerating Silicon Success

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SSG Institutes, Universities, Consultants

TU Delft, DFT Solutions Ltd, eda2asic, edacentrum, Friedrich-Alexander-Universität Erlangen-Nürnberg, GSA, imec, IMMS, ITRI Industrial Technology Research Institute, LANCASTER UNIVERSITY, UNIVERSITÄT SIEGEN, TEI, iima CNRS - Grenoble INP - UJF, TTÜ 1918, T2C2

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Identified Standardization Needs

During the SSG discussions,
the following standardization needs were identified:

- **Die and Stack Test**
  1. DfT test access architecture
  2. Wafer probe interface
- **Access for Board-Level Users**
  3. Board-level interconnect test
  4. Access to embedded instruments
- **Test Data Formats**
  5. Wafer map and device tracking
  6. Standard Test Data Format (STDF)

1. DfT Architecture for Manufacturing Test

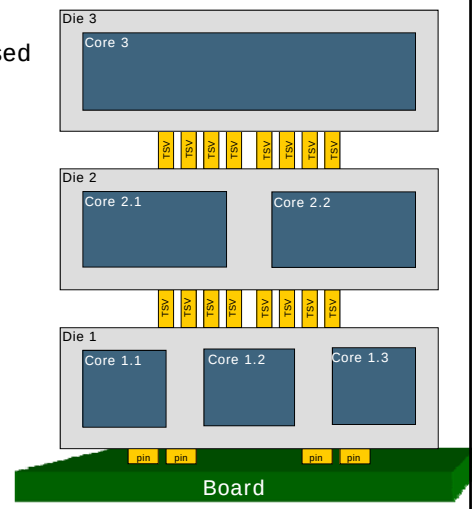
- **Motivation**
  - Die makers need to provide DfT, also for stack- and board makers
  - Interoperability between various dies required
- **Requirements**
  - Support (1) pre-bond die test and (2) post-bond stack test
  - Support modular test approach
  - Generic and scalable
  - Low cost
    - Few extra product pins
    - Leverage of existing DfT and DfT standards
- **Status**
  - Two proposals by IMEC, based 3D extension of IEEE Std 1500 and IEEE Std 1149.1

1. DfT Architecture for Manufacturing Test

IMEC Proposals

Functional Design

- ≥2 stacked dies, possibly core-based
- Inter-connect: TSVs
- Extra-connect: pins



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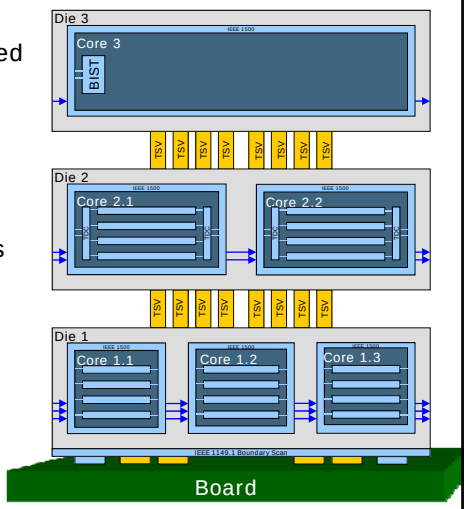
Existing Design-for-Test

- Core: internal scan, TDC, LBIST, MBIST; IEEE 1500 wrappers, TAMs
- Product: IEEE 1149.1



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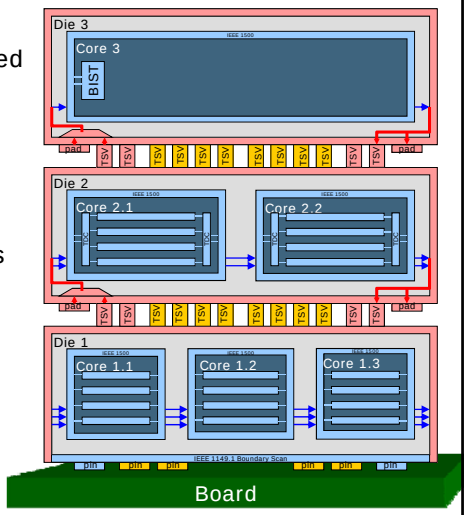
3D DfT Architecture

Test wrapper per die

- Based on IEEE Std 1500/1149.1
- Two entry/exit points per die:
  1. Pre-bond : extra probe pads
  2. Post-bond: extra TSVs

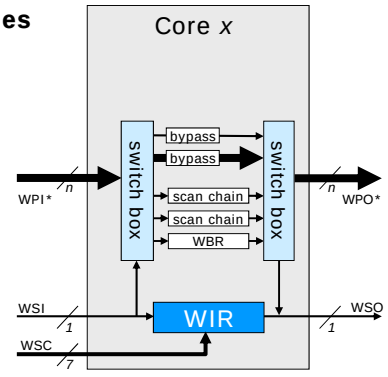


1. DfT Architecture for Manufacturing Test

IMEC Proposal: 1500-Based Die Wrapper

- **Conventional (2D) IEEE 1500 Features**
  - WSC Control: `WRCK`, `WRSTN`, `SelectWIR`, `ShiftWR`, `CaptureWR`, `UpdateWR`, `TransferDR*`
  - Serial interface: `WSI-WSO`
  - Parallel interface: `WPI*-WPO*`
  - Wrapper Instruction Register (WIR)
  - Wrapper Boundary Register (WBR)
  - Serial and parallel* Bypass

* = optional

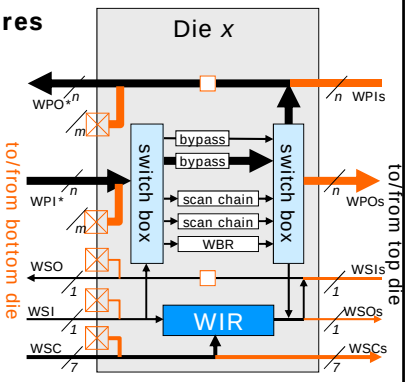


Note: Figure abstracts from functional circuitry and only shows DfT features

1. DfT Architecture for Manufacturing Test

IMEC Proposal: 1500-Based Die Wrapper

- **Conventional (2D) IEEE 1500 Features**
- **New 3D Features**
  1. *TestTurns*
     - Serial and parallel interface towards bottom die
     - Flip-flops for clean timing
  2. *Probe pads on non-bottom dies*
     - Mandatory on WSC, WSI-WSO
     - Scalable on WPI-WPO
  3. *TestElevators* to higher-up die(s)
     - Mirrored standard 1500 interface: WSCs, WSIs-WSOs, WPIs-WPOs
  4. *Hierarchical* WIR chain (not shown here)



[Marinissen et al. – VTS'10]

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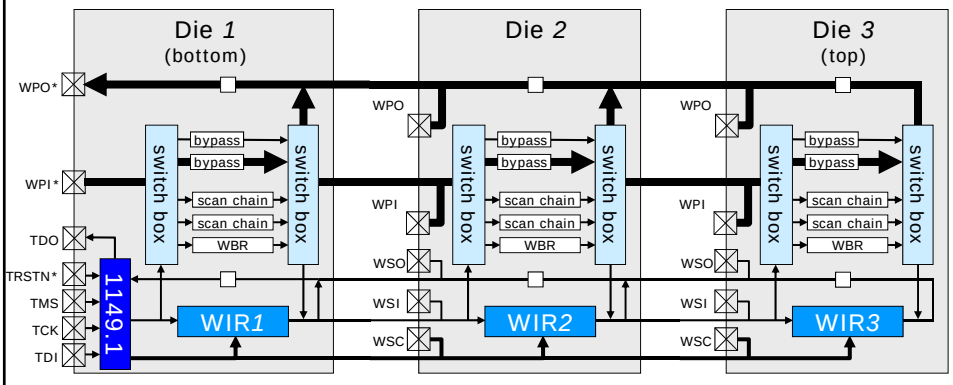
1. DfT Architecture for Manufacturing Test

IMEC Proposal: 1500-Based Die Wrapper

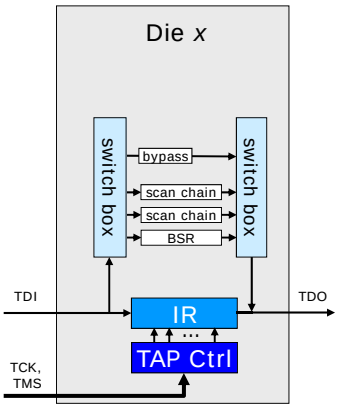


- **Bottom Die**: no extra product pins
  - Serial interface multiplexed onto IEEE 1149.1 interface
  - Parallel interface multiplexed onto existing functional pins
- **Top Die**: no TestElevators (as no other die above)

1. DfT Architecture for Manufacturing Test

IMEC Proposal: 1149.1-Based Die Wrapper

- **Conventional IEEE 1149.1 Features**
  - TAP: TCK, TMS, TDI, TDO
  - Regular 16-state TAP Controller
  - Instruction Register
  - Bypass



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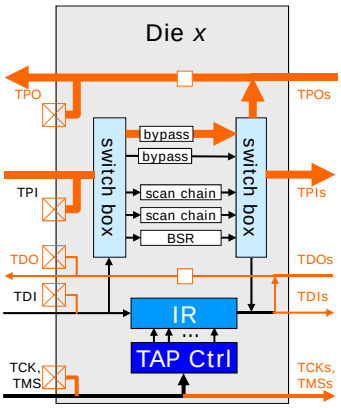
1. DfT Architecture for Manufacturing Test

IMEC Proposal: 1149.1-Based Die Wrapper

- **Conventional IEEE 1149.1 Features**
- **New 3D Features**
  0. *Scalable parallel test data port*
     - For higher-bandwidth access
  1. *TestTurns*
     - Interface towards bottom die
     - Flip-flops for clean timing
  2. *Probe pads on non-bottom dies*
     - Mandatory on TCK, TMS, TDI-TDO
     - Scalable on TPI-TPO
  3. *TestElevators* to higher-up die(s)
     - Mirrored bottom interface: TCKs, TMSs, TDIs-TDOs, TPIs-TPOs
  4. *Hierarchical* test control IRs+WIRs for free

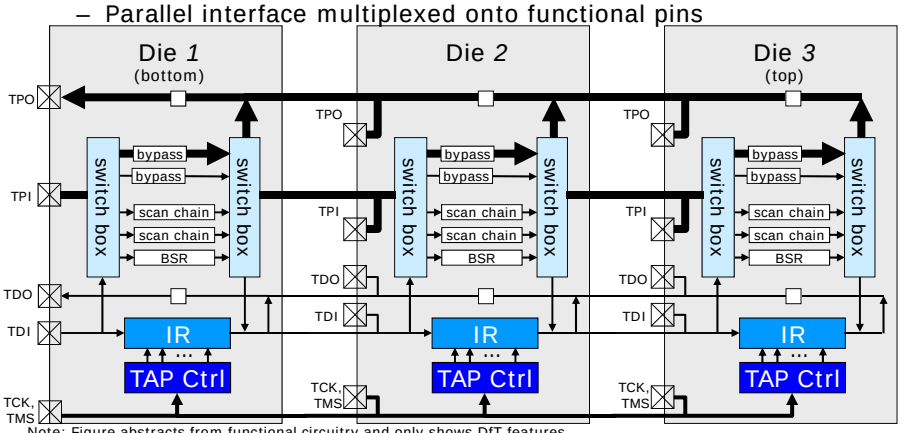


Note: Figure abstracts from functional circuitry and only shows DfT features

1. DfT Architecture for Manufacturing Test

IMEC Proposal: 1149.1-Based Die Wrapper

- No extra product pins
  - IEEE 1149.1 interface on bottom die present anyway
  - Parallel interface multiplexed onto functional pins



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1. DfT Architecture for Manufacturing Test

1149.3D Instructions = 1149.1 User Instr.

Field 1	Field 2	Field 3	Field 4
Serial Parallel	Prebond Postbond	Bypass Intest Extest	Turn Elevator

Pre-Bond Instructions

- *SerialPrebondBypassTurn*
- *SerialPrebondIntestTurn*
- *ParallelPrebondBypassTurn*
- *ParallelPrebondIntestTurn*

Post-Bond Instructions

- *SerialPostbondBypassTurn**
- *SerialPostbondIntestTurn* **= INTEST**
- *SerialPostbondExtestTurn* **= EXTEST**
- *SerialPostbondBypassElevator*
- *SerialPostbondIntestElevator*
- *SerialPostbondExtestElevator*
- *ParallelPostbondBypassTurn*
- *ParallelPostbondIntestTurn*
- *ParallelPostbondExtestTurn*
- *ParallelPostbondBypassElevator*
- *ParallelPostbondIntestElevator*
- *ParallelPostbondExtestElevator*

* = functional start-up mode

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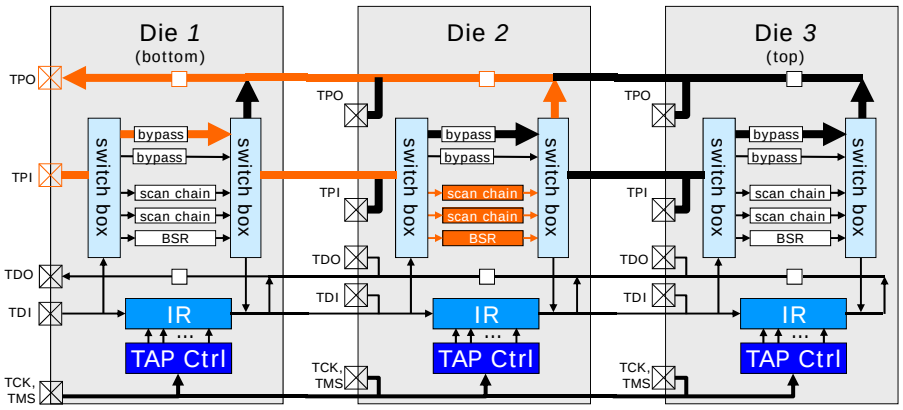
1. DfT Architecture for Manufacturing Test

Example 1: Testing Die 2



Die 1:
ParallelPostbond
BypassElevator

Die 2:
ParallelPostbond
IntestTurn

Die 3:
ParallelPostbond
BypassTurn

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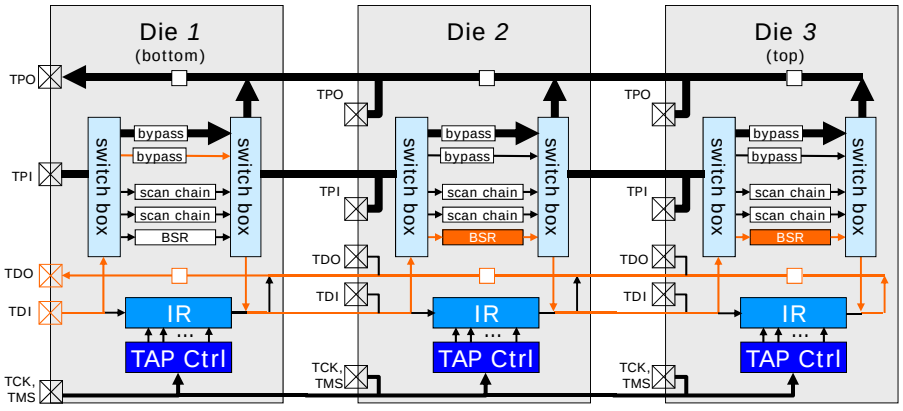
1. DfT Architecture for Manufacturing Test

Example 2: Test of Interconnect Die 2-3



Die 1:
SerialPostbond
BypassElevator

Die 2:
SerialPostbond
ExtestElevator

Die 3:
SerialPostbond
ExtestTurn

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2. Wafer Probe Interface

Wafer Probing on TSVs / Micro-Bumps is Challenging
- Small pitch; small probe area
- Probe damage might impair downstream bonding

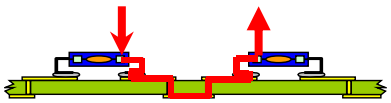
Wafer Probe Industry Would be Helped by Standardization
- Standard pad pitches
- Standard pad footprints
- Standard pad materials and designs

Benefits also for design, assembly, second sourcing, ...

Status
- Idea only, no proposals yet
- Planning to start dedicated sub-team on this topic

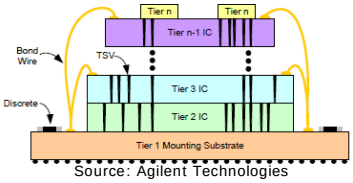
3. Board-Level Interconnect Test

Board-Level Interconnect Test
- Via on-chip DfT, a.k.a. "JTAG":
  IEEE Std 1149.1 Test Access Port (TAP)



Source: Philips Electronics

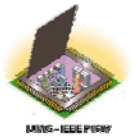
External I/Os distributed over Multiple Dies
- For example due to
  - Stacks with TSVs + wire-bonds
  - Pass-through-only TSVs
- JTAG distributed over multiple dies
- Board-level test needs to know this in a standardized view



Source: Agilent Technologies

Status
- Idea only, no proposals yet
- Discussion in SSG how likely this would happen in products

4. Access to Embedded Instruments



For Today's 2D Chips and Boards

- JTAG TAP reused for alternative purposes
  - BIST, diagnosis, silicon debug, FPGA progr., SW debug, etc.
  - Access to *'embedded instruments'*: monitors, sensors, etc. (IEEE P1687, a.k.a. "Internal-JTAG")

Extension to 3D-SICs

- Purpose: enable this type of usage also for 3D-SICs
- Stack might contain multiple TAP Controllers
- Status: three proposals so far
  - Mix of Existing Standards: 1149.7 (stack), 1149.1/6 (die), 1500 (core) (Asset-Intertech)
  - TAP Linking Module (Texas Instruments)
  - iMajik (Intellitech)

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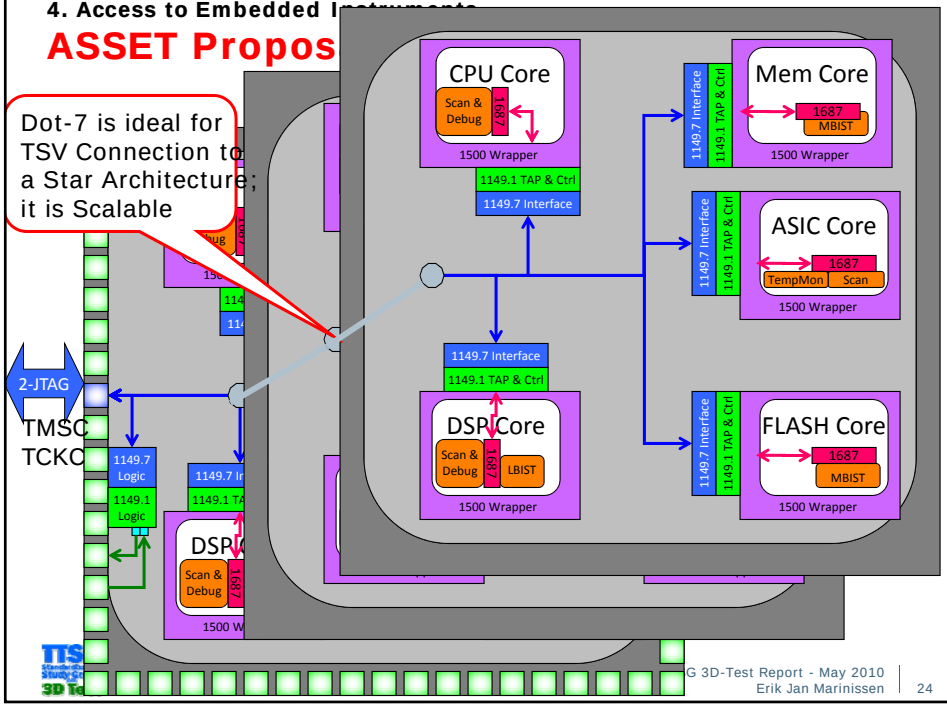
4. Access to Embedded I

ASSET Propos



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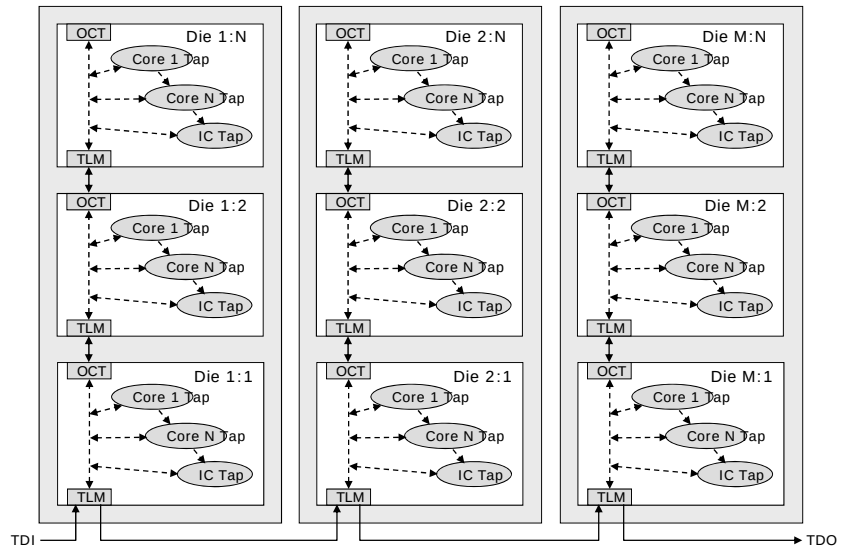
imec

4. Access to Embedded Instruments

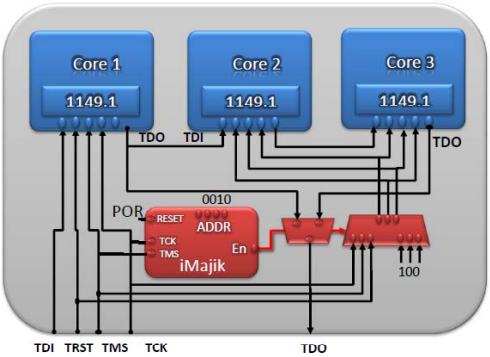
TI Proposal: TAP Linking Module + OCT

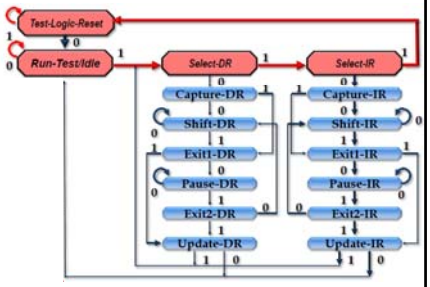


4. Access to Embedded Instruments

Intellitech Proposal: iMajik

[Clark – VTS'10]





5+6. Test Data Formats

- **Wafer Maps**
  - Pass/fail information per die
- **Inkless Assembly and Single-Device Tracking**
  - Die to wafer location and wafer processing
  - Die to assembly, packaging, and test processes
  - All dies in multi-chip package
- **Standard Test Data Format (STDF)**
  - File format for (diagnostic) IC test data collection
  - Currently at STDF-v4 (2007), developing JTDF

Standards

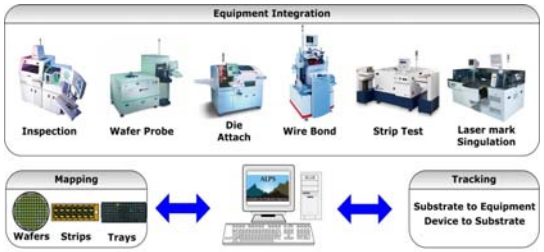
SEMI G81/G85
- obsolete

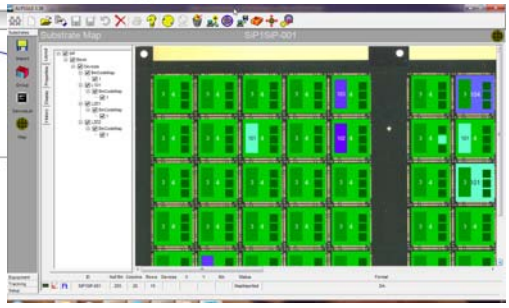
SEMI E142
- Already handles 3D?

SEMI STDF-v4
- Requires extension to 3D

5. Wafer Maps

SEMI E142





Source: Dave Huntley, Kinesys

Conclusion

- 3D-SIC: hot topic w.r.t. processing, design, and now also test
- 3D-Test Standardization Study Group active per January 2010
- Topics under discussion
  - Die and Stack Test
    1. DfT test access architecture
    2. Wafer probe interface
  - Access for Board-Level Users
    3. Board-level interconnect test
    4. Access to embedded instruments
  - Test Data Formats
    5. Wafer map and device tracking
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