Logistics for ResE Timing/Synchronization Work

Draft Rev. 0

December 7, 2005

Outline

- Introduction
- Items needed for ResE timing/synchronization specifications
  - Protocol related
  - Profile related
- Items in IEEE 1588
  - Current version (version 1)
  - New version (version 2)
- Possible division of ResE work
- Current view on possible solution

Introduction

- The current draft ResE Timing/Synch PAR indicates that the standard will specify the use of IEEE 1588 in the context of IEEE Stds 802.1D and 802.1Q with the purpose of meeting the synch requirements for time sensitive applications such as audio and video across Bridged and Virtual Bridged LANs (both protocols and procedures will be specified)
- The draft PAR also indicates that the standard will leverage the emerging version of IEEE 1588 to develop the additional specs required to address these requirements

Introduction (Cont.)

- In a recent ResE call, 2 possible sets of logistics for working with IEEE 1588 were discussed
  1) Individuals would submit work directly to IEEE 1588, and the work would essentially be done there
  2) Individuals would submit work to the ResE group; the work would be done there and then liaised to IEEE 1588
- The ResE group preferred approach 1); the author was asked to communicate this to the IEEE 1588 committee in their next regular call

Introduction (Cont.)

- The IEEE 1588 Committee indicated it needed more detail on the needs of ResE, e.g., what does “leverage the new version of 1588 to the fullest extent possible” mean?
  - The 1588 Committee said that its PAR for version 2 is already approved, and it needs to understand how the ResE work would fit into this PAR (or if a new or modified PAR would be needed)
  - Once the work is better understood, it can be determined which subcommittee the work would proceed in
- The 1588 Committee asked for a presentation from the ResE group addressing these issues

Items Needed for ResE Timing/Synch Specifications

- The list of items needed is divided into two categories
  - Protocol-related items
  - Profile-related items
- This is done mainly for convenience, as traditionally IEEE 1588 has specified protocol-related items, while each application area of 1588 has specified profiles in other documents (usually in other standards bodies)

Items Needed for ResE Timing/Synch Specifications (Cont.)

- Protocol-related items
  - Layer 2 message definitions and formats
    - Definition of each field in each message type
      - Format for representing time would be included here
      - This would address whether every message carries full information needed for both phase/frequency compensation and Grandmaster selection (or whether the two aspects could be in separate messages)
  - Definitions of communication path, sub-domain, domain
  - Message exchange procedure/sequence
    - Two-way versus one-way with less frequent two-way messages
    - Nominal inter-message time
  - Algorithm for selecting grandmaster and synch paths

Items Needed for ResE Timing/Synch Specifications (Cont.)

- Protocol-related items (Cont.)
  - Clock type(s) (but only high-level indication; detailed clock requirements are part of profile)

Items Needed for ResE Timing/Synch Specifications (Cont.)

- Profile-related items
  - Phase and frequency compensation algorithms, e.g.
    - Filtered phase adjustments with less frequent instantaneous frequency adjustments, possibly with synch intervals between successive pairs of clocks syntonized or synchronized
    - Frequency compensated clock (FCC), possibly with synch intervals between successive pairs of clocks syntonized or synchronized
    - Offset and frequency compensated clock (OFCC), possibly with synch intervals between successive pairs of clocks synchronized
    - Etc.

Items Needed for ResE Timing/Synch Specifications (Cont.)

- Profile-related items (Cont.)
  - Filter requirements
    - Where filtering is done (e.g., end nodes only, end nodes and intermediate nodes with possibly different requirements for each)
    - Equivalent bandwidth and gain peaking (or other equivalent parameters) for each filter location (application dependent for end node; essentially is demapper filter)
  - Eventual solution must allow any expensive filtering needed by stringent applications (e.g., uncompressed digital video) to be done at the endpoint demapper (so that the expense can be limited to the stringent application and not be borne by the entire network)
    - Does not preclude filtering at intermediate nodes, but requires that cost of such filtering be acceptable for network

Items Needed for ResE Timing/Synch Specifications (Cont.)

- Profile-related items (Cont.)
  - Time-stamp measurement accuracy
    - Eventually must specify layer for time-stamp measurement; this spec may be in IEEE 802.3
  - Clock requirements
    - Frequency accuracy, possibly jitter and wander generation

Items in IEEE 1588

- Current version (list is not all-inclusive, and level of detail is limited)
  - Message types and formats
    - Includes format for representing time
    - Current transport is over Layer 3; Annex D (normative) specifies case where Layer 2 is Ethernet (layer 3 is still present in this case)
  - Definitions of communication path, sub-domain, domain
  - Clock types (boundary clock, ordinary clock)
  - Clock quality (stratum levels)
  - Message exchange procedure/sequence
  - Best master clock algorithm

Items in IEEE 1588 (Cont.)

- Current version (Cont.)
  - Detailed state machines for clocks for various message exchanges, and data maintained by each clock
  - Some performance statistics definitions (e.g., Allan variance)
    - But not specified whether this must be measured in real time versus supplied by the clock vendor, integration and sampling times, or any requirements
  - Synch interval limited to 1, 2, 8, 16, and 64 s

Items in IEEE 1588 (Cont.)

- New version (this information is taken from v2 PAR)
  - Layer 2 mappings (i.e., no layer 3 present)
  - Higher sampling rates (synch interval less than 1 s), with shorter messages defined
  - Transparent clock, to limit phase error accumulation in long chains
    - Phase error accumulation in long chains if clocks have narrow bandwidth, large noise generation, and large gain peaking (which can be the case for inexpensive oscillators)
  - Fault tolerance
  - Security

Possible Division of ResE Work

- Protocol-related items on slides 7 and 8 fall within current and/or new versions of IEEE 1588
  - ResE will operate at Layer 2; message definitions and formats could be done under layer 2 work for version 2
  - ResE would use simplified version of 1588 communication path, sub-domain, and domain
    - Essentially, a single ResE would be one sub-domain with one grandmaster
    - All ResE links will be point-to-point (in current PARs; ResE over wireless will be covered in future work); each link is a communication path

Possible Division of ResE Work (Cont.)

- Protocol-related items (Cont.)
  - Message exchange procedure could be a simplified version of 1588 version 1 message exchanges
    - E.g., No explicit followup message; instead the time placed in sync could be the time of the previous sync message
    - At present, transparent clocks have not been heavily discussed in ResE, though not explicit decision to preclude using them
  - Algorithm for selecting grandmaster and synch paths could be simplified version of Best Master Clock Algorithm
    - ResE does not need multiple clock stratum definitions; expected that there will be a single clock quality

Possible Division of ResE Work (Cont.)

- Protocol-related items (Cont.)
  - ResE will need short synch interval to achieve desired jitter and wander performance
    - Likely no more than 1 ms, and possibly less than 1 ms (though not less than 0.1 ms)
    - Consequently, layer 2 messages used by ResE to carry timing information will need to be short (compared to 1588 v1 messages)
    - May be desirable for ResE to have separate messages for timing information and grandmaster selection information

Possible Division of ResE Work (Cont.)

- Profile-related items on slides 9 – 11 fall within draft ResE Timing/Synch PAR, but not within IEEE 1588 v1 nor v2 PAR
- Profile related items could therefore easily go in a new 802.1 document
  - If they were included directly in 1588, a new or revised 1588 PAR would likely be needed

Possible Division of ResE Work (Cont.)

- Possible division of work
  - Include protocol-related items in IEEE 1588
    - Development of short messages at layer 2, simplified message exchange, plus simplified version of best master clock algorithm
  - Include profile-related items in new IEEE 802.1 document

Possible Division of ResE Work (Cont.)

- The carrying out of the work would be greatly facilitated if it could be done in a single thread of phone calls
  - If all the work in 1588 were under a single subcommittee, it might be possible to coordinate the calls
    - E.g., 802.1 ResE call for profile related work could immediately follow the respective 1588 subcommittee call
  - May be difficult, though, if the work in 1588 falls under multiple subcommittees

Possible Rough View of Solution

- Single sub-domain with one grandmaster (for one ResE)
- Single clock quality
- Short messages, defined at layer 2
- Message exchange procedure is slightly simplified version of current 1588 procedure (e.g., no followup message; time in sync refers to previous sync; retain delay_req and delay_resp (but less frequent exchanges of these)

Possible Rough View of Solution (Cont.)

- Algorithm for selecting grandmaster and sync paths is simplified version of best master clock algorithm
- Phase and frequency compensation algorithm will be one of the algorithms on slide 9
- Filter and clock requirements TBD (except it is known now that clock frequency accuracy will be ± 100 ppm)
  - Inexpensive filtering at intermediate nodes
  - Any expensive filtering will be limited to demappers at end nodes (end devices) and expense will be limited to and borne by the applications that require it

Possible Rough View of Solution (Cont.)

- Time stamp measurement accuracy TBD
  - Very likely that measurement will be at least (i.e., at a layer no higher than) between the PHY and MAC