Specifying P802.1Qbv Gate Schedules

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Setup

- P802.1Qbv schedule specification.
- All schedule times are in terms of nanoseconds.
- Cycle time (repeat time) is in terms of nanoseconds.
- Systems implementing these have clock ticks of some frequency that is not necessarily an integral number of nanoseconds.
- The clocks that drive the schedule may or may not be syntonized with the PTP-synchronized system clock.
- How do we get the schedules in sync (long term), and know what will actually happen?

Problem 1

- The requirement for the length of one schedule cycle can be either:
  - *N* nanoseconds per cycle; or
  - *M* cycles per second.
- These are not equivalent, when it comes to functionality, and go to the root of the problem.
- If the goal is to have 3 cycles per second (333.333… ms per cycle), and some devices have a 300 MHz clock and some have a 500 kHz clock, then implementing a cycle in terms of an integral number of clock ticks per cycle is doomed to failure, in the long term.

Solution 1

- The length of a cycle can be expressed **either** as:
  - *N* nanoseconds per cycle; or
  - *M* cycles per second.
- It is the responsibility of a system to ensure, within some accuracy that is made known to the system controller, that it will operate at the requested cycle length.

Problem 2

- The same issues apply the the open/close events within a port's schedule.

Solution 2

- Schedules are given in terms of nanoseconds, not frequency.
- There is a mechanism by which the system makes its resolution and accuracy parameters known to the central controller.
- The schedule creator takes into account the systems' accuracy and resolution parameters.
- A system takes the schedule given it in terms of nanoseconds, and converts that schedule by mathematical rounding to its own schedule of time ticks, assuming a perfectly accurate start of cycle for the schedule.
- A system starts each cycle, to the best of its ability, to exactly the time or frequency specification of the cycle period.

Problem 3

- **This necessarily means that the system is required to start cycle *n*+1 either shortly before, or shortly after, the end of cycle *n*.**

Solution 3

1. The schedule creator must not schedule an event closer to the end of the schedule than the amount of overlap made possible by a system's stated resolution and accuracy.
2. The schedule create must understand that the time span between the last event in the schedule and the first event in the schedule has to accommodate the largest overlap or gap possible by these factors. That is, this one event-to-event period has a higher inaccuracy than other events.
3. The system has to deal with this uncertainty in some manner, to ensure that a frame transmission does not extend beyond the end of a window.

- Make every effort to start each cycle at the right time according to the system synchronized clock.

- Each cycle's duration is defined by a number of local ticks.
- Therefore there can be overlap or gaps.

Thank you.