IEC / IEEE 60802 - IA profile

Synchronization problems -
identified topics for IEEE 802.1AS-Rev

-To be discussed-

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Basic scope

IEC / IEEE 60802 decided to use IEEE802.1AS-Rev for synchronization

Fulfillment of the requirements for synchronization need to be checked; deviations need to be stated and solved

Path delay calculation

Precise path delay shall be available latest 1s after Link Up.

Thus, at least five path delay measurements as a burst after Link Up shall be supported by all IA profile devices.

-> Valid path delay available in less than 1s

Asymmetric cable delay

Transparent media converters leading to asymmetric cable delay need to be supported.

Thus, from the path delay calculation point of view asymmetric cable delay, e.g. up to 10µs, shall be supported.

-> Valid path delay available even with asymmetric cable delay

Cable delay

Cable delay for copper may be bigger than 800ns

Thus, any limitation to this value need to be changeable.

-> Valid path delay available even with cable delay greater than 800ns

Bridge delay

IEEE802.1Q / IEEE802.1AS-Rev moved the reference point to the MDI.

Thus, bridge delays based on this model are now port depended if different PHYs or MAU-Types are used.

-> Need to be covered by the defined management objects or model for bridge delay need to be changed

Bridge delay - model

IEEE802.1Q / IEEE802.1AS-Rev moved the reference point to the MDI.

What level of PHY offset / jitter can be accepted to support the system definitions (100 nodes, 1µs, 3ppm/s frequency drift in a range of 100ppm, …)?

-> Need to be covered by the TSN-IA profile

Synchronization intervall

Working Clock uses the existing <100ppm (100Mbit/s devices) or <50ppm (1Gbit/s) oscillators. Precision of <1µs for linear topology with up to 100 nodes needs to be achieved with this hardware.

Thus, synchronization interval of 30ms (for WorkingClock) shall be supported to fulfill the required precision for the whole temperature range.

-> Need to be covered by IA profile supporting devices

Detection of Grandmaster loss

Each device using Working Clock needs to detect Grandmaster loss in less than 100ms to avoid destruction of machine, even in linear topologies with 100 nodes.

Thus, means to detect Grandmaster loss such fast need to be supported by IEEE802.1AS-Rev

->IA profile devices need to support this

Fast lock in “sync within <1µs accuracy”

Working Clock need to be always inside the required <1µs range. Thus, a clear definition of “sync within <1µs accuracy” is needed. Additional this state shall be achieved in less than 1s per device.

Thus, means to detect “sync within <1µs accuracy” need to be defined

->IA profile devices need to support this

Sync forwarding delay

Working Clock need to support 100 nodes in linear topology. Thus, the maximum sync forwarding delay needs to be limited; e.g. to <10ms.

Example: 100 nodes; 10ms sync forwarding delay -> Origin timestamp is more than 1s old; 1s dead time for disciplining the slave time

->IA profile devices need to support this

Sync tree

Portions of the network, including Grandmasters may be switched on / off during production e.g. to save energy. This shall not change the sync tree to avoid unexpected switch over between Grandmasters.

Thus, sync tree needs to be administered external for all needed domains.

->IA profile devices need to support this

Grandmaster switchover

Vendor defined hierarchy of Grandmasters needed to ensure the planned/expected behavior in case of Grandmaster loss.

Thus, sync tree needs to be administered external for all needed domains. And switchover hierarchy needs to be administered.

->IA profile devices need to support this

One step sync or hardware optimized two step

Ensuring minimal sync forwarding delays may be done by supporting either one step sync for all needed sync domains or two step sync for all sync domains in hardware.

This may help to reduce the sync forwarding delay to <1ms.

->IA profile devices should to support this

Implicit sync domain boundary

Vendor defined sync domain boundaries, particular for Working Clock, need to be kept.

Thus, a concept e.g. based on LLDP needs to be defined and implemented

->IA profile devices need to support this

Diagnostics for synchronization

Vendor expects to get diagnostic information from the devices in case of sync problems, e.g. Grandmaster loss

Thus, a concept e.g. based IEEE802.1AS-Rev management objects needs to be defined

->IA profile devices need to support this

IEEE802.1AS-Rev management objects

Vendor independent setup / parameterization for synchronization is expected covering all needed domains and features.

Thus, a concept based IEEE802.1AS-Rev management objects needs to be defined

->IA profile devices need to support this

Working Clock only

Devices may start without Universal Time using only Working Clock (Domain ID !=0). Later a Grandmaster for Universal Time (Domain ID =0) is added. Adding the Universal Time later shall not influence the running Working Clock.

Thus, this needs to be covered by IEEE802.1AS-Rev

->IA profile devices need to support this

Thank you

Questions?

Publications - 1

- *"An Optimal Control Approach to Clock Synchronization"*, Philipp Wolfrum, Ruxandra Lupas Scheiterer and Dragan Obradovic, 2010 International IEEE Symposium on Precision Clock Synchronization for Measurement, Control and Communication (ISPCS), September 29-October 1, 2010, University of New Hampshire, Portsmouth, USA.

- *"Optimal Estimation and Control of Clock Synchronization Following the Precision Time Protocol"*, Chongning Na, Philipp Wolfrum, Dragan Obradovic and Ruxandra Lupas Scheiterer, 2010 IEEE Multi-Conference on Systems and Control (MSC), September 8-10, 2010,Yokohama.

- *"Clock Synchronization Based On Distributed Hidden State Estimation"*, C. Na, R. L. Scheiterer, D. Obradovic and J. A. Nossek, 2009 International IEEE Symposium on Precision Clock Synchronization for Measurement, Control and Communication (ISPCS), October 12-16, 2009, University of Brescia, Brescia, Italy.

- *"Improving Synchronization Performance of the Precision Time Protocol"*, P. Wolfrum, C. Na, R. L. Scheiterer, D. Obradovic, G. Steindl, poster at Symposium on Recent Trends in Networked Systems and Cooperative Control (NESCOC), Workshop on Network-Induced Constraints in Control (NETCOC), Sept. 28-29, 2009, Univ. of Stuttgart, Germany.

- *"A Kalman Filter Approach To Clock Synchronization Of Cascaded Network Elements"*, C. Na, R. L. Scheiterer, D. Obradovic, 1st IFAC Workshop on Estimation and Control of Networked Systems (NecSys'09), 24-26 September, 2009, Venice, Italy.

Publications - 2

- *"Probabilistic Model for Clock Synchronization Of Cascaded Network Elements",* C. Na, D. Obradovic, R. L. Scheiterer, International Instrumentation and Measurement Technology Conference (I2MTC), 5-7 May 2009, Singapore.

- *"A Probabilistic Approach to Clock Synchronization of Cascaded Network Elements"*, C. Na, D. Obradovic, R. L. Scheiterer, International Conference on Acoustics, Speech and Signal Processing ICASSP 09, 19-24 April, 2009, Taipei, Taiwan.

- *"Synchronization Performance of the Precision Time Protocol in Industrial Automation Networks"*, R. L. Scheiterer, C. Na, D. Obradovic and G. Steindl, IEEE Transactions on Instrumentation and Measurement, Vol. 58, Issue 6, pp. 1849 – 1857, June 2009.

- *"1µs-conform Line Length of the Transparent Clock Mechanism defined by the Precision Time Protocol (PTP Version 2)"*, R. L. Scheiterer, C. Na, D. Obradovic, G. Steindl, F.-J. Goetz, 2008 International IEEE Symposium on Precision Clock Synchronization for Measurement, Control and Communication (ISPCS), September 22-26, 2008, University of Michigan, Ann Arbor, Michigan, USA.

- *"Synchronization Performance of the Precision Time Protocol in the Face of Slave Clock Frequency Drift"*, D. Obradovic, R. L. Scheiterer, C. Na, G. Steindl and F. J. Goetz, IEEE CASE conference, August 23-26, 2008, Washington DC, USA.

Publications - 3

- *"Synchronization Performance of the Precision Time Protocol: Effect of Clock Frequency Drift on the Line Delay Computation"*, R. L. Scheiterer, D. Obradovic, C. Na, G. Steindl and F. J. Goetz, WFCS 2008, May 20-23, 2008, Dresden, Germany.

- *"Clock Synchronization in Industrial Automation Networks: Comparison of Different Syntonization Methods"*, D. Obradovic, R.L. Scheiterer, C. Na, G. Steindl and F.J. Goetz, in: Proc. of 5th International Conference on Informatics in Control, Automation and Robotics, May 11 - 15, 2008, Funchal, Portugal.

- *"Enhancement of the Precision Time Protocol in Automation Networks with a Line Topology"*, Chongning Na, Dragan Obradovic, Ruxandra Lupas Scheiterer, Günter Steindl, Franz-Josef Goetz, 17th IFAC World Congress (International Federation of Automatic Control), July 6-11, 2008, Seoul, Korea.

- *"Synchronization Performance of the Precision Time Protocol"*, Chongning Na, Dragan Obradovic, Ruxandra Lupas Scheiterer, Günter Steindl, Franz-Josef Goetz, 2007 International IEEE Symposium on Precision Clock Synchronization for Measurement, Control and Communication (ISPCS), October 1-3, 2007, Austrian Academy of Sciences, Vienna, Austria.