

# ATS

# Current Work

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# Status

## Short Summary

- First WG draft is in progress
- Goal: **Draft as complete as possible**, i.e. no stub clauses, no big changes needed afterwards
- Special Topic: Informative Delay Analysis Framework for ATS

## Challenge

- A Delay Analysis Framework has been published in 2016  
<https://ieeexplore.ieee.org/abstract/document/7557870/>
- ATS Evolved - Most important:  
IEEE 802.1Qcr allows real-world implementation inaccuracies
- The Delay Analysis Framework should take these into account!

## This Slidedeck

- Description of Inaccuracies
- Current work of the Editor

# Delay Analysis 2016

$$d_f^{max} \leq \max_{\forall f' \text{ in } Q(f)} \left( \frac{\sum_{i \in H} b_i^{max} + \sum_{i \in S} b_i^{max} + l_{f'}^{min} + \max_{i \in L} (l_i^{max})}{R - \sum_{i \in H} r_i} + \frac{l_{f'}^{min}}{R} \right)$$

Max. over all streams in the traffic class of  $f$  in the receiving bridge  
 Interference by all competing streams In at the sending bridge (not only The ones in the same class like  $f$ ).  
 S&F

## Description

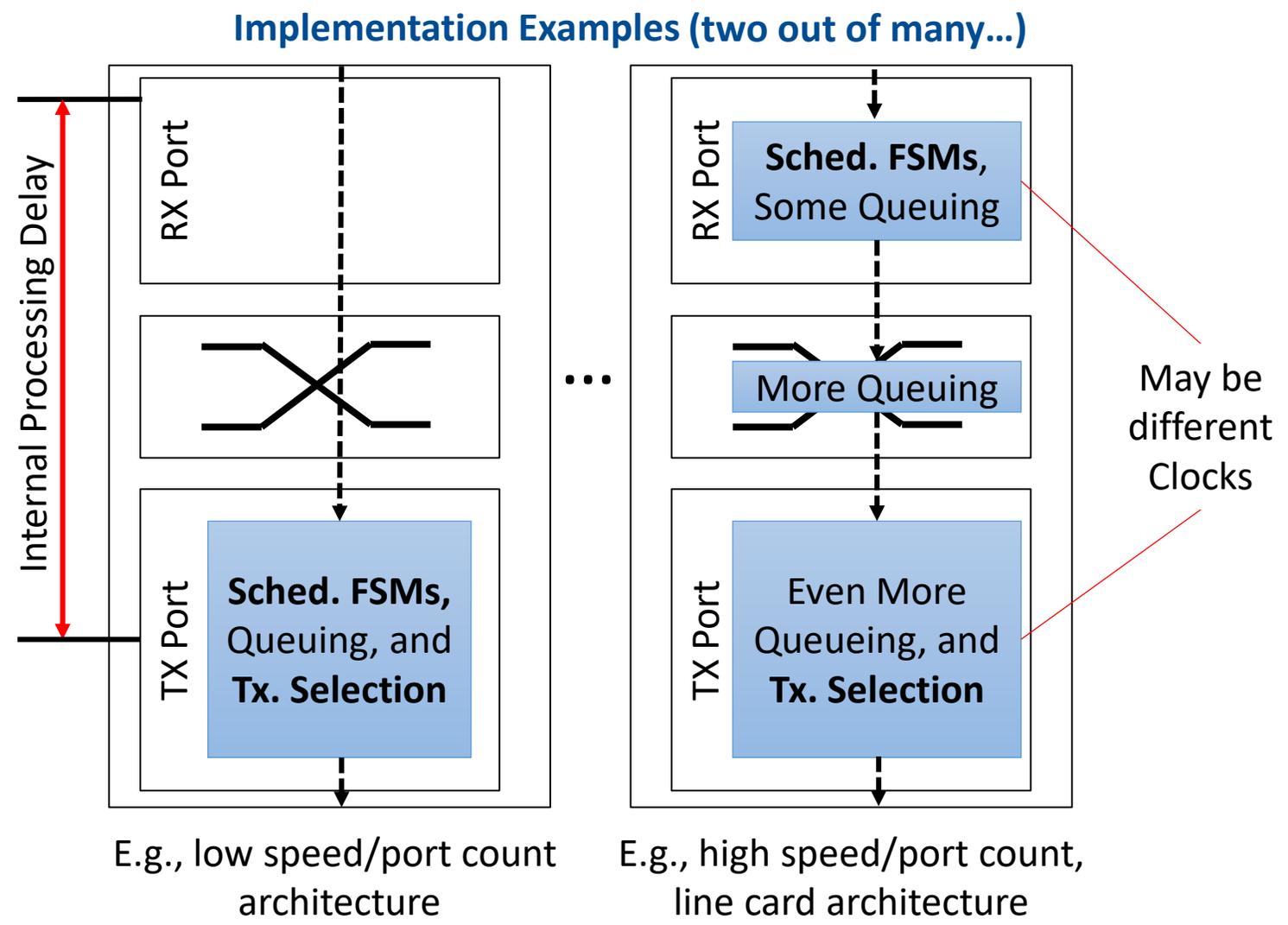
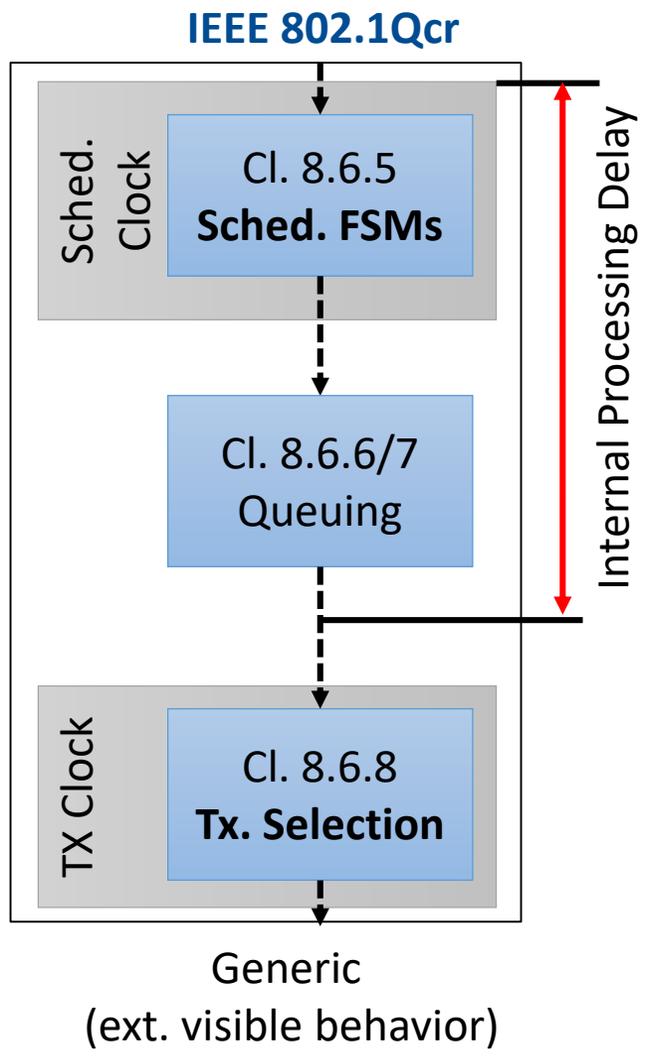
- Single hop delay bound from a sending bridge to a receiving bridge
- End-to-end: Sum of single hop delay bounds  
Note: Simplified equation for the last hop

## What is missing: Inaccuracies (the new stuff!)

- *Link Delays*  
Often rather small
- *Device Internal Processing Delays*  
Implementation dependent – implementations may vary significantly
- *Clock Inaccuracies*  
ATS entities in a bridge may be placed in different clock domains - in terms of digital logic, not in terms of 802.1AS or similar (!)

Term	Description
$d_f^{max}$	Max. per hop delay of a stream $f$ .
$\sum_{i \in H} b_i^{max}$	Sum of max. burstiness (i.e., <i>Committed Burst Size</i> parameters) of streams with a higher priority than $f'$ .
$\sum_{i \in S} b_i^{max}$	Sum of max. burstiness of stream $f$ and all streams with priority level equal to the priority level of $f'$ .
$\max_{i \in L} (l_i^{max})$	Maximum frame length of all streams with a lower priority level than $f'$ , including all non-ATS lower priority traffic classes.
$l_{f'}^{min}$	Minimum frame length of stream $f'$ .
$R$	Link speed.
$\sum_{i \in H} r_i$	Sum. of max. data rates (i.e., <i>Committed Information Rate</i> parameters) of streams with a higher priority than $f'$ .

# 802.1 Qcr Model and Implementation

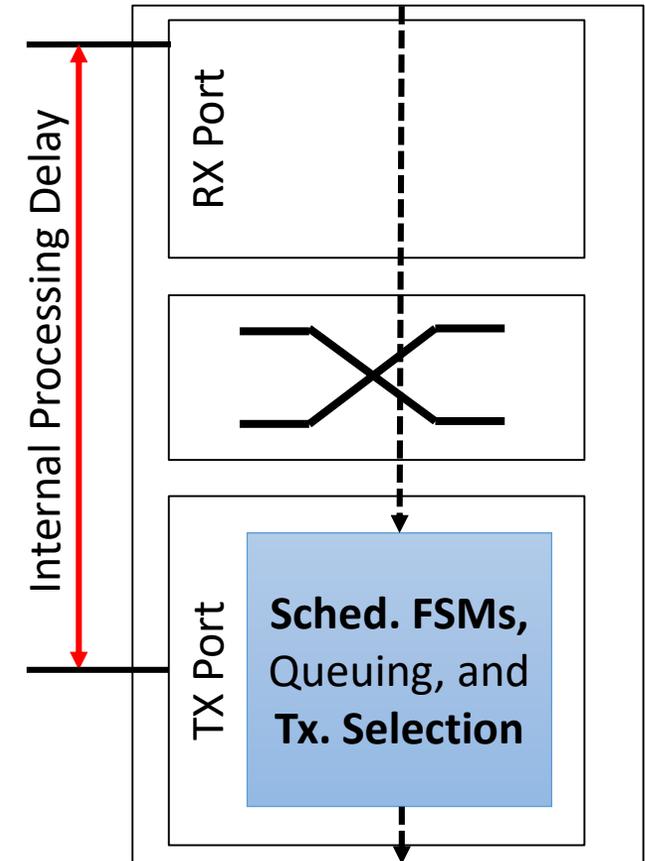


# On Inaccuracies: Delays

$$d_f^{max} \leq \max_{\forall f' \text{ in } Q(f)} \left( \frac{\sum_{i \in H} b_i^{max} + \sum_{i \in S} b_i^{max} + l_{f'}^{min} + \max_{i \in L} (l_i^{max})}{R - \sum_{i \in H} r_i} + \frac{l_{f'}^{min}}{R} \right)$$

## Rather trivial: Link and Processing Delays

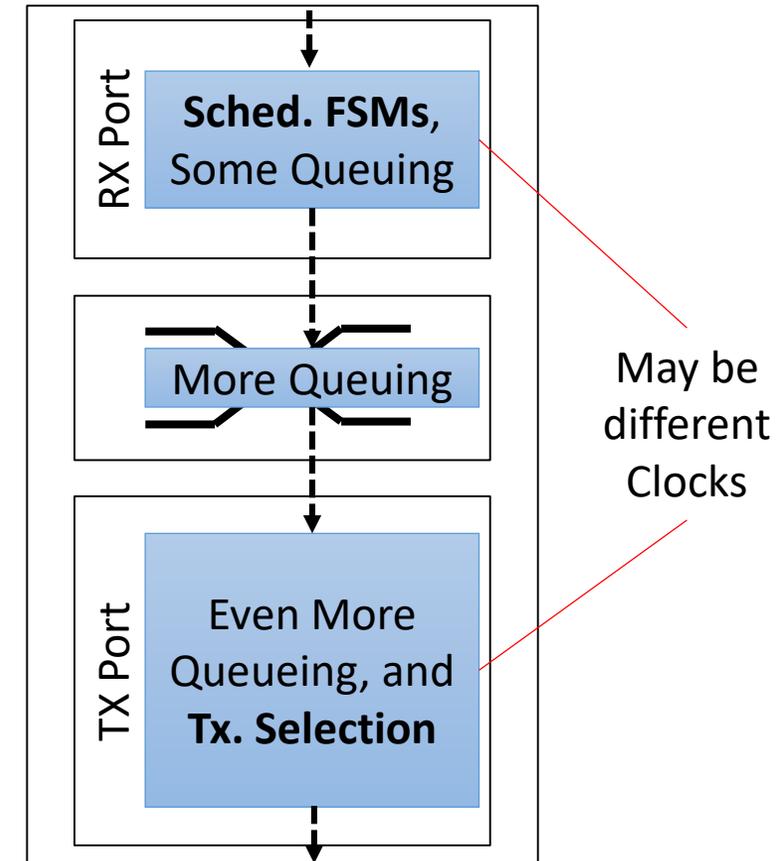
- Max. Processing delay added to the per hop delay bound
- Max. Link delay added to the per hop delay bound
- I.e.: new  $d_f^{max} = \text{old } d_f^{max} + \text{both delays}$



# Inaccuracies: Clocks

## Non-trivial: Clock Inaccuracies (Work in Progress)

- *Sched. Clock* and *Tx Clock*: Offsets and Drifts
    - Ok in IEEE 802.1Qcr, as long as the maximum offset is bounded
    - Assumed to be a desirable degree of freedom for implementers (i.e., no “very accurate” device-internal sync. mechanism needed)
  - Inaccuracies can deform traffic envelopes, as enforced by shaping
- Several questions:
- One time, two times, three times?
  - Interaction with processing above delays?
  - Does one absorb the other?
  - Packet Ordering/Race Conditions?



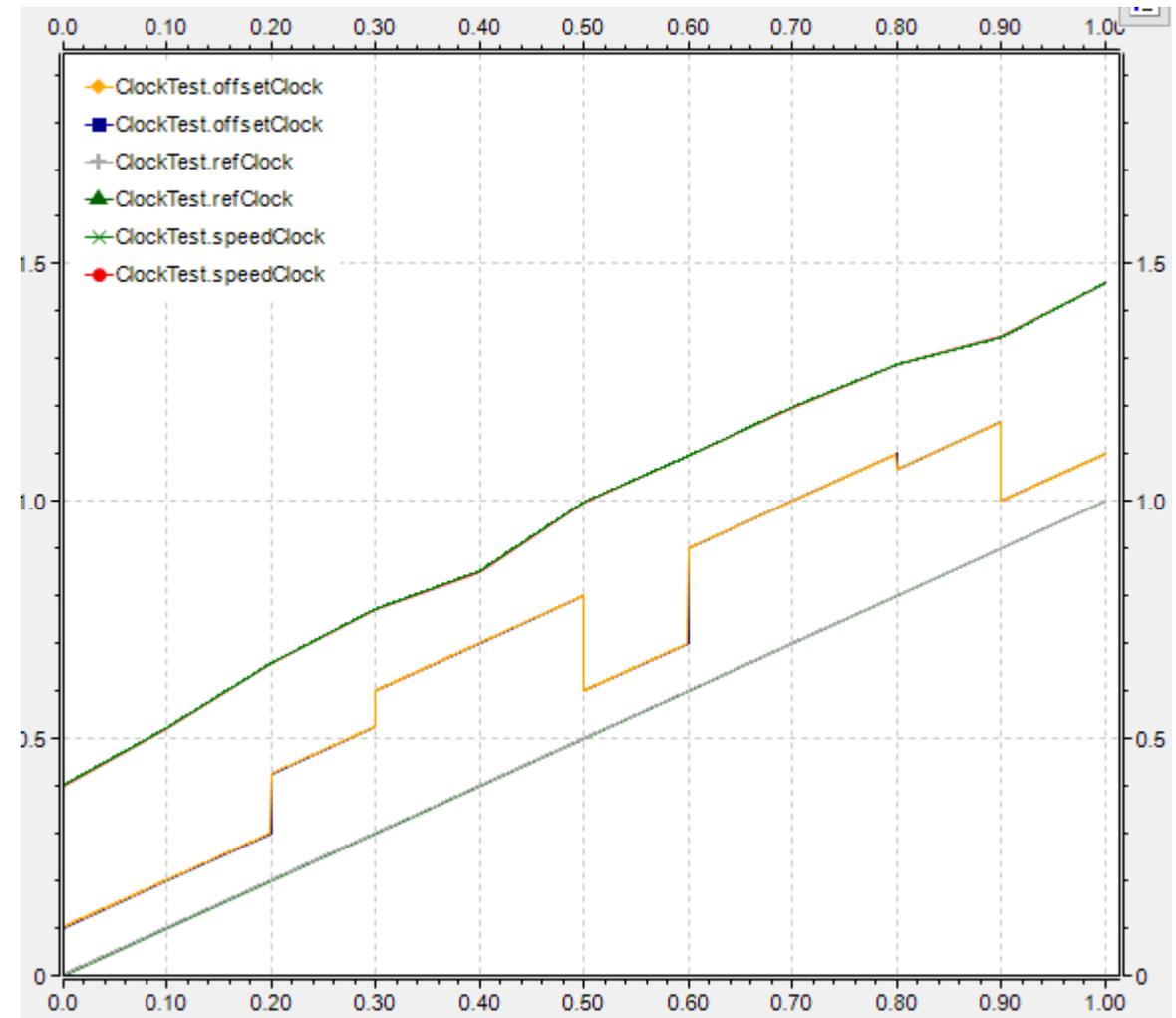
# Clocks: Obtaining Answers

## Math. Analysis

- Formal proofs (i.e., Guarantees)
- Implies abstraction

## Simulations

- NO Replacement for Analysis, but ...
  - ... Validation: “Abstraction...Gaps?”
  - ... Supportive: “How to proof?”
- Feedback for math. Analysis



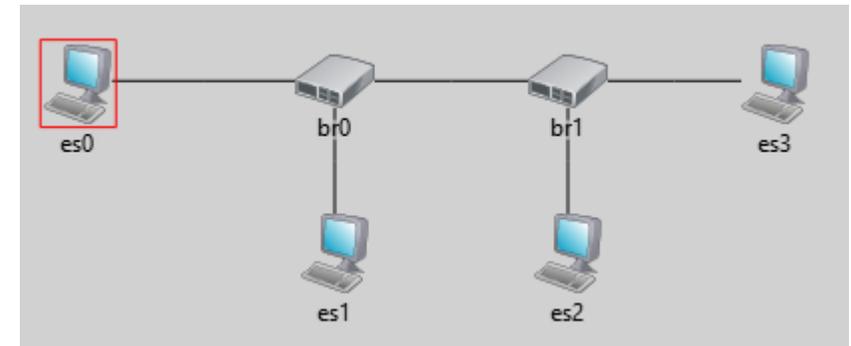
# Math. Analysis and Simulation In Progress

## Math Analysis

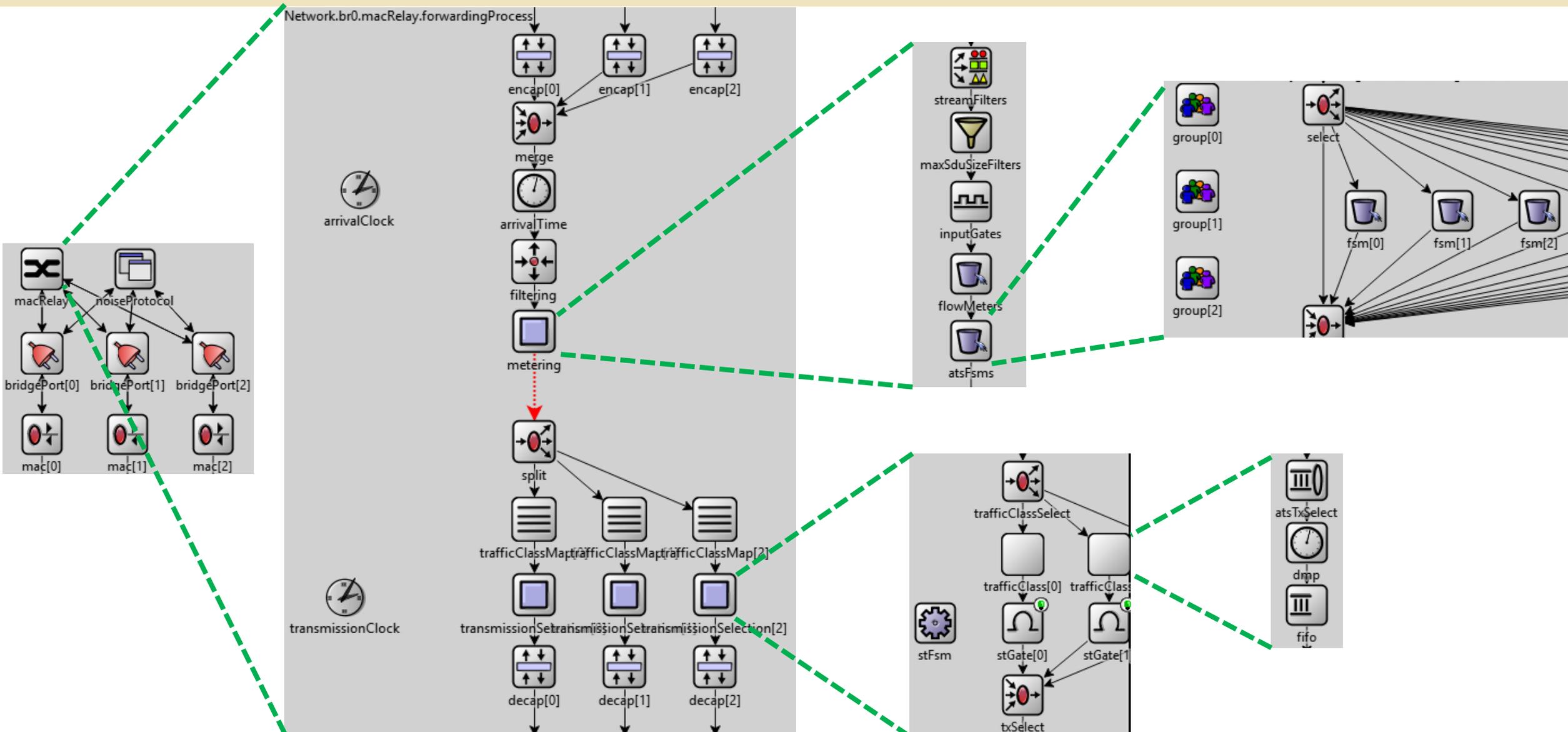
- A good guess is there ;)
- Working towards a proof
- May affect “AssignAndProceed(...)”

## Simulation close to IEEE 802.1Q

- Based on 802.1Qcr/Q-Rev 2018
  - not based on
    - UBS/ATS 2016 Models
    - Old IEEE 802.1 Std. Models
    - Particular Implementation Models
    - ...
- More 802.1Qcr: Full data plane model
- Implementation inaccuracies (like clocks):
  - Flexible submodule placement/ordering
  - Replacement by “imperfect” versions



# Bridge Model in a Nutshell



# Thank you for your Attention!

## ***Questions, Opinions, Ideas?***

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