Crystal Fundamentals & State of the Industry

Agenda

Crystal basics

- Common specifications
- Design tradeoffs and common sizes

Frequency Stability vs temperature

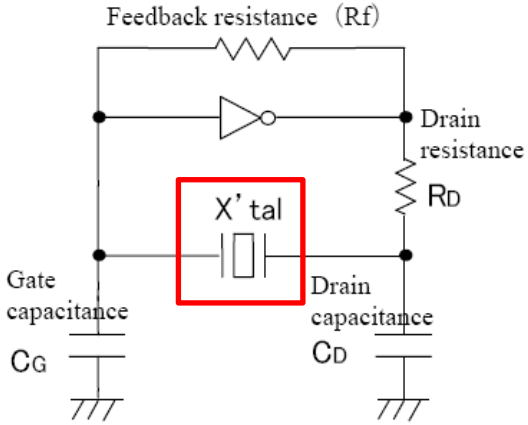
- Frequency/temp data and dependencies
- Specifying frequency stability & limitations

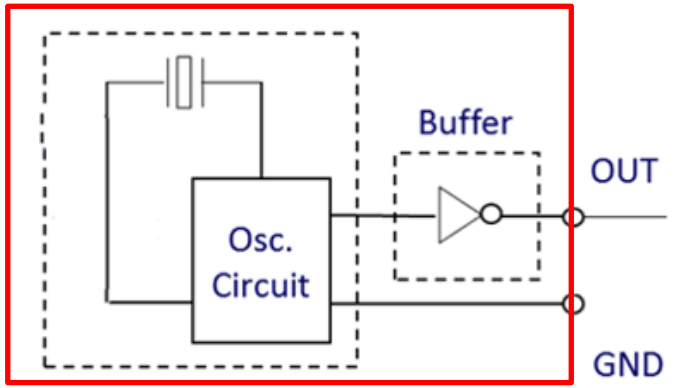
Crystal Specification & selection best practices

- Notes on frequency error specification
- Other important points for consideration

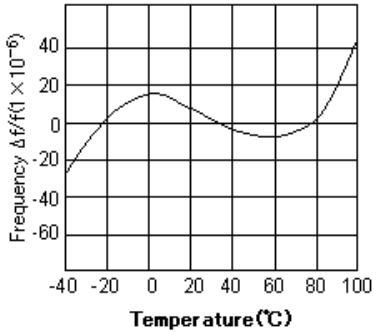
Crystal vs Crystal Oscillator

- **Crystal units** are passive devices which require an external oscillation circuit
  - The presentation hereafter is mostly regarding crystal units
- **Crystal oscillators** are active devices which have the crystal unit and oscillation circuit IC integrated into a single package
  - When evaluating or selecting crystal oscillators, the specifications of relevance will be different from a crystal unit





MHz Crystals – Basics & Specifications

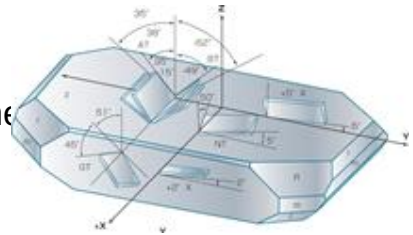


MHz crystals use the AT-cut, resonate as a bulk acoustic wave in thickness-shear vibration mode

The fundamental frequency is determined by the thickness of the crystal

Common specs

- **Frequency** – Desired nominal frequency
  - Ex. 25MHz or 50MHz for ethernet applications
- **Tolerance** – Deviation of the actual frequency from the nominal frequency value at +25C ambient temperature.
  - ±20ppm is a common maximum specification
- **Stability** – Frequency deviation over operating temperature
  - ±20ppm is a common maximum specification
- **Load Capacitance** – The expected capacitive load as seen by the crystal to deliver the nominal frequency
  - Typical CL values are between 6-20pF
- **ESR** – Equivalent Series Resistance or motional resistance. The higher the value, the more difficult for oscillation start up.
  - 80Ω is a common maximum specification for 2x1.6mm crystals
- **Drive Level** – Power or oscillation output level required to operate (drive) a crystal device.
  - 100µW is a common maximum specification



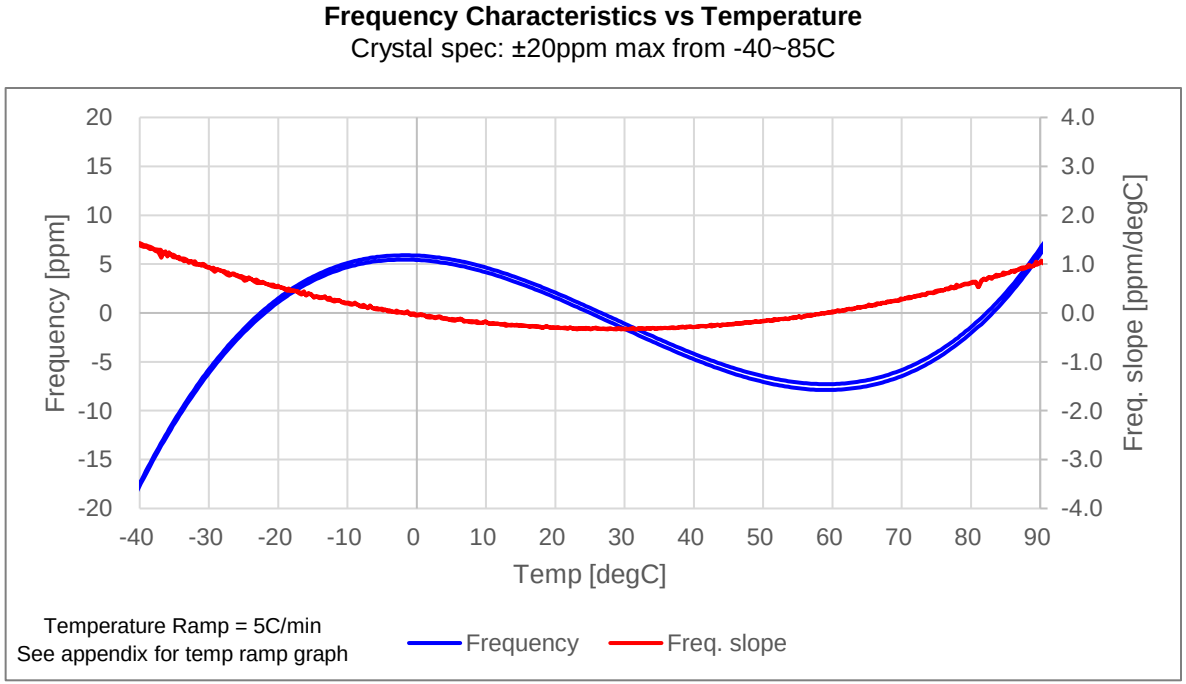
MHz Crystals – Size & Tradeoffs

MHz crystals follow industry standard footprints from 5x3.2mm to 1x0.8mm

- **Size tradeoffs**
  - Larger crystals: lower ESR, higher maximum drive level, lower minimum frequency range
  - Smaller crystals: higher capacity, tighter process control, higher maximum frequency, longer product lifecycle horizon
- **Frequency tradeoffs**
  - Higher frequency: lower ESR
- **Industry "sweet spot" is currently at 2x1.6mm for high volume projects**
- **Many lower volume projects still use crystals are large as 3.2x2.5mm**

Frequency Stability vs Temperature

- Max frequency slope is ~1.5ppm/C at -40C
- Below ~100C, max frequency deviation and frequency slope occurs at -40C
- Above ~100C, max frequency deviation and slope occur at the maximum specified temperature



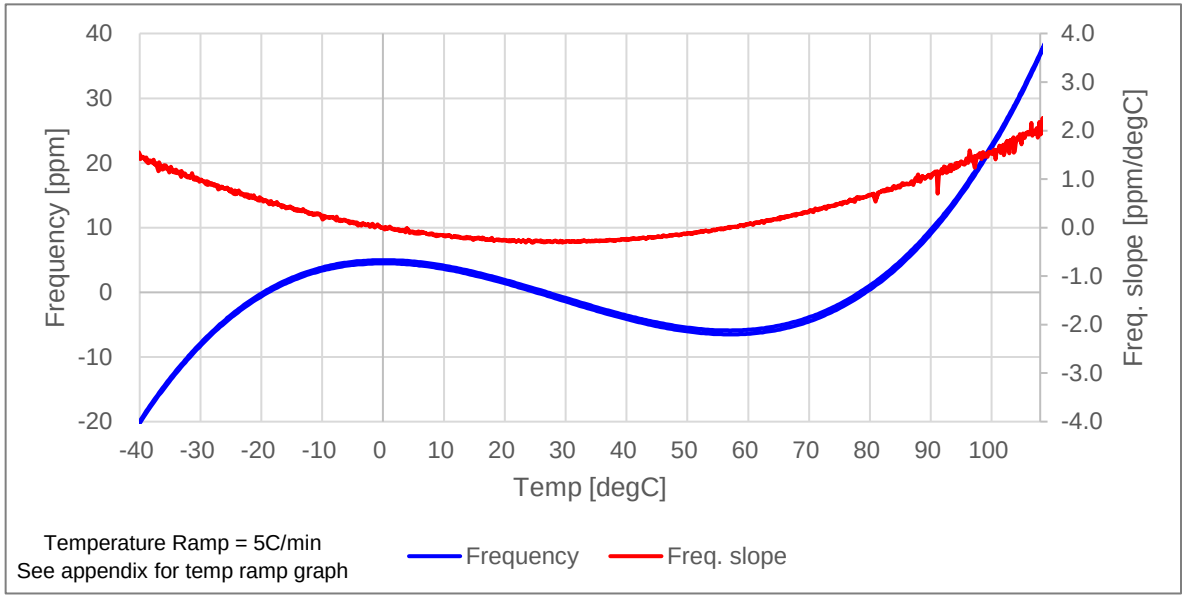
* Variance in the frequency vs temp plot above is due to hysteresis

f/T curves will be a similar shape and size for most AT-cut crystals, but may vary slightly across frequency, manufacturer, technology, cut angle, etc.

Frequency Stability vs Temperature

- Max frequency slope is **~2ppm/C at 105C**
- Below ~100C, max frequency deviation and frequency slope occurs at -40C
- Above ~100C, max frequency deviation and slope occur at the maximum specified temperature

Frequency Characteristics vs Temperature
Crystal spec: ±50ppm max from **-40~105C**

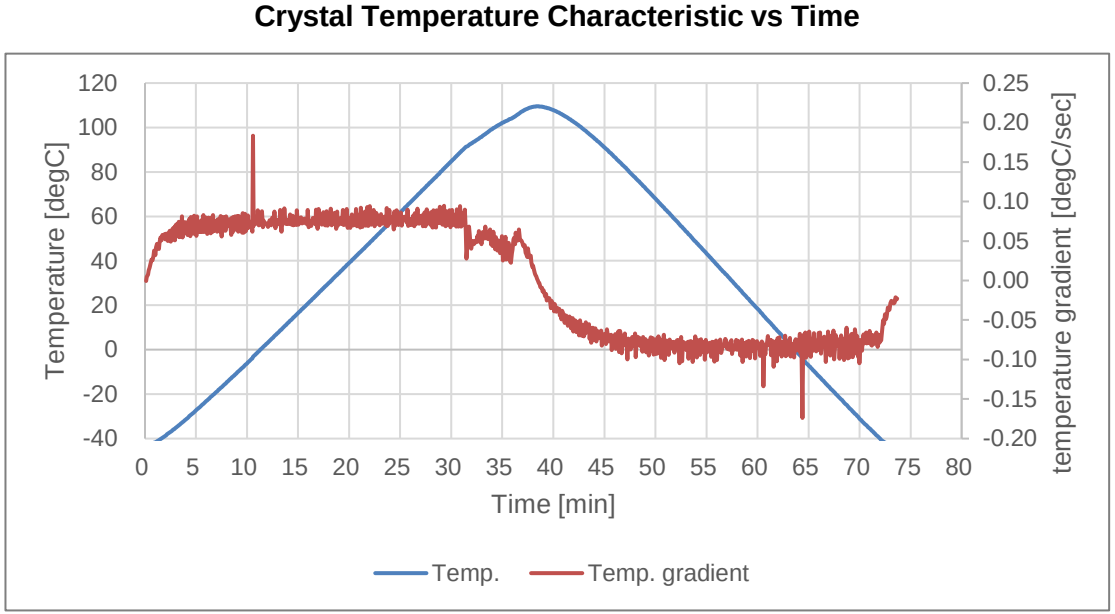


* Variance in the frequency vs temp plot above is due to hysteresis

f/T curves will be a similar shape and size for most AT-cut crystals, but may vary slightly across frequency, manufacturer, technology, cut angle, etc.

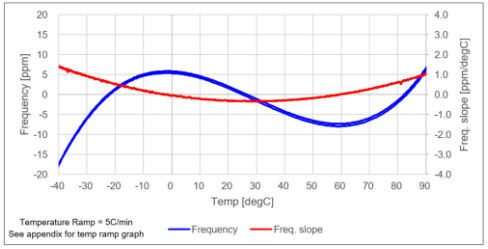
Temperature Ramp and Gradient

- For this data, we used a special crystal product with built-in thermistor
- Temperature is measured at the crystal unit by the thermistor
- Temperature ramp rates above 5C/min resulted in an erratic non-linear temperature profile from the chamber



Temperature ramp is set at 5C/min nominal due to limitations of our test environment

Specifying Frequency Stability



Industry Specifications

- Frequency stability (f/T) common.
  - All crystal products will specify this in product datasheets
- Frequency slope (df/dT) not used, unlikely to provide max specification
  - df/dT is sometimes specified for TCXO products
- Frequency/time slope (df/dt) not used, unlikely to provide any specification
  - Never specified for frequency control products

Test Equipment Limitations

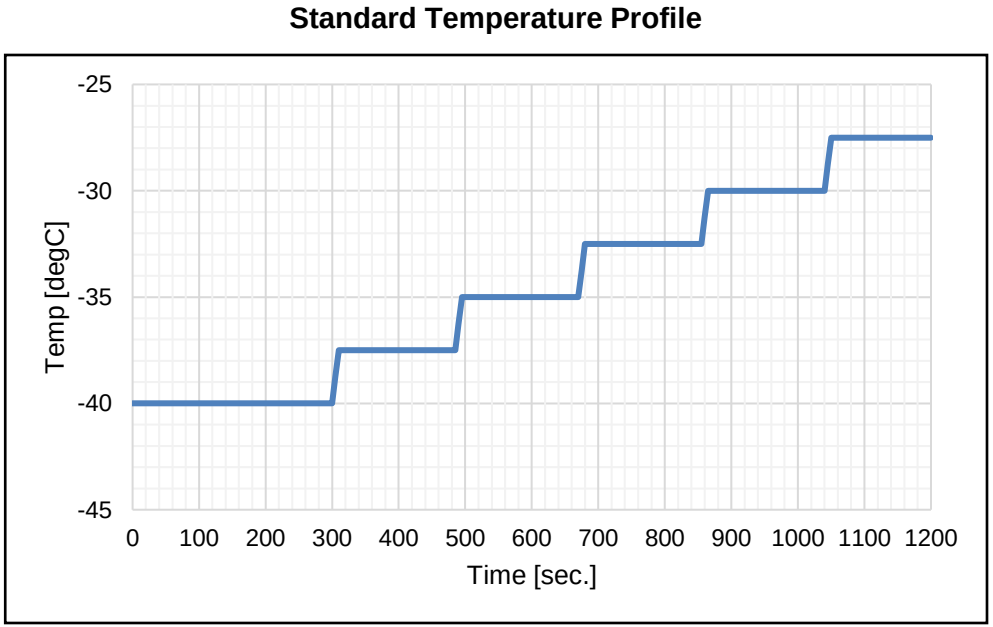
- Industry-standard crystal production test equipment does not support linear temperature profile
- Test equipment usually captures the temperature of the oven, not the crystal

Specifying Frequency Stability

Typical temperature evaluation conditions are non-linear

Example conditions

- Range: -40~125C
- Temp step: 2.5C
- Initial cold temp hold: 300 seconds
- Soak time: 180 seconds
- Ramp time: 10-15 seconds
- Frequency measurement: 10 seconds



Frequency measurement will be made immediately before the temperature change

Temperature data is from the ambient chamber temperature

Crystal Specifications

A crystal's total frequency error budget:

a) **Frequency Tolerance** – The difference between the actual frequency of the crystal from the nominal frequency value at +25C.

b) **Frequency Stability** – The maximum frequency shift due to temperature across a given temperature range.

c) **Aging** – The maximum frequency drift expected in a crystal over time.

It's important to specify whether the requirement is for total frequency error or only frequency stability

[3] Operating Conditions

Item	Symbol	Rating value			Unit	Note
		Min.	Typ.	Max.		
Operating temperature range	T_use	-40	-	+85	°C	
		-40	-	+105		Please contact Epson
Level of drive	DL	1		200	µW	Recommended: 1 µW to 100 µW

[4] Static Characteristics

Item	Symbol	Specifications	Unit	Condition / Remarks
Nominal frequency range	f_nom	16.000 to 54.000	MHz	
Frequency tolerance (Standard)	f_tol	±10 ±30	x10^{-6}	T_use = +25 °C ± 3 °C DL = 100 µW Does not include frequency aging Please contact Epson for requirements not listed in the specifications
Frequency vs. temperature characteristics (Standard)	f_tem	±10 ±30	x10^{-6}	Reference at T_use = +25 °C ± 3 °C -20 °C to +75 °C Please contact Epson for requirements not listed in the specifications
Load capacitance	CL	6 to ∞	pF	Please specify
Motional resistance (ESR)	R1	Table 1.	Ω	π circuit IEC 60444-2 T_use = Operating temperature range DL = 100 µW
Shunt capacitance	C0	3.0 Max.	pF	
Frequency aging	f_age	±1 Max. (16 MHz ≤ f_nom < 40 MHz) ±2 Max. (40 MHz ≤ f_nom ≤ 54 MHz)	x10^{-6}	T_use = +25 °C ± 3 °C First year

Table 1.

Frequency	R1
16 MHz ≤ f_nom < 18 MHz	200 Ω Max.
18 MHz ≤ f_nom < 20 MHz	150 Ω Max.
20 MHz ≤ f_nom < 26 MHz	100 Ω Max.
24 MHz ≤ f_nom < 26 MHz	80 Ω Max.
26 MHz ≤ f_nom ≤ 54 MHz	60 Ω Max.

Selection Best Practices

For crystal specification & selection, it is recommended to note best practices on topics not covered in this presentation

- ESR, drive level, CL
- Circuit layout

- These topics are well documented. Information available in the appendix and available online

Recommendations

1. Current frequency slope (df/dT) simulation budget of 3ppm/sec (~6ppm/C) is conservative for -40~85C temperature range
2. Frequency slopes of ~2ppm/C are achievable across the industry
3. Specifying a maximum frequency slope may be difficult for crystal suppliers
4. When specifying frequency error, it is recommended to clarify whether total frequency error or frequency stability over temperature (f/T) is being specified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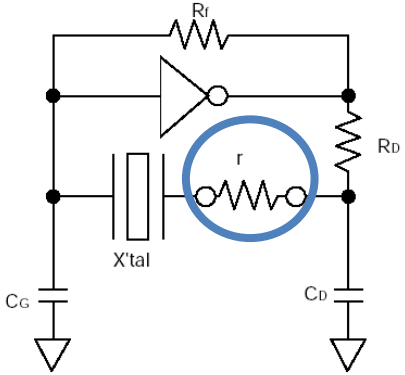
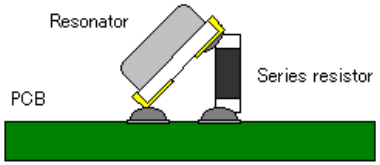
Equivalent Series Resistance (ESR)

- **To ensure sufficient oscillation margin, negative resistance (-R) is measured with a test resistor (r) in series with the crystal.**
- **Continue to increase r value until oscillation stops**
- **For stable oscillation: Oscillation Margin should be > 5 x Max ESR**



|-R| = r + ESR

$$ESR = R1\left(1+\frac{C0}{C_L}\right)^2$$



Use Case:

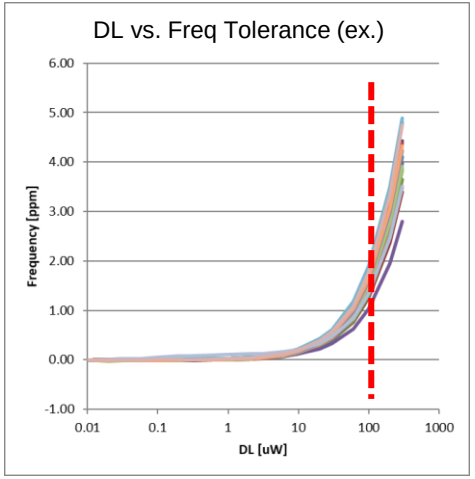
Designer uses the smallest size crystal to save board space. –R is measured to be insufficient.

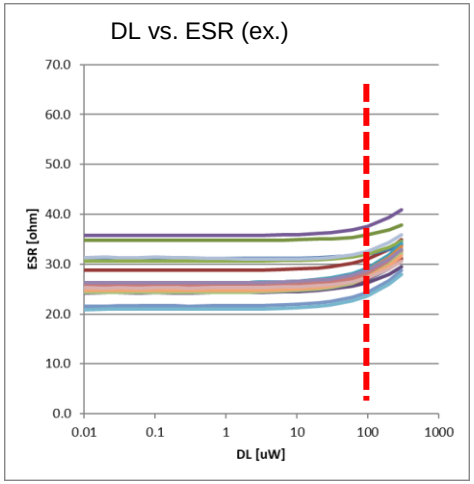
Best Practice:

Honor the ASIC's requirement for ESR, even if a smaller size crystal is needed. Work closely with the crystal supplier about custom requirements and circuit evaluation services.

Drive Level (DL)

- **DL refers to the power used to operate the MHz crystal, 1µW to 100µW is typical to maintain stable oscillation**
- **Exceeding DL max specification causes adverse affect to frequency tolerance, ESR and other performance parameters**
- **Excessive DL, >1mW, may cause irreversible damage due to breakage**





Use Case:

Designer wants increased DL to improve oscillator phase noise or startup time. Too much and the opposite occurs…

Best Practice:

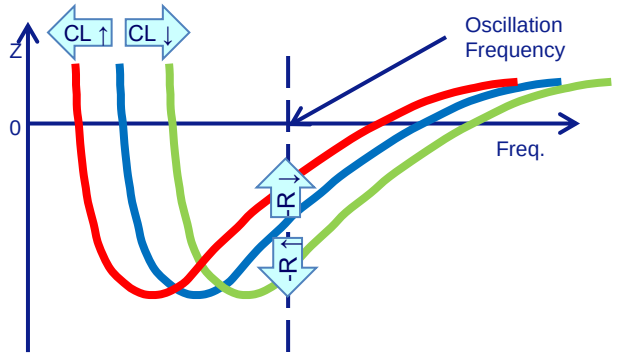
Honor ASIC's requirement for DL. Check with supplier for extra margin and perform measurement.

CL Tradeoffs and Cg/Cd Design Criteria

OSC characteristics vs CL

CL Value	Smaller	Larger
Negative Resistance	Larger	Smaller
Oscillation Allowance	Larger	Smaller
Power Consumption	Smaller	Larger
Drive Level	Smaller	Larger
Frequency Stability	Worse	Better
Start-up Time	Shorter	Longer

Xtal Impedance Characteristics



- CL is determined by the IC designers by the tradeoffs above
  - A higher CL improves the frequency stability, Trim Sensitivity, $S = -\frac{C1}{2(C0+CL)^2} * 10^{-6}, in\ \boldsymbol{ppm/pF}$
  - But negatively impacts the rest of the key performance parameters
- For reliable oscillation, CL should ≈ the capacitance at the Xtal terminals

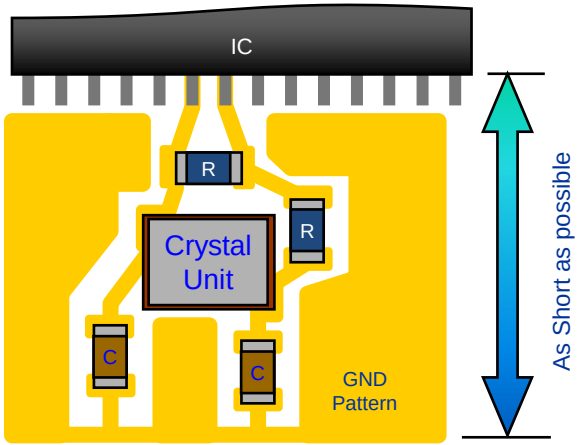
$$CL = \frac{(Cg + Cin) * (Cd + Cout)}{Cg + Cin + Cd + Cout} + \mathrm{Cs}$$

Where: Cin = IC input capacitance, Cout = output capacitance, Cs = PCB parasitic capacitance
If Cin and Cout are not specified, assume a value 3~5 pF

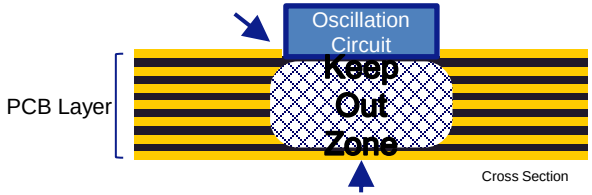
Xtal PCB Layout Guidelines

Layout of external components

- **The Xtal, capacitors and resistors should be placed as close as possible to the IC**
- **The traces should be as short as possible and not cross with any other signal line**
- **A GND shield should be on the same side of the PCB as the IC**
  - Use GND to surround the external components as shown below
  - Using a via to connect an external capacitor to GND increases the total impedance



GND Pattern, signal line and power line should keep out of this area to avoid unstable oscillation and generating noise



If a GND shield is used, the GND layer should be kept far from the oscillation circuit to minimize parasitic capacitance and decreasing the negative resistance