60802 Dynamic Time Sync Error – Monte Carlo Analysis Results for Comparison with Time Series Simulations

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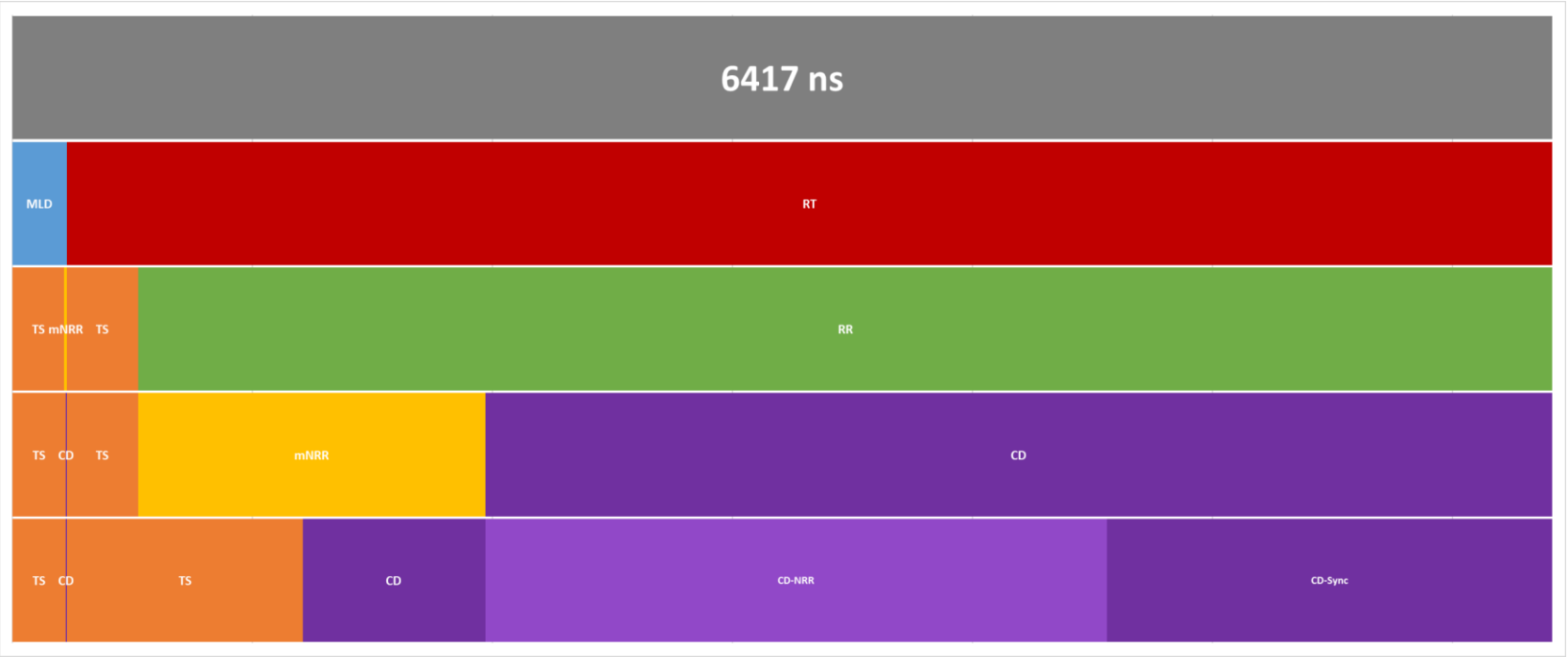
Abstract

- Industrial Automation Systems require microsecond-accurate time across long daisy-chains of devices using IEEE Std. 802.1AS™-2020 as specified by IEEE/IEC 60802.
- Simulated protocol and system parameters have thus far either been judged impractical or have failed to meet the time-accuracy requirement.
- An analysis of how errors accumulate suggested that a Monte Carlo method analysis could support fast iteration of potential scenarios and deliver insights into cause and effect. See...
  - 60802-McCall-et-al-Time-Sync-Error-Model-0921-v03.pdf
  - 60802-McCall-Stanton-Time-Sync-Error-Model-and-Analysis-2021-11-v02.pdf
  - 60802-McCall-Stanton-Time-Sync-Error-Model-and-Analysis-0222-v03.pdf
  - 60802-McCall-Stanton-Time-Sync-Error-Model-and-Analysis-0322-v01.pdf
- In this contribution:
  - Present Monte Carlo analysis results to compare with upcoming Time Series simulation results

Content

- Addition of Error due to Clock Drift during Sync Messaging to Error Breakdown Charts
- Summary of Cases
- Summary of Results
  - Including contribution from different error factors
- Backup – Detailed Results
  - Graphs from Monte Carlo Analysis

Error Breakdown Charts



Input Errors		
GM Clock Drift Max	+1.5	ppm/s
GM Clock Drift Min	-1.5	ppm/s
Clock Drift Max (non-GM)	+1.5	ppm/s
Clock Drift Min (non-GM)	-1.5	ppm/s
Timestamp Granularity TX	4	±ns
Timestamp Granularity RX	4	±ns
Dynamic Time Stamp Error TX	4	±ns
Dynamic Time Stamp Error RX	4	±ns
Input Parameters		
pDelay Interval	250	ms
Sync Interval	125	ms
pDelay Response Time	10	ms
residenceTime	10	ms
Input Correction Factors		
Mean Link Delay Averaging	0	%
NRR Drift Rate Correction	0	%
RR Drift Rate Error Correction	0	%
pDelayResponse → Sync	0	%
mNRR Smoothing N	1	
mNRR Smoothing M	1	
Configuration		
Hops	100	
Runs	1,000,000	

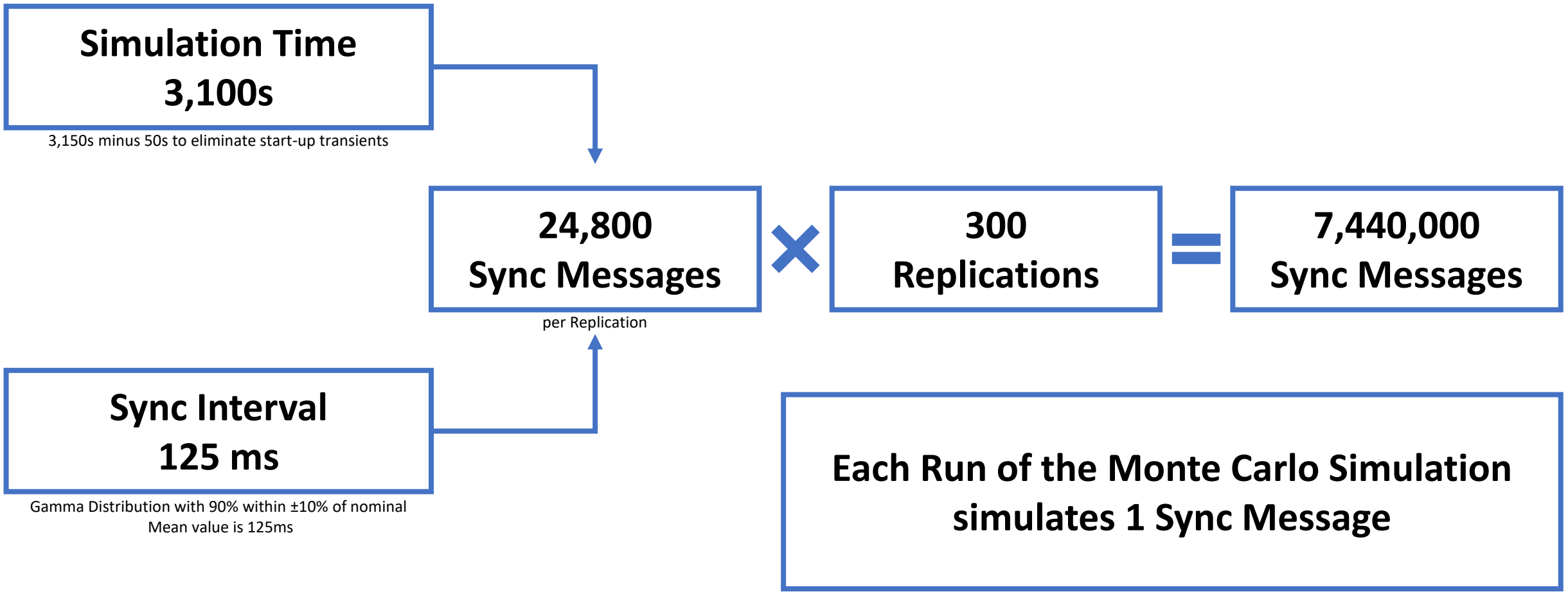
Summary of Cases

Proposed Time Series Simulations – Details

Experiment	Reason	Errors			Parameter			Correction Factors	
		Clock Drift Model – 40°C ↔ +85°C Hold for 1min at Each (Each node's position in cycle distributed at random across 100% of Cycle)	**Timestamp Granularity (ns)**	**Dynamic Timestamp Error (±ns)**	**pDelay Interval (ms)**	**Residence Time (ms)**	**pDelay Turnaround Time (ms)**	**Mean Link Delay Averaging**	**mNRR Smooting Factor N**
A	Baseline with previous assumptions	Ramp Rate 1°C / s (Cycle of 310 s)	8	8	31.25	1	1	Off	1
B	Verify optimised pDelayInterval		8	4	1000	10	10		
C					250	10	10		
D					31.25	10	10		
E	Verify effect of reduced Timestamp Error (reduced DTE when pDelay Interval is low, i.e. 31.25ms)		4	2	31.25	10	10		
F	Verify effect of reduced Clock Drift (reduced DTE when pDelay Interval is high, i.e. 1000ms)	Ramp Rate 0.5°C / s Cycle of 560s	8	4	1000	10	10		

Timestamp Granularity and Dynamic Timestamp Error are uniform distributions unless otherwise stated
Sync Interval: 125ms pDelay Interval variation is +0-30% with uniform distribution
Sync Interval variation is ±10% with 90% probability with gamma distribution
Note: 8ns Timestamp Granularity in Time Series Simulation is equivalent to ±4ns Timestamp Granularity Error in Monte Carlo Analysis
1°C / s temperature ramp rate is the equivalent of ±1.5 ppm/s clock drift rate in Monte Carlo Analysis
No difference between base (PHY related) propagation delay for pDelay and Sync messages

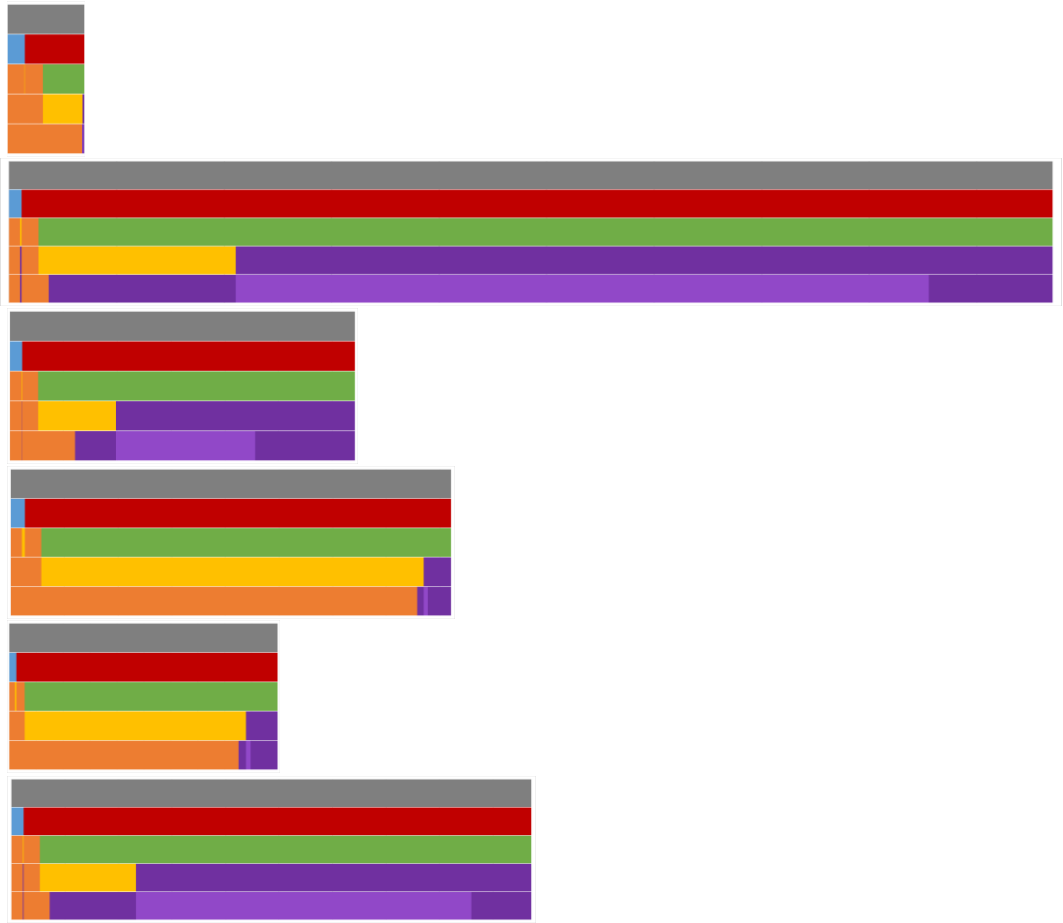
Number of Sync Messages



Summary of Results

Summary of Results - 7σ Charts

Case	Reason	Key Factor	7σ DTE	max|DTE|
A	Baseline with previous assumptions	pDelayInterval 31.25ms; 1ms Residence Time & pDelay Turnaround; 8ns Dyn. Timestamp Error	1460	986
B	Verify optimised pDelayInterval	pDelay Interval 1000ms	19400	12800
C		pDelay Interval 250ms	6420	3980
D		pDelay Interval 31.25ms	8210	5850
E	Verify effect of reduced Timestamp Error	Timestamp Errors halved pDelay Interval 31.25ms	4990	3290
F	Verify effect of reduced Clock Drift	Clock Drift halved pDelay Interval 1000ms	9720	6460



Comparison with Time Series Simulation

See 60802-garner-mult-replic-time-series-simul-resutls-for-comparison-with-monte-carlo-simuls-0322-v01.pdf

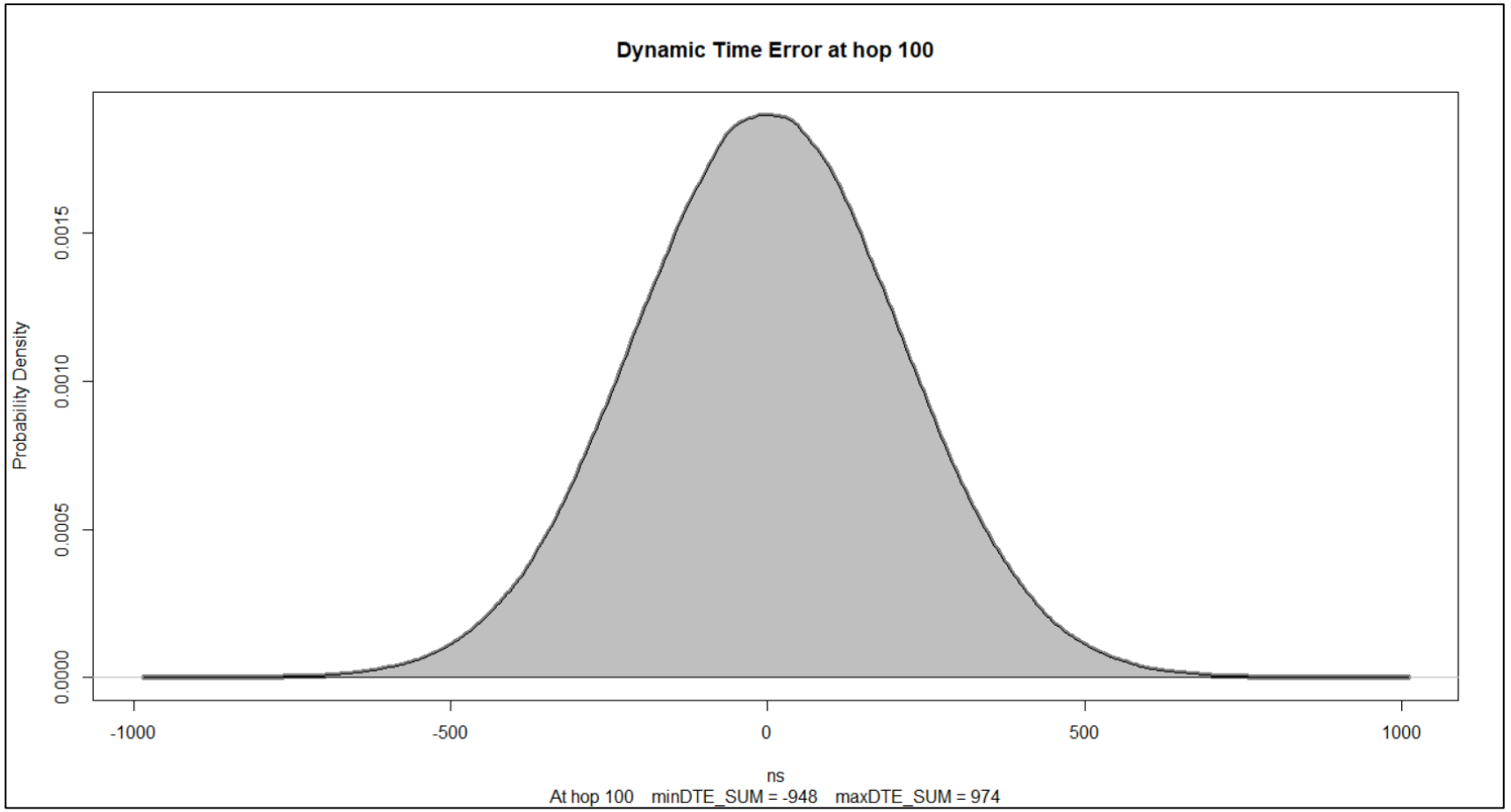
Case	Reason	Key Factor	7σ DTE	max|DTE|	Time Series max|DTE| Filtered	Time Series max|DTE| Unfiltered
A	Baseline with previous assumptions	pDelayInterval 31.25ms; 1ms Residence Time & pDelay Turnaround; 8ns Dyn. Timestamp Error	1460	986	1888	2515
B	Verify optimised pDelayInterval	pDelay Interval 1000ms	19400	12800	15939 (9989 max Confidence Interval)	Odd Data
C		pDelay Interval 250ms	6420	3980	Not Run	Not Run
D		pDelay Interval 31.25ms	8210	5850	6407	7089
E	Verify effect of reduced Timestamp Error	Timestamp Errors halved pDelay Interval 31.25ms	4990	3290	3558	3845
F	Verify effect of reduced Clock Drift	Clock Drift halved pDelay Interval 1000ms	9720	6460	13086 (5240 max Confidence Interval)	Odd Data

Thank you!

Backup Material

Detailed Results

Case A – Baseline



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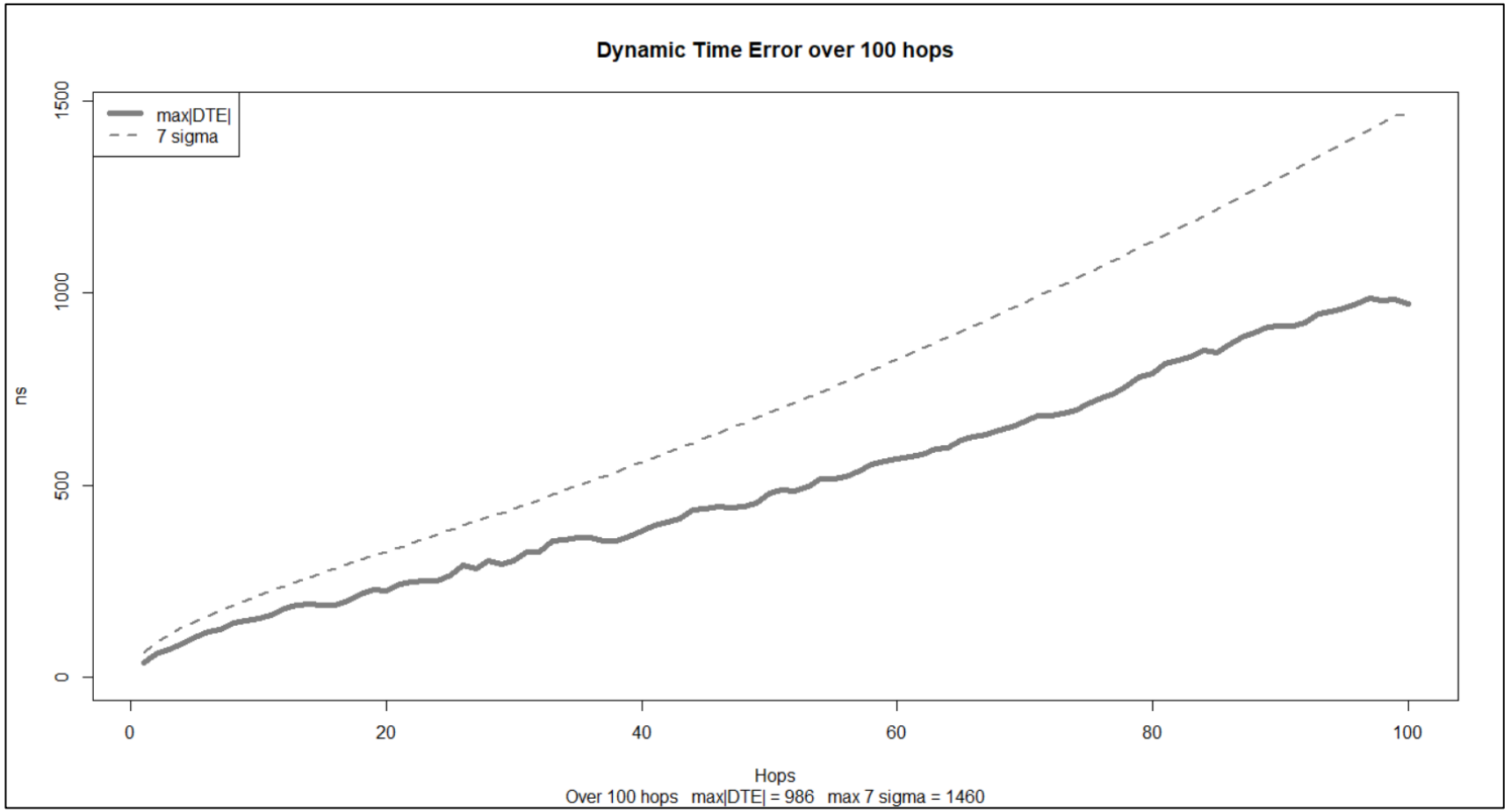
GM Clock Drift Max	+1.5	ppm/s
GM Clock Drift Min	-1.5	ppm/s
Clock Drift Max (non-GM)	+1.5	ppm/s
Clock Drift Min (non-GM)	-1.5	ppm/s
Timestamp Granularity TX	4	±ns
Timestamp Granularity RX	4	±ns
Dynamic Time Stamp Error TX	8	±ns
Dynamic Time Stamp Error RX	8	±ns
Input Parameters		
pDelay Interval	31.25	ms
Sync Interval	125	ms
pDelay Response Time	1	ms
residenceTime	1	ms
Input Correction Factors		
Mean Link Delay Averaging	0	%
NRR Drift Rate Correction	0	%
RR Drift Rate Error Correction	0	%
pDelayResponse → Sync	0	%
mNRR Smoothing N	1	
mNRR Smoothing M	1	
Configuration		
Hops	100	
Runs	1,000,000	

Case A – Baseline



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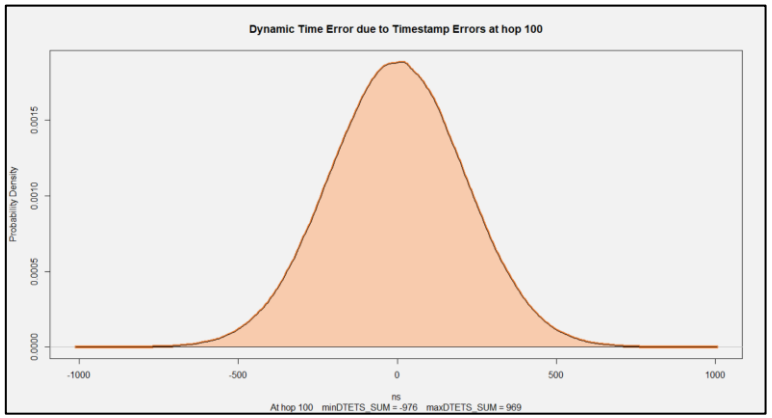

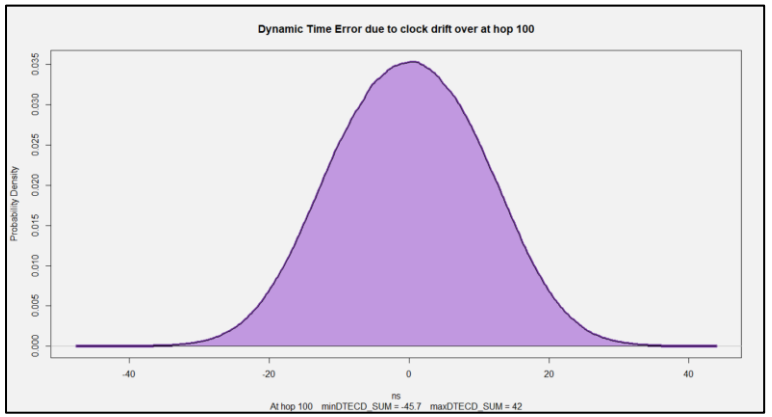

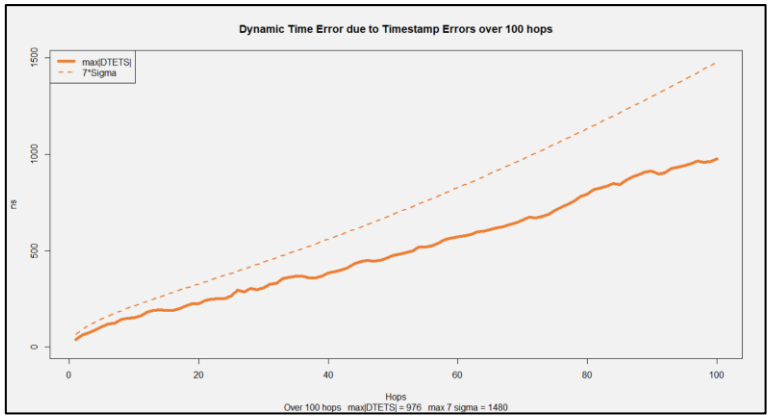

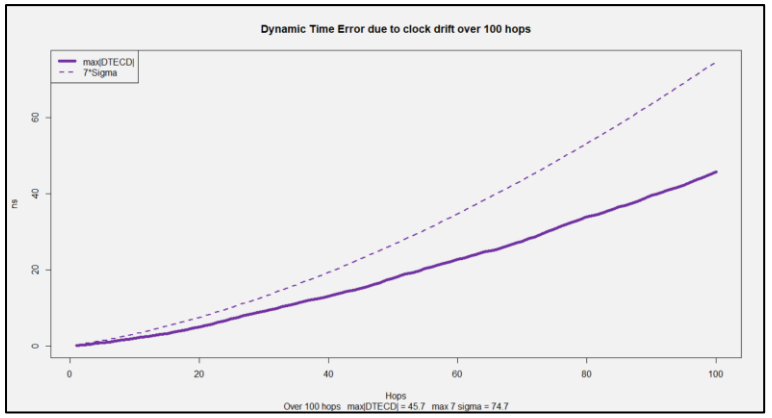

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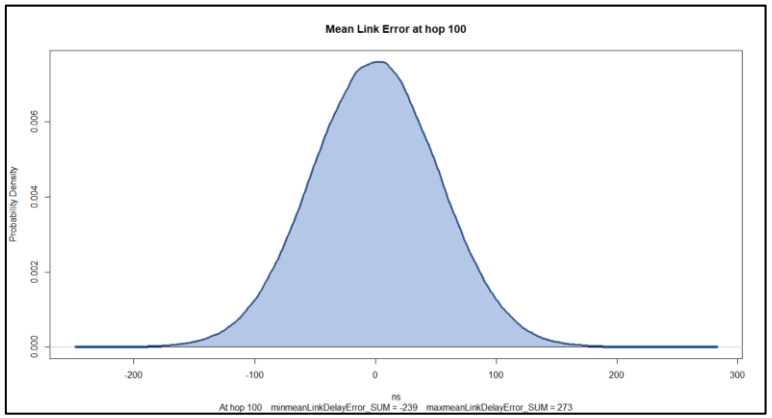
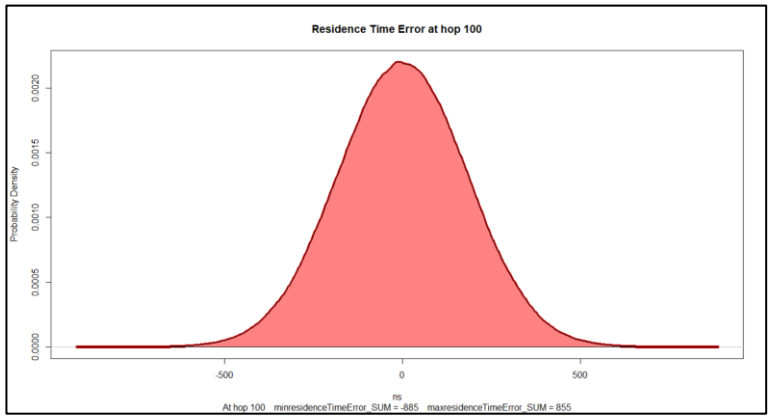
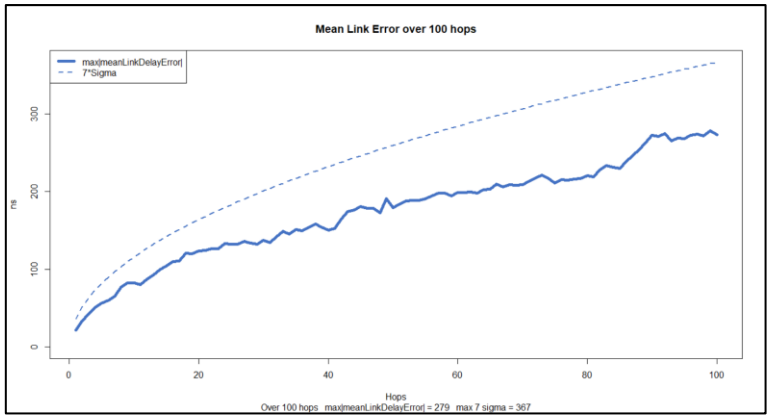
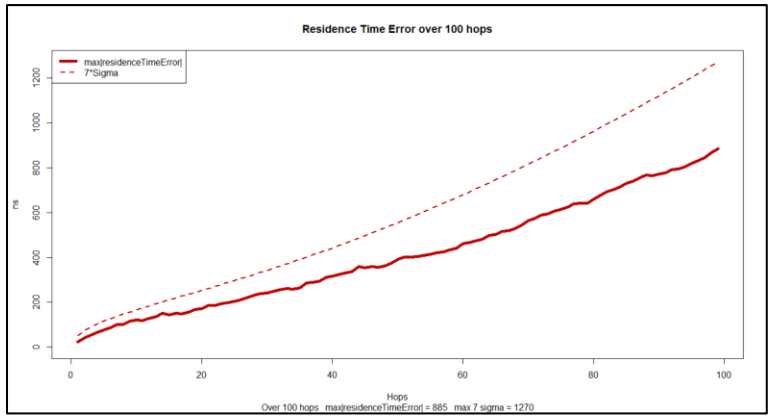
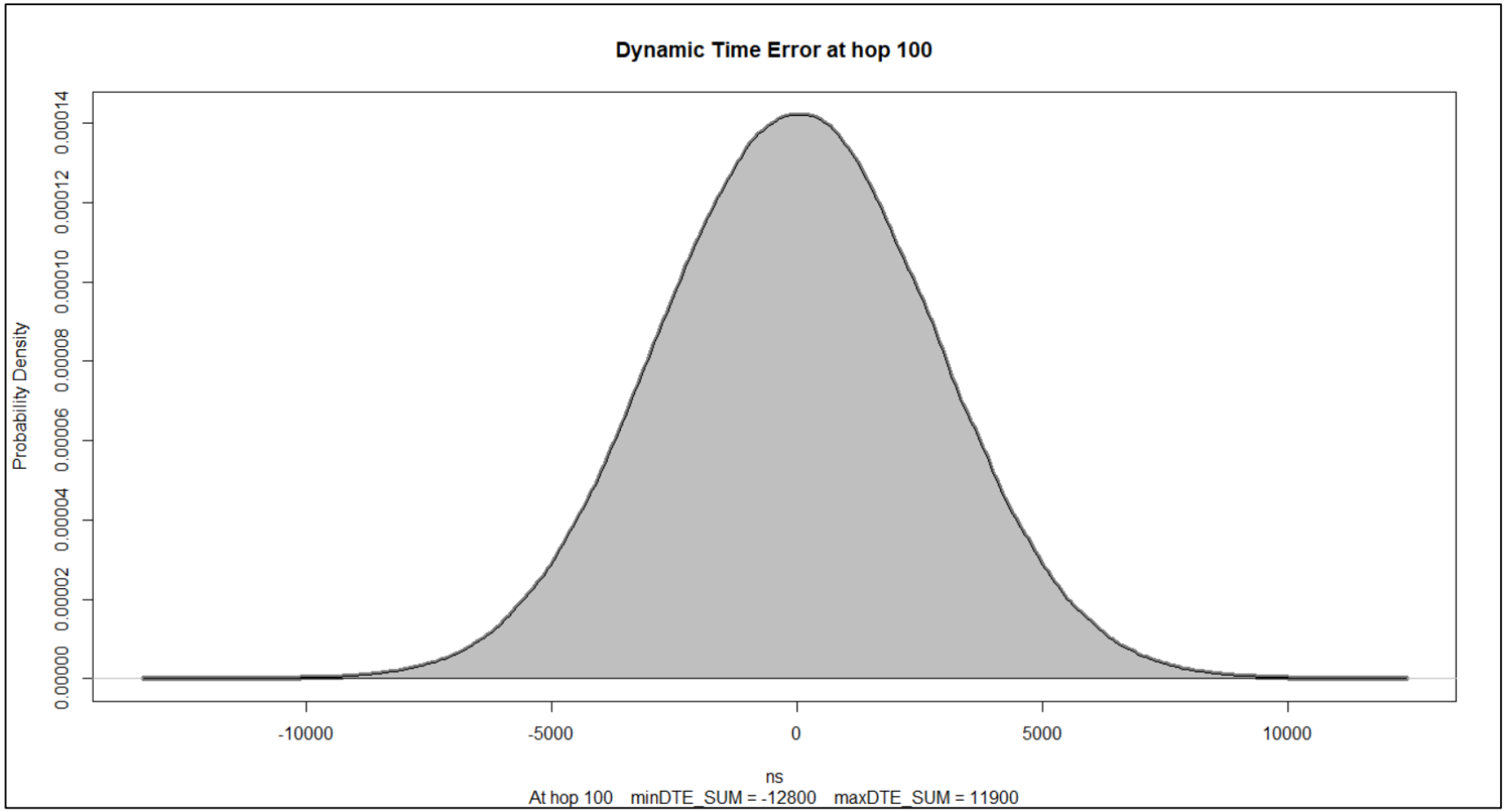








Case B – Optimise pDelay – 1000 ms



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GM Clock Drift Min	-1.5	ppm/s
Clock Drift Max (non-GM)	+1.5	ppm/s
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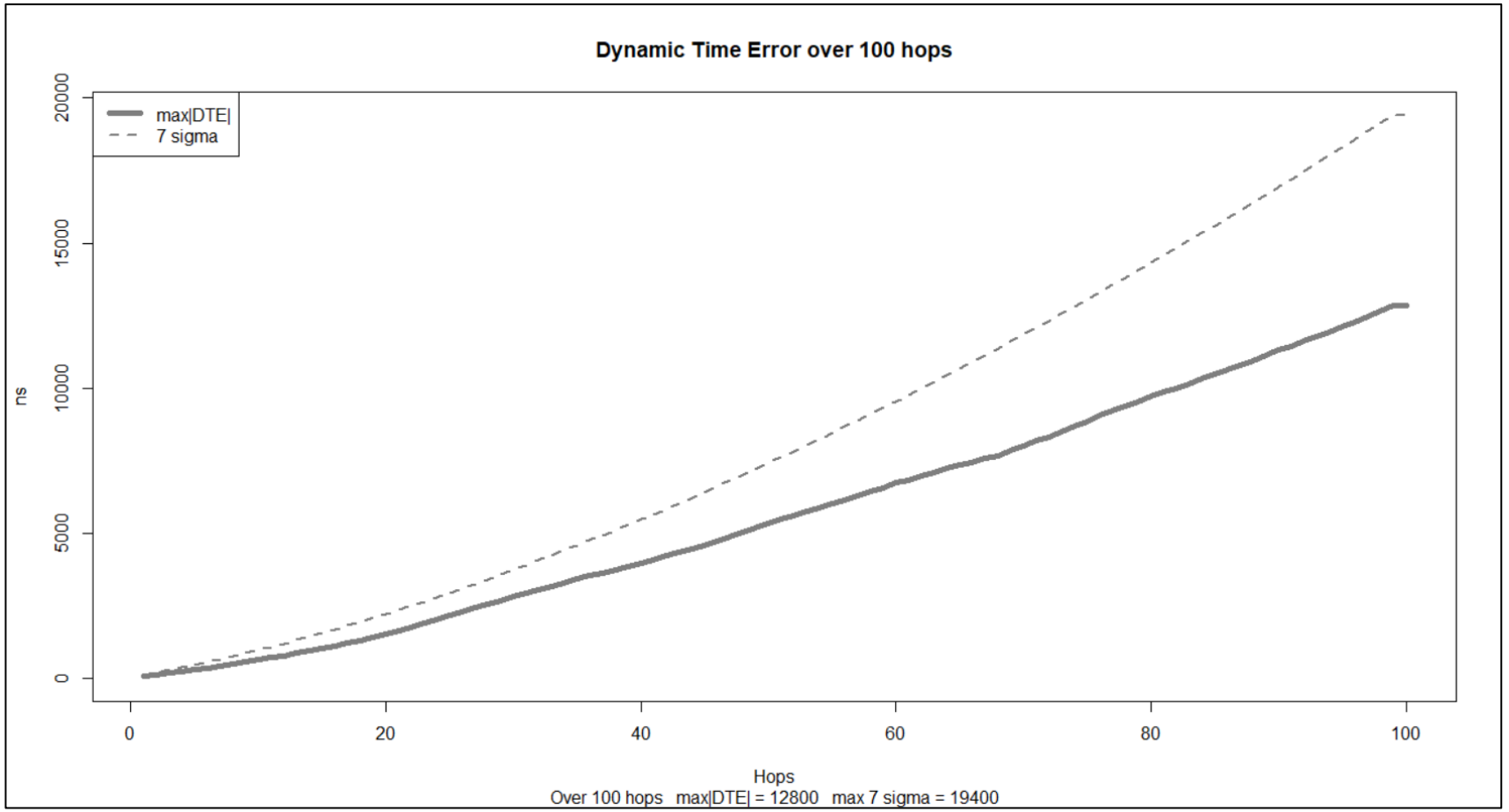
Timestamp Granularity TX	4	±ns
Timestamp Granularity RX	4	±ns
Dynamic Time Stamp Error TX	4	±ns
Dynamic Time Stamp Error RX	4	±ns
Input Parameters		
pDelay Interval	1000	ms
Sync Interval	125	ms
pDelay Response Time	10	ms
residenceTime	10	ms
Input Correction Factors		
Mean Link Delay Averaging	0	%
NRR Drift Rate Correction	0	%
RR Drift Rate Error Correction	0	%
pDelayResponse → Sync	0	%
mNRR Smoothing N	1	
mNRR Smoothing M	1	
Configuration		
Hops	100	
Runs	1,000,000	

Case B – Optimise pDelay – 1000 ms



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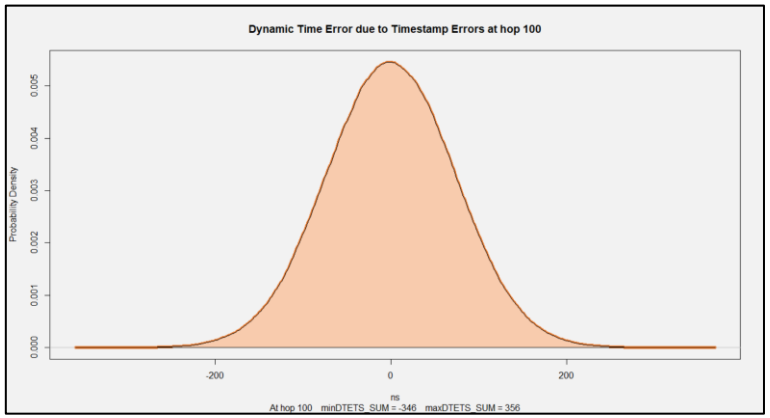

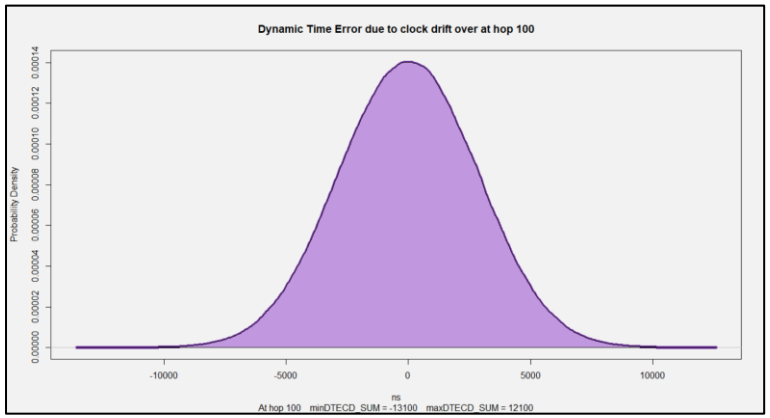

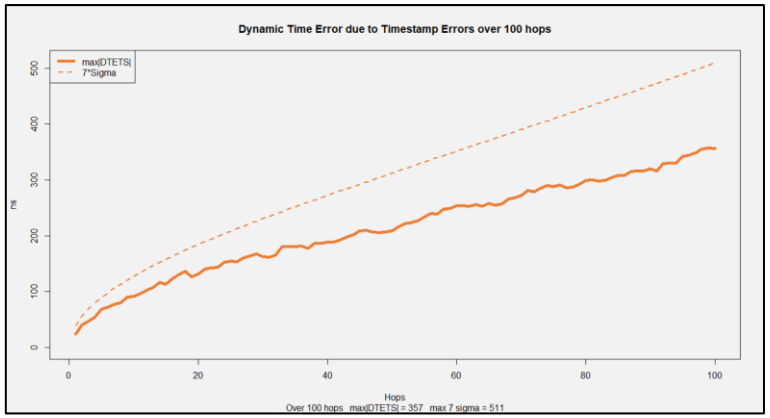

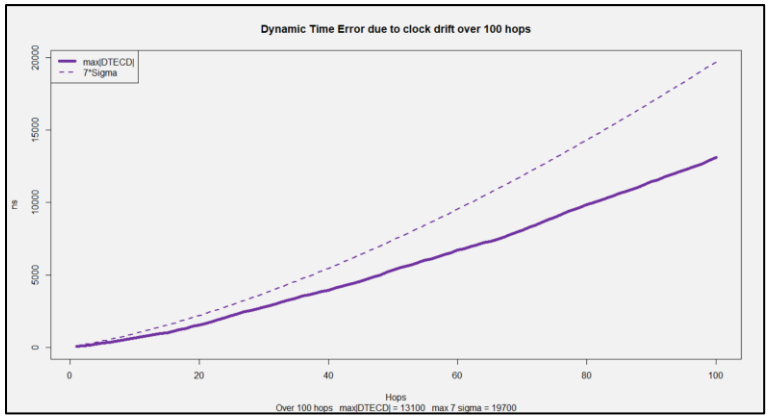

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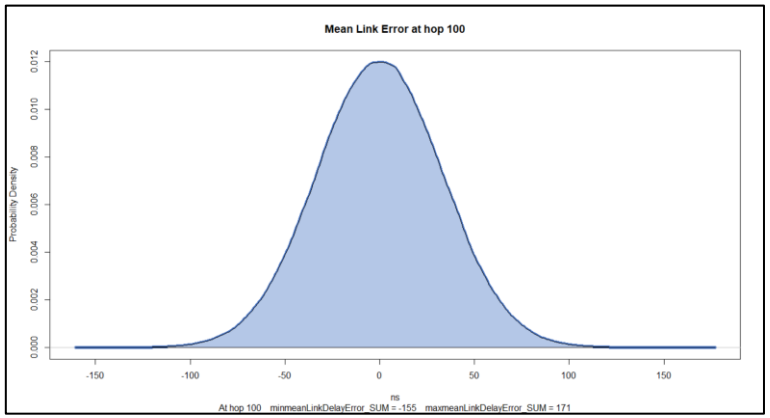
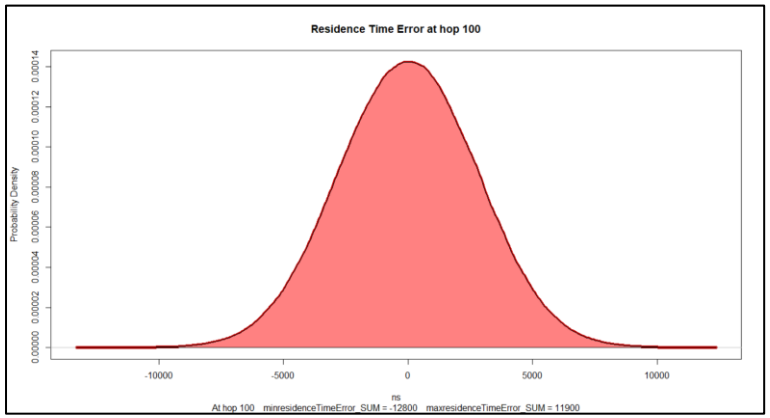
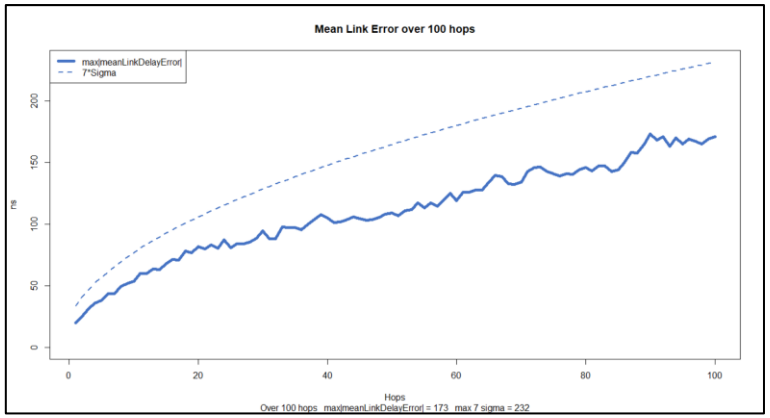
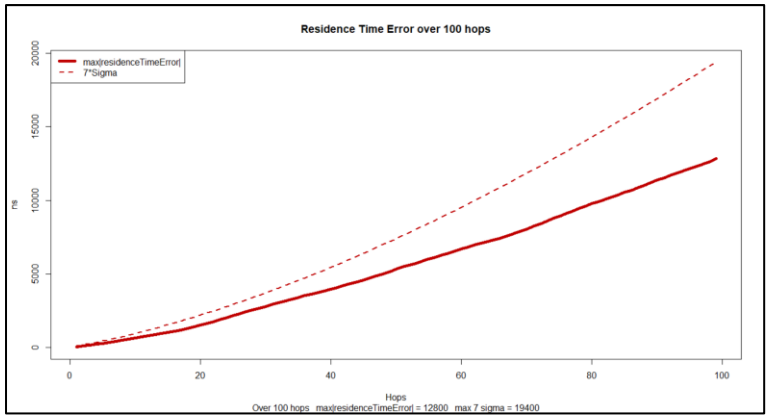
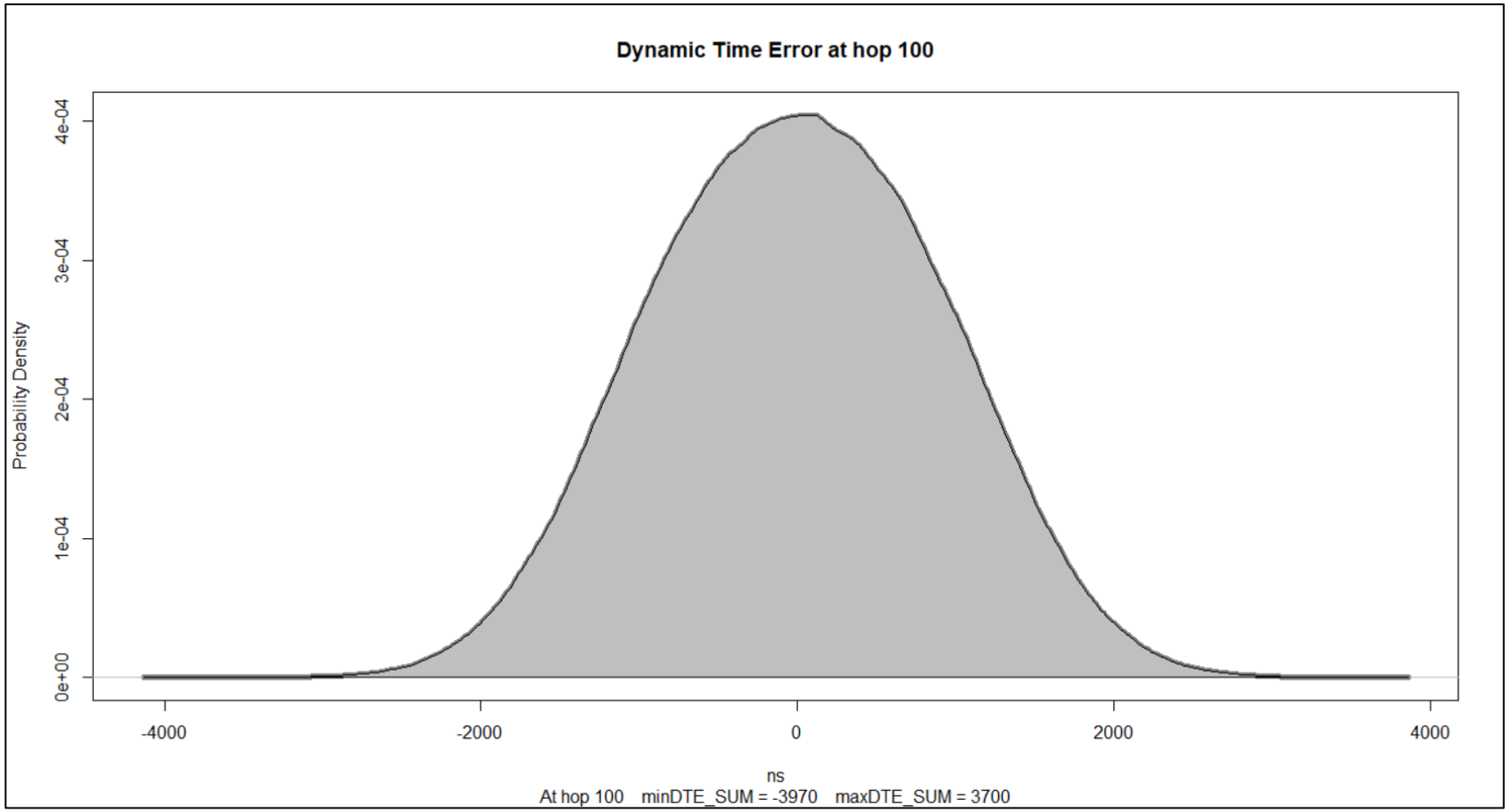








Case C – Optimise pDelay – 250 ms



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Clock Drift Max (non-GM)	+1.5	ppm/s
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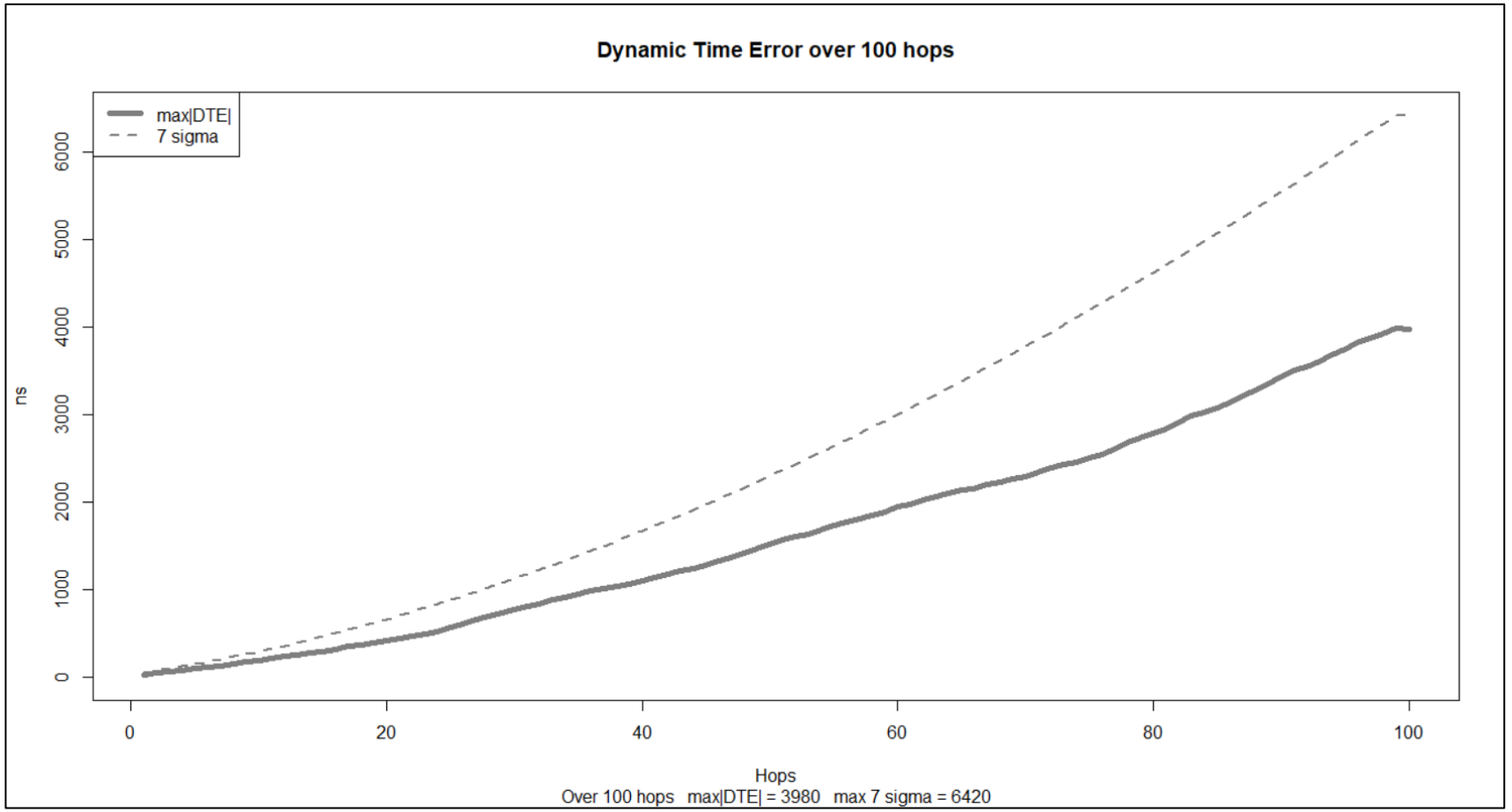
Timestamp Granularity TX	4	±ns
Timestamp Granularity RX	4	±ns
Dynamic Time Stamp Error TX	4	±ns
Dynamic Time Stamp Error RX	4	±ns
Input Parameters		
pDelay Interval	250	ms
Sync Interval	125	ms
pDelay Response Time	10	ms
residenceTime	10	ms
Input Correction Factors		
Mean Link Delay Averaging	0	%
NRR Drift Rate Correction	0	%
RR Drift Rate Error Correction	0	%
pDelayResponse → Sync	0	%
mNRR Smoothing N	1	
mNRR Smoothing M	1	
Configuration		
Hops	100	
Runs	1,000,000	

Case C – Optimise pDelay – 250 ms



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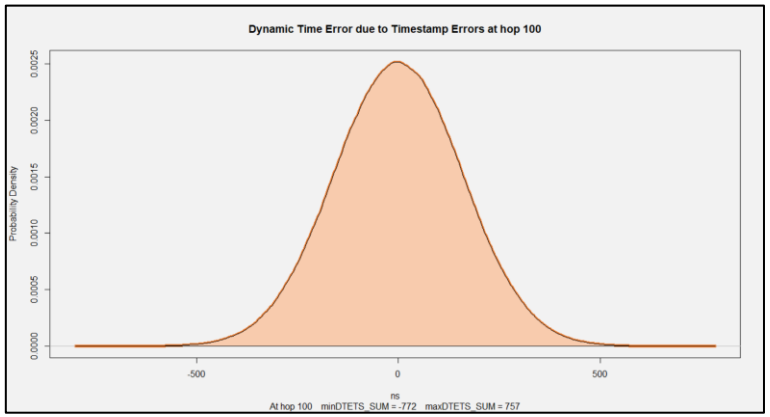

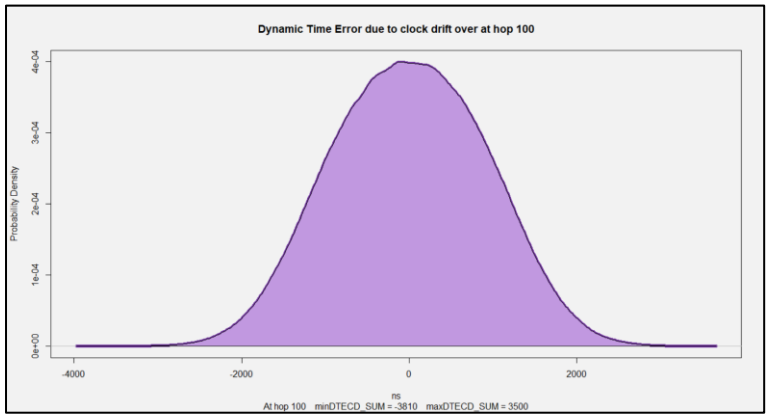

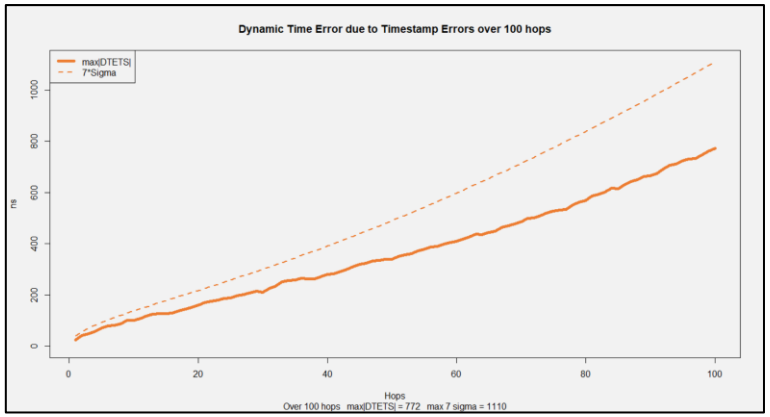

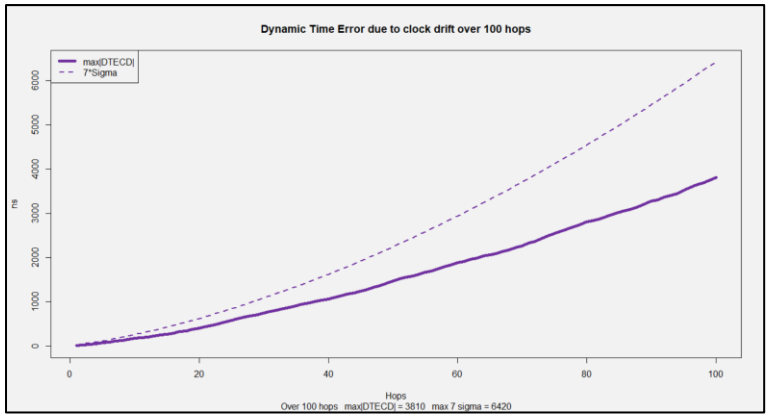

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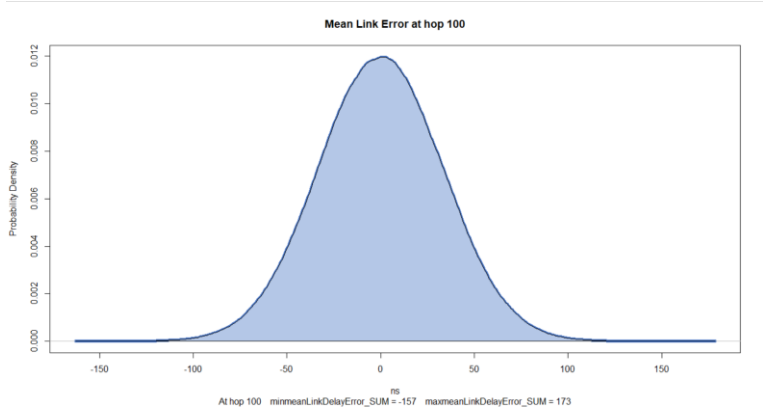
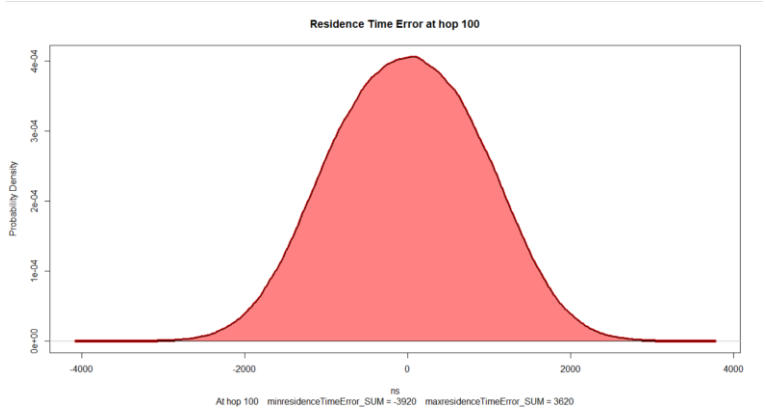
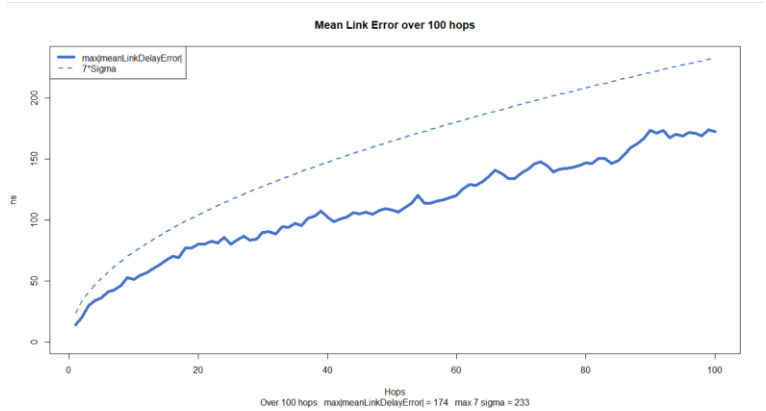
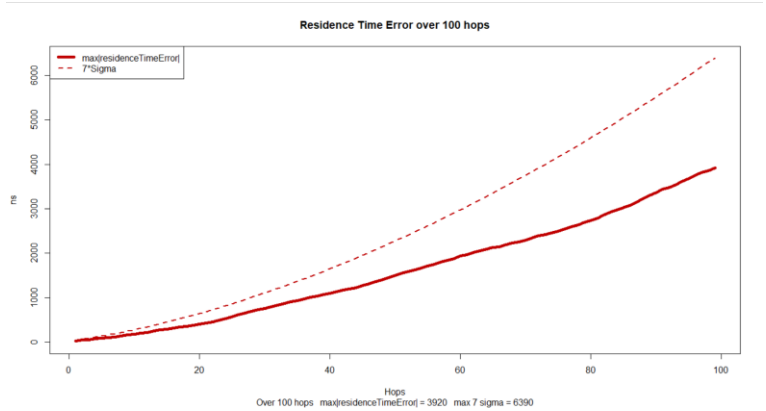
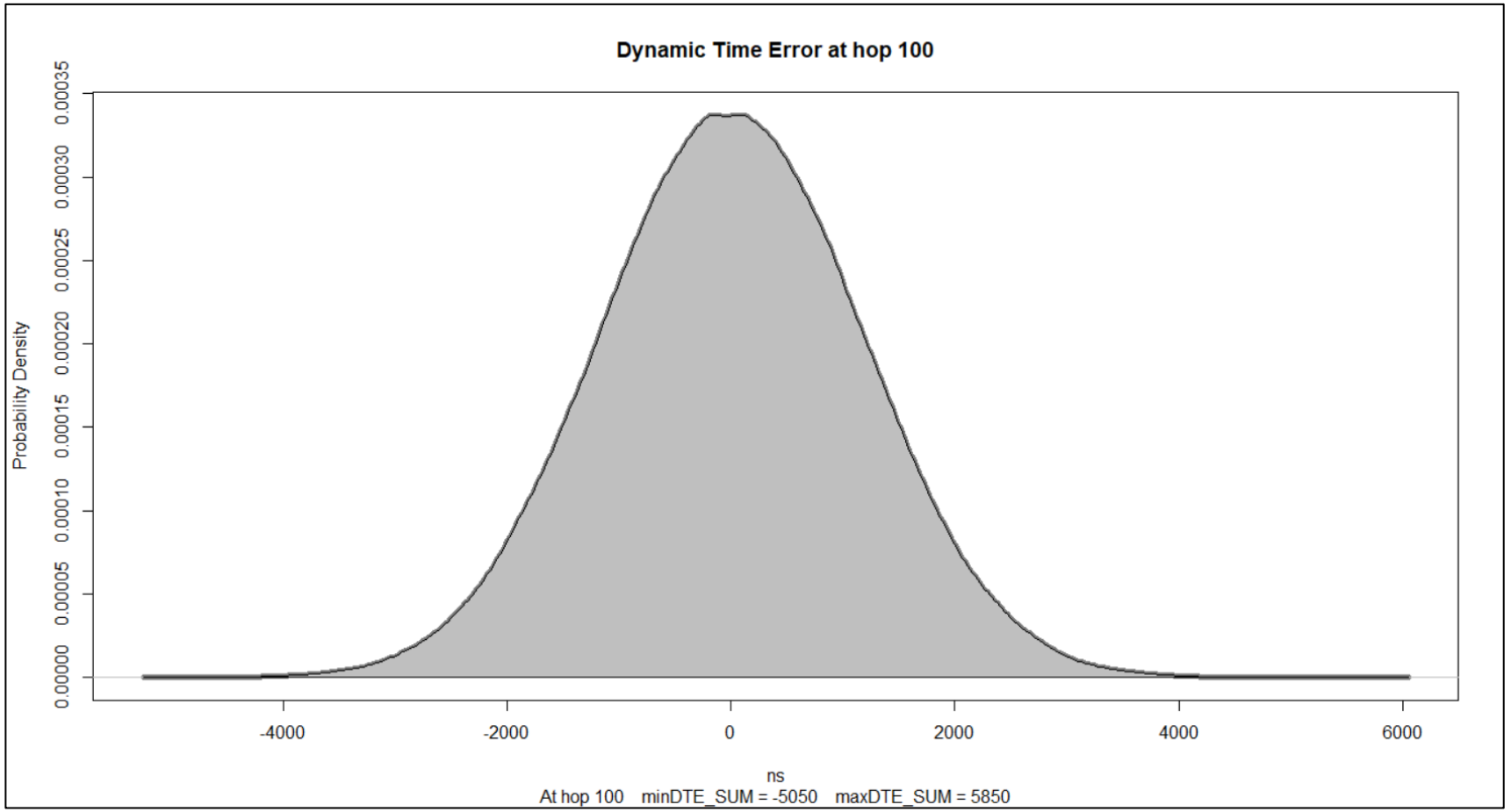








Case D – Optimise pDelay – 31.25 ms



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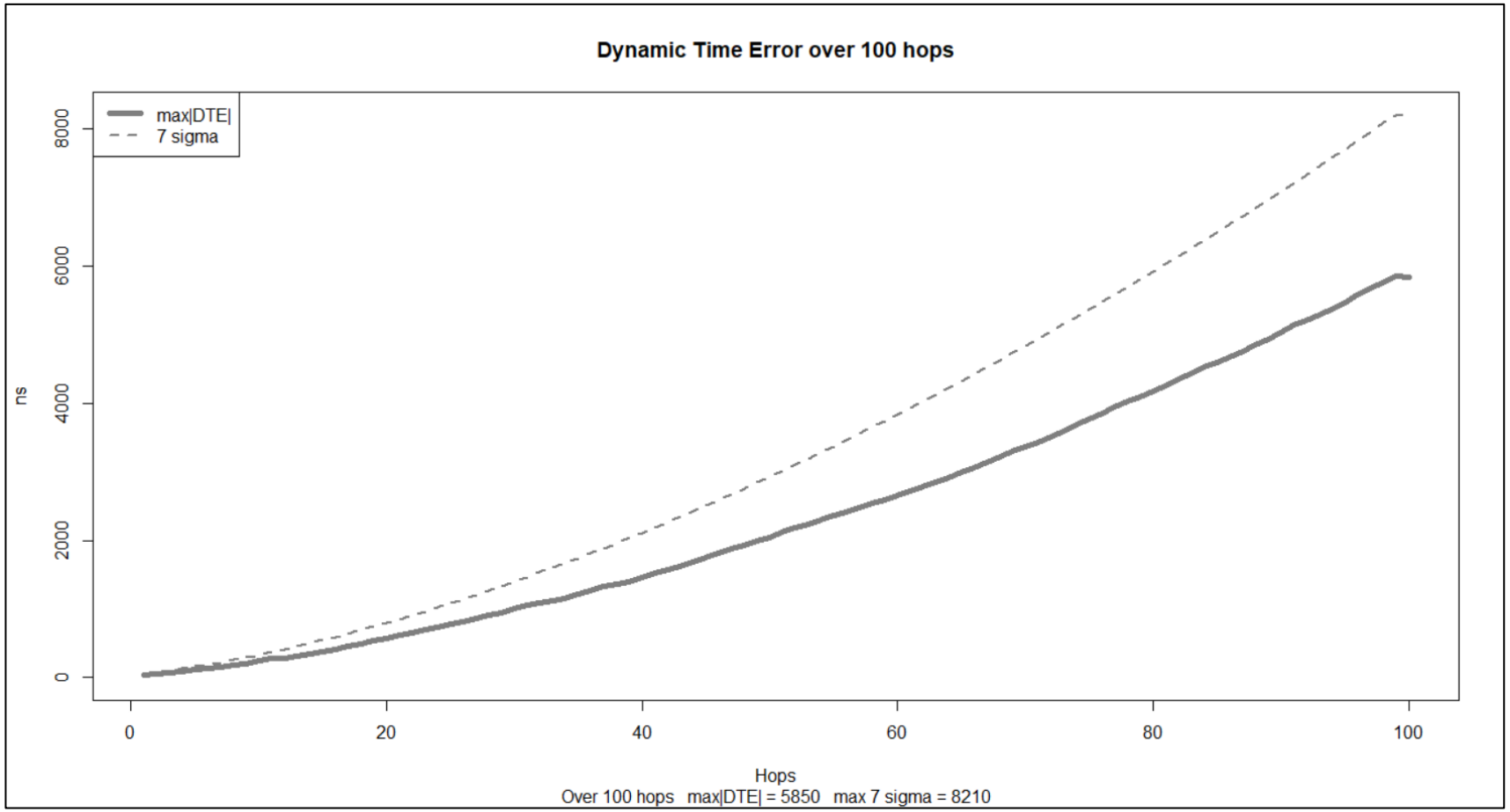
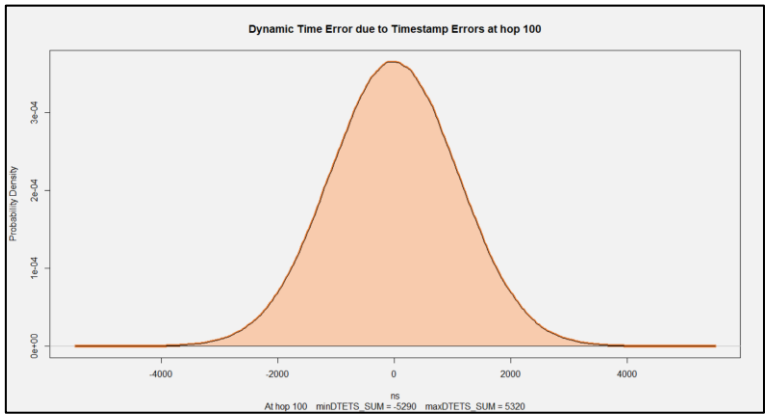
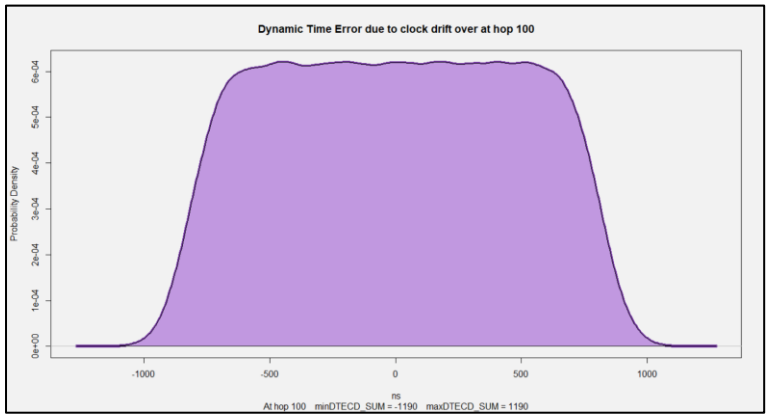
Timestamp Granularity RX	4	±ns
Dynamic Time Stamp Error TX	4	±ns
Dynamic Time Stamp Error RX	4	±ns
Input Parameters		
pDelay Interval	31.25	ms
Sync Interval	125	ms
pDelay Response Time	10	ms
residenceTime	10	ms
Input Correction Factors		
Mean Link Delay Averaging	0	%
NRR Drift Rate Correction	0	%
RR Drift Rate Error Correction	0	%
pDelayResponse → Sync	0	%
mNRR Smoothing N	1	
mNRR Smoothing M	1	
Configuration		
Hops	100	
Runs	1,000,000	

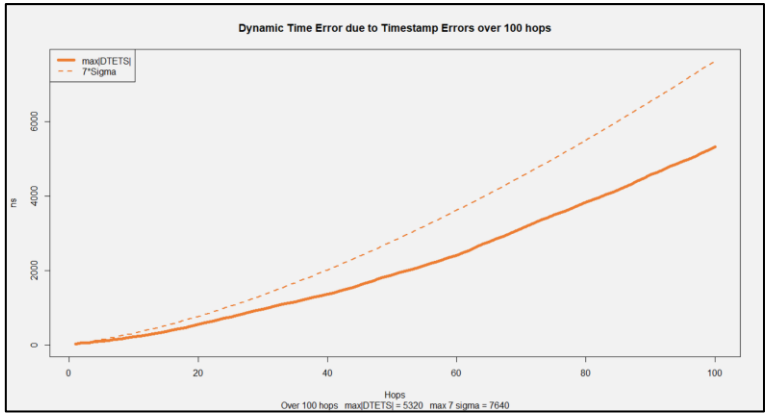
Case D – Optimise pDelay – 31.25 ms

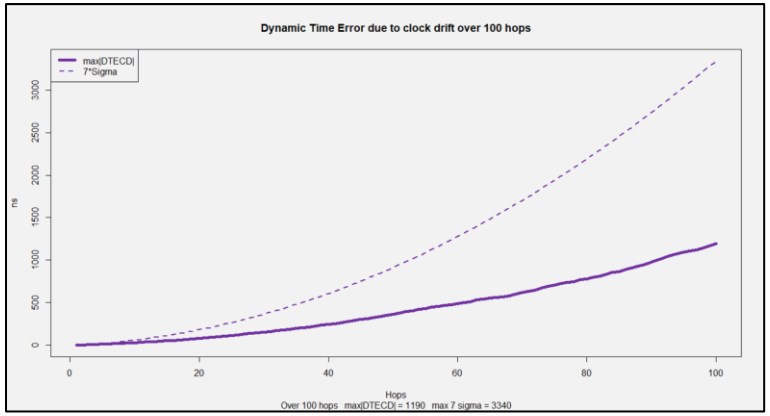


Case D – Optimise pDelay – 31.25 ms

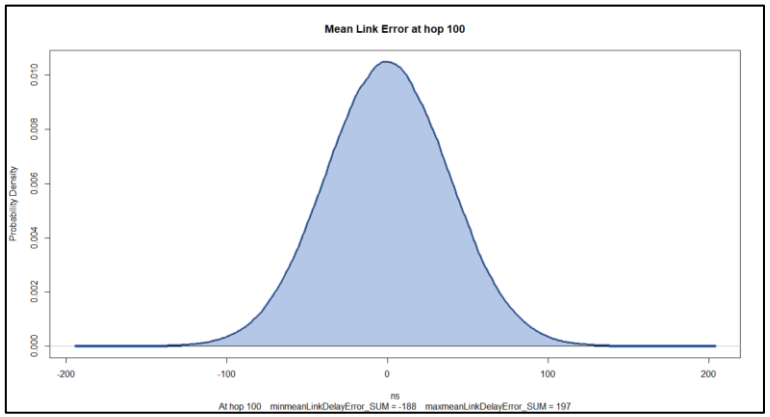


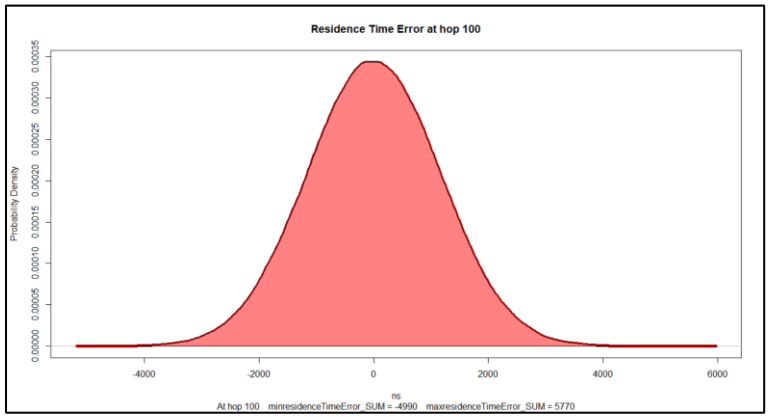


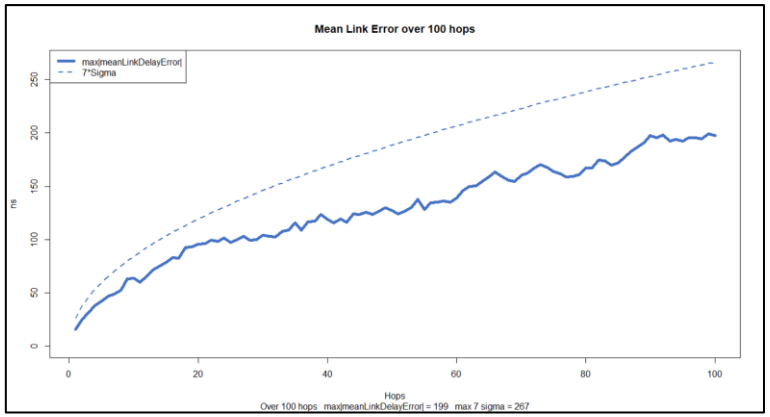


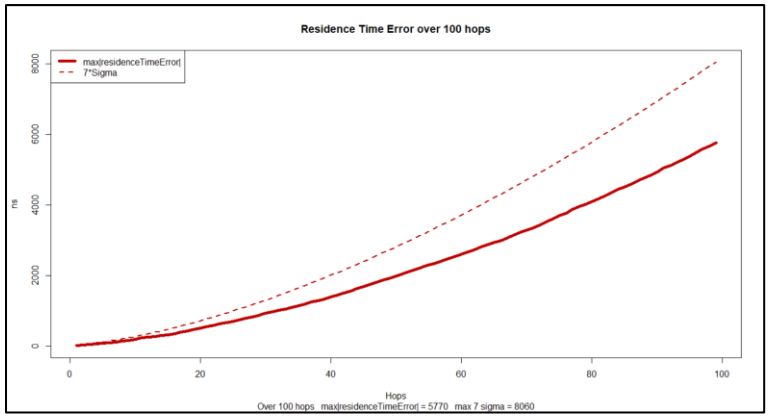


Case D – Optimise pDelay – 31.25 ms



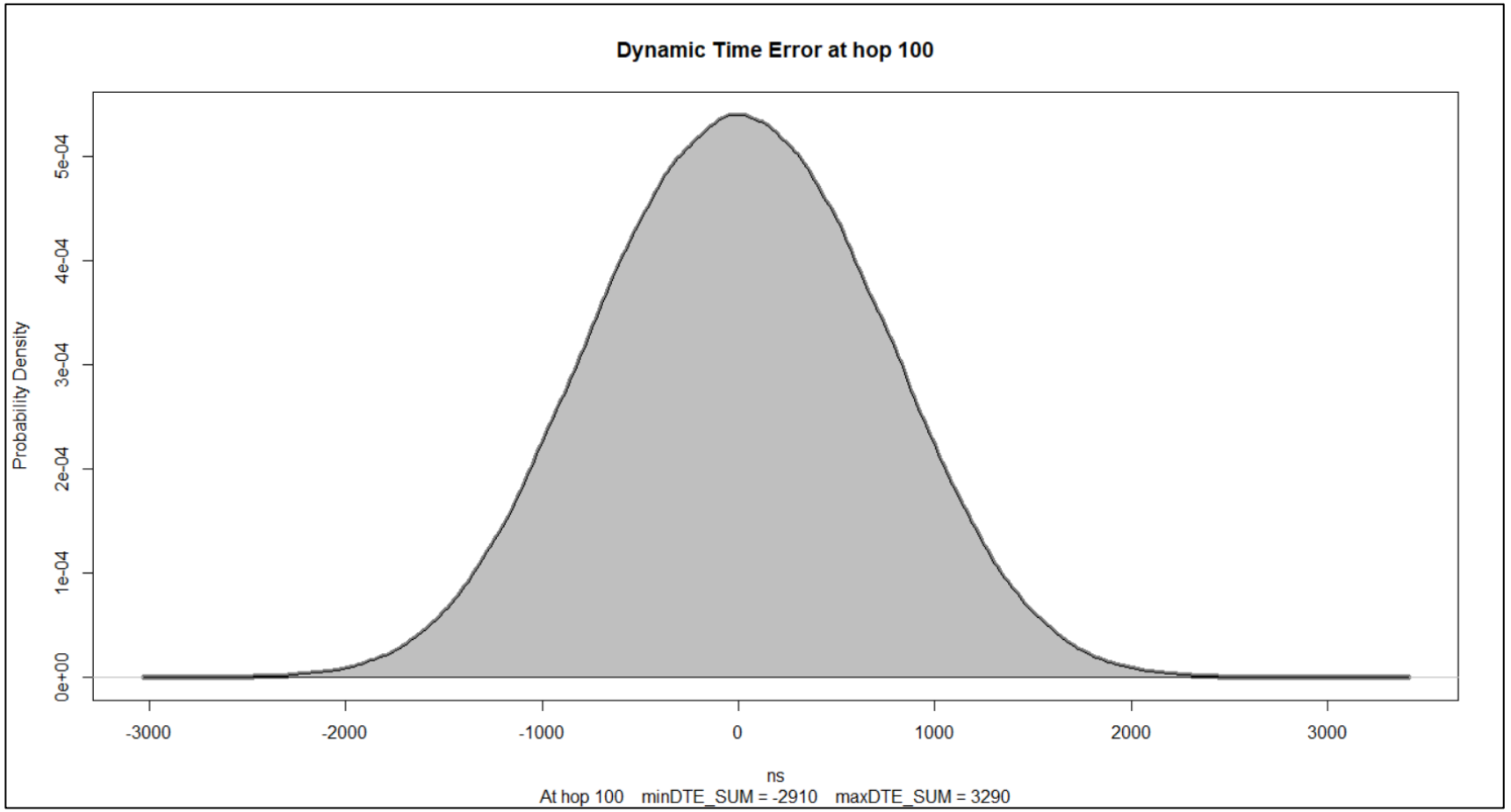






Case E – Timestamp Errors Halved

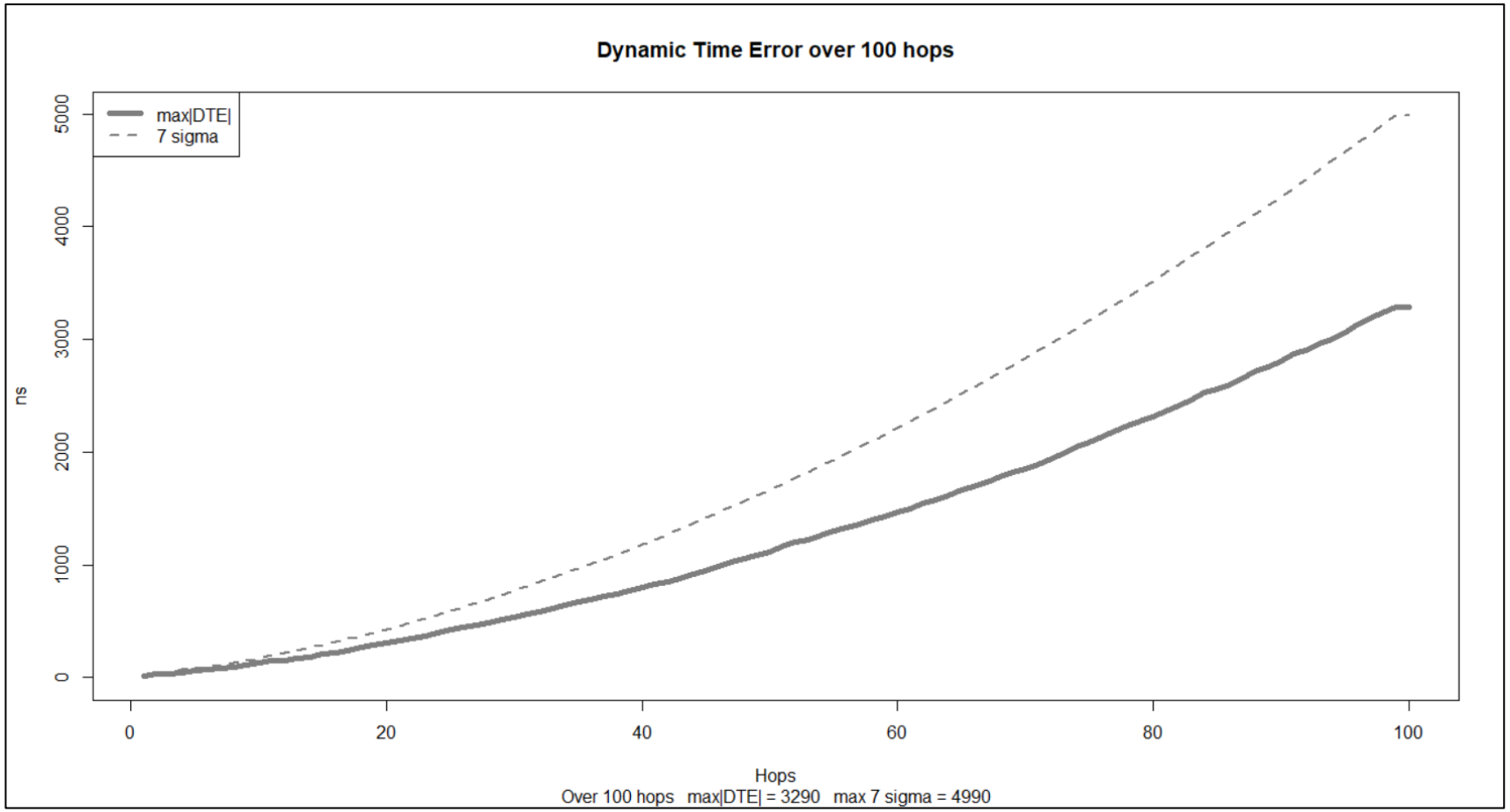
pDelay Interval 31.25ms



Input Errors		
GM Clock Drift Max	+1.5	ppm/s
GM Clock Drift Min	-1.5	ppm/s
Clock Drift Max (non-GM)	+1.5	ppm/s
Clock Drift Min (non-GM)	-1.5	ppm/s
Timestamp Granularity TX	2	±ns
Timestamp Granularity RX	2	±ns
Dynamic Time Stamp Error TX	2	±ns
Dynamic Time Stamp Error RX	2	±ns
Input Parameters		
pDelay Interval	31.25	ms
Sync Interval	125	ms
pDelay Response Time	10	ms
residenceTime	10	ms
Input Correction Factors		
Mean Link Delay Averaging	0	%
NRR Drift Rate Correction	0	%
RR Drift Rate Error Correction	0	%
pDelayResponse → Sync	0	%
mNRR Smoothing N	1	
mNRR Smoothing M	1	
Configuration		
Hops	100	
Runs	1,000,000	

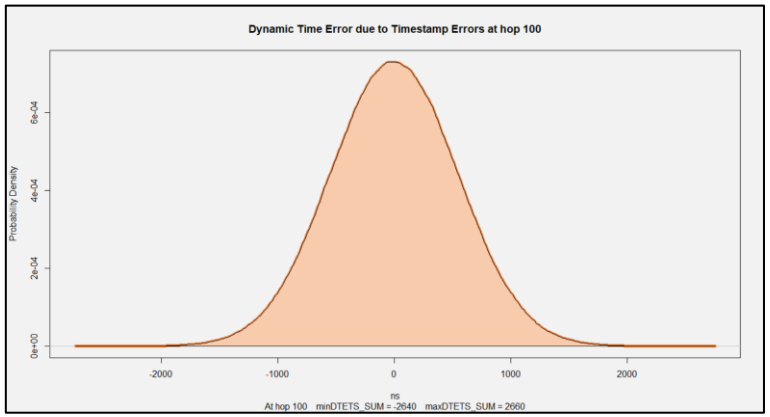
Case E – Timestamp Errors Halved

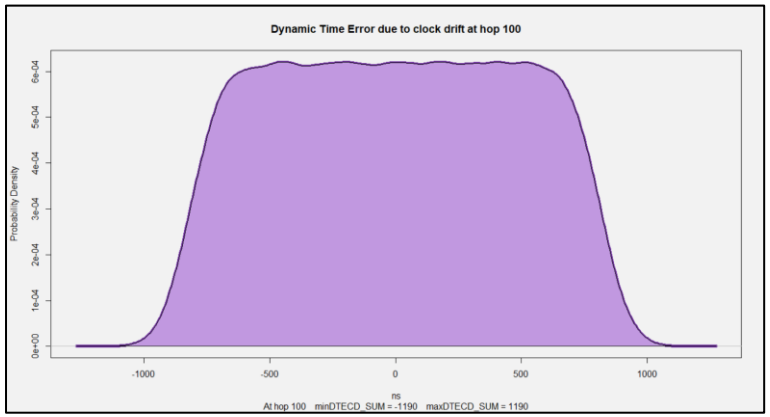
pDelay Interval 31.25ms

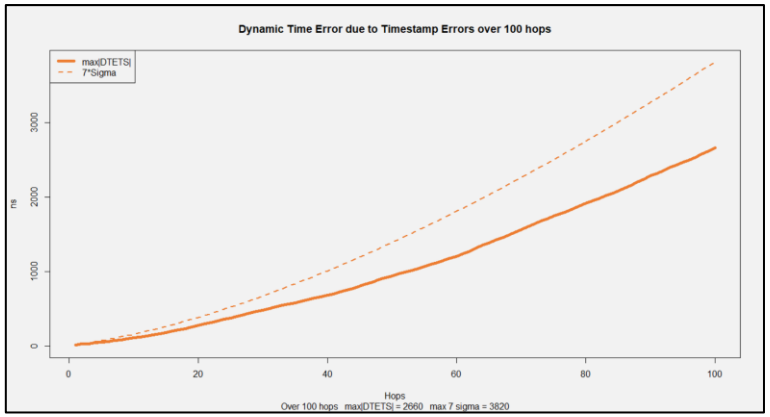


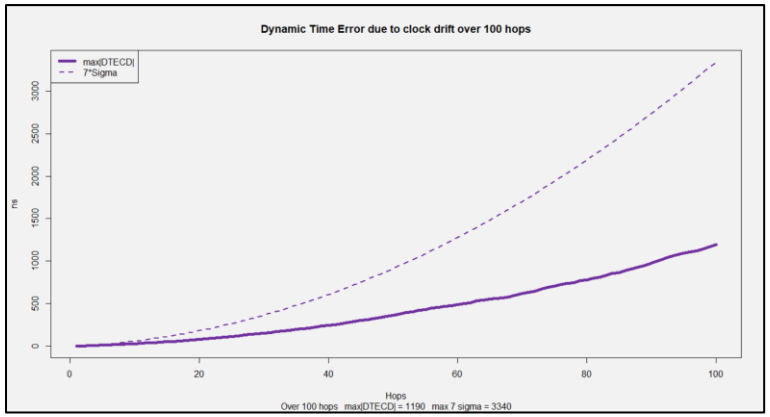
Case E – Timestamp Errors Halved

pDelay Interval 31.25ms



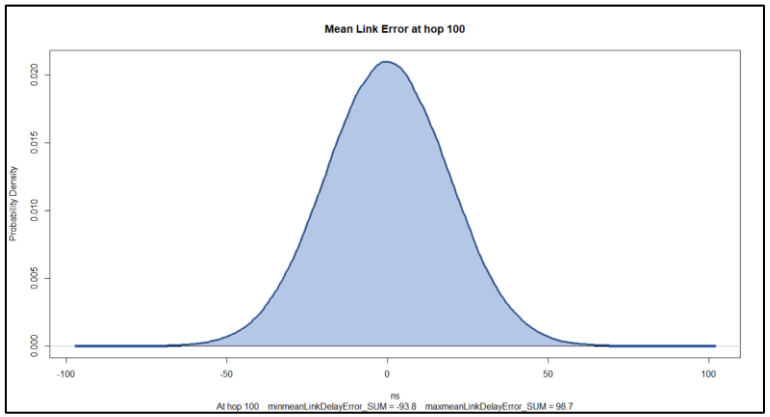


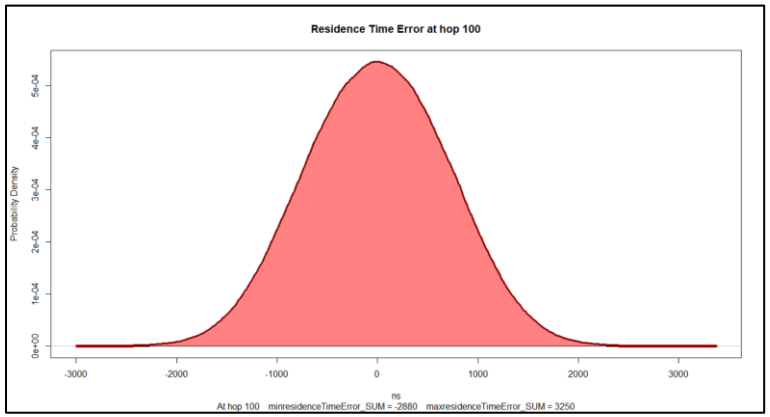


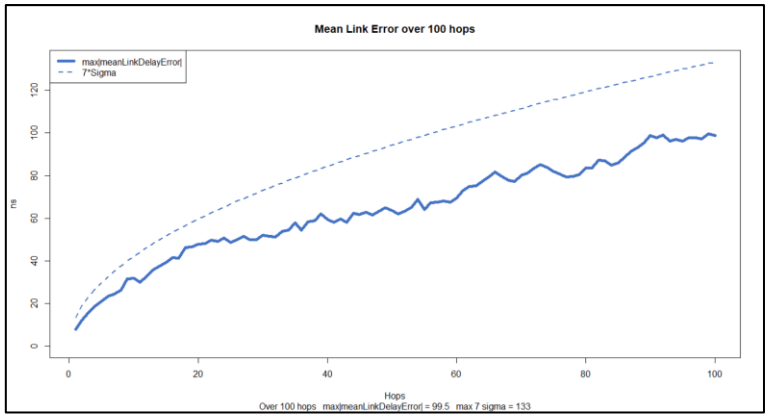


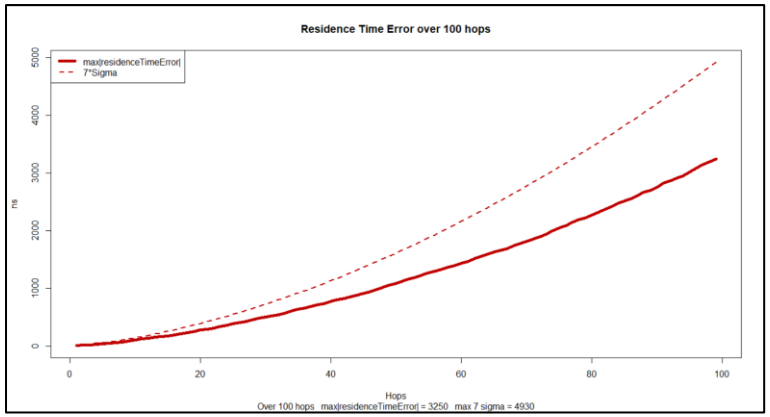
Case E – Timestamp Errors Halved

pDelay Interval 31.25ms



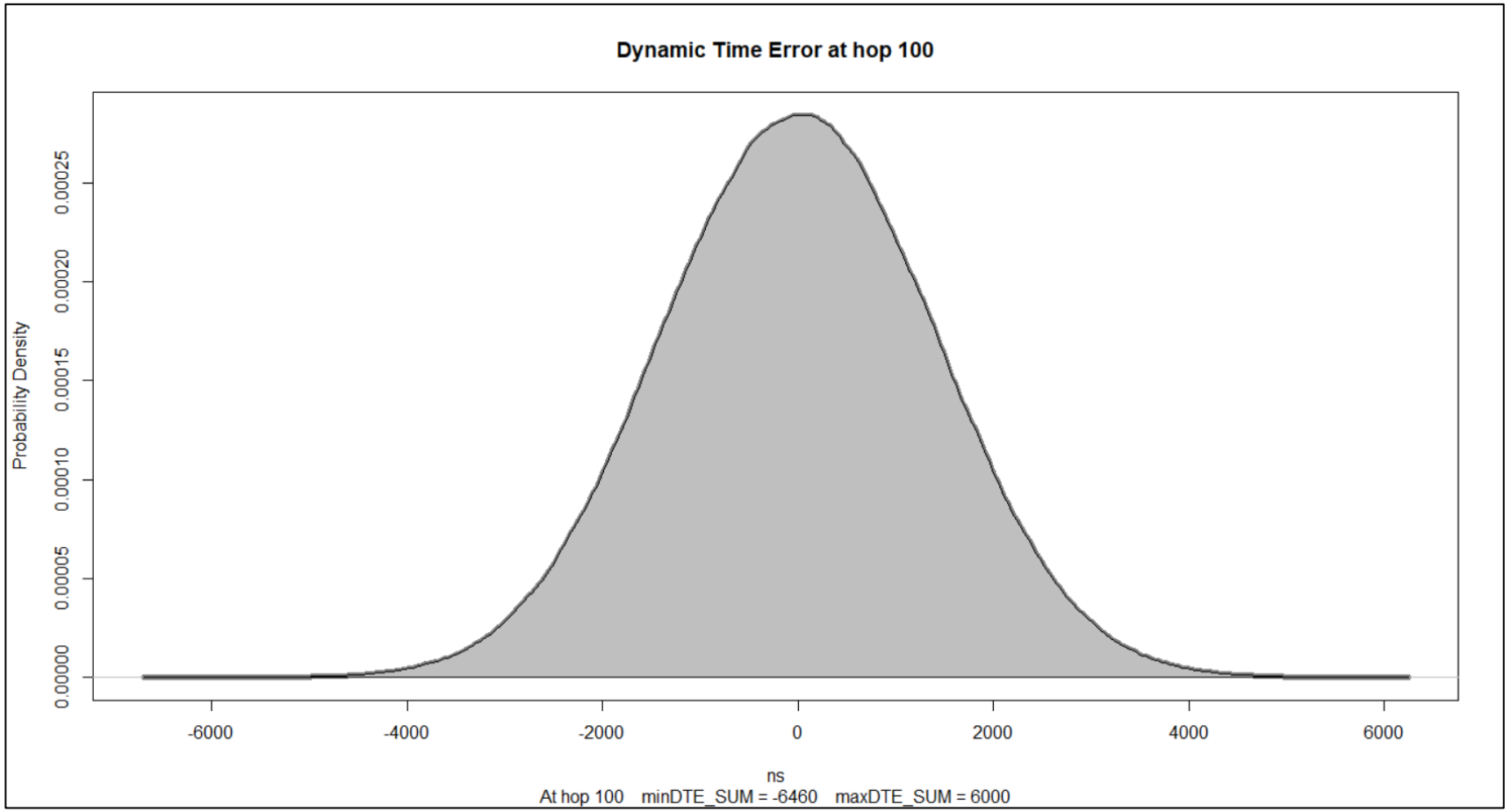






Case F – Clock Drift Halved

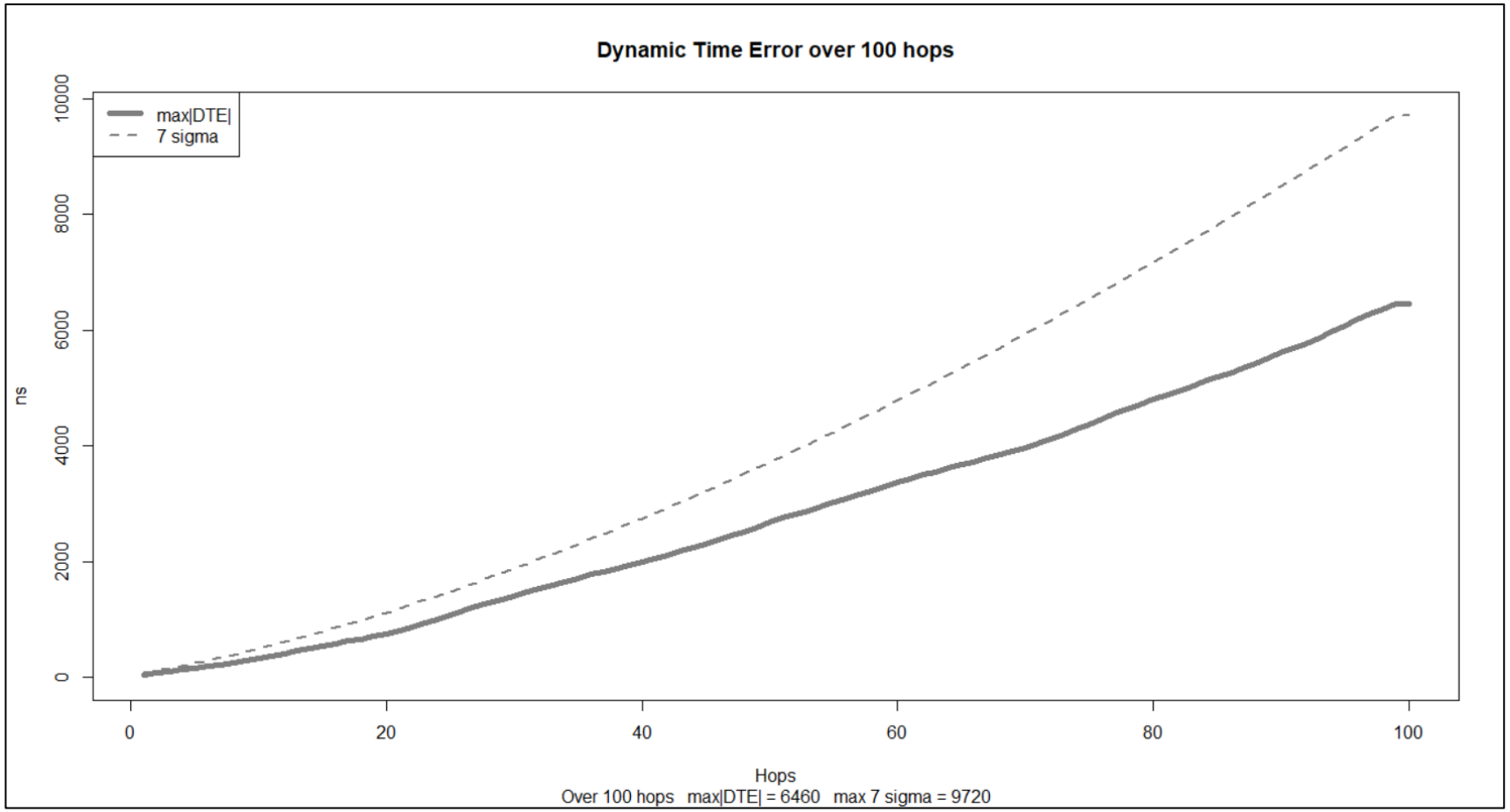
pDelay Interval 1000ms



Input Errors		
GM Clock Drift Max	+0.75	ppm/s
GM Clock Drift Min	-0.75	ppm/s
Clock Drift Max (non-GM)	+0.75	ppm/s
Clock Drift Min (non-GM)	-0.75	ppm/s
Timestamp Granularity TX	4	±ns
Timestamp Granularity RX	4	±ns
Dynamic Time Stamp Error TX	4	±ns
Dynamic Time Stamp Error RX	4	±ns
Input Parameters		
pDelay Interval	1000	ms
Sync Interval	125	ms
pDelay Response Time	10	ms
residenceTime	10	ms
Input Correction Factors		
Mean Link Delay Averaging	0	%
NRR Drift Rate Correction	0	%
RR Drift Rate Error Correction	0	%
pDelayResponse → Sync	0	%
mNRR Smoothing N	1	
mNRR Smoothing M	1	
Configuration		
Hops	100	
Runs	1,000,000	

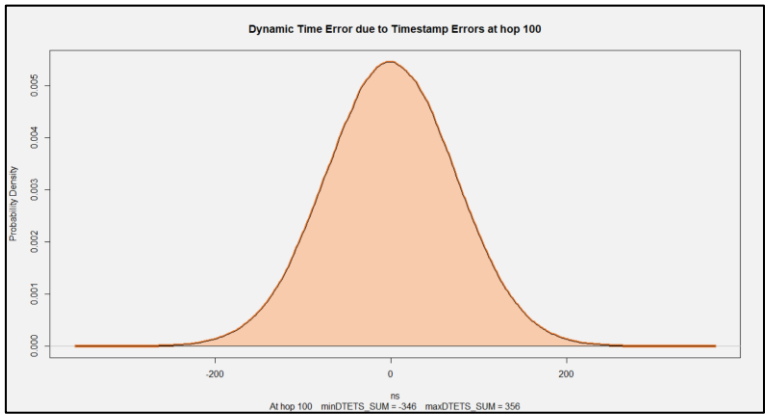
Case F – Clock Drift Halved

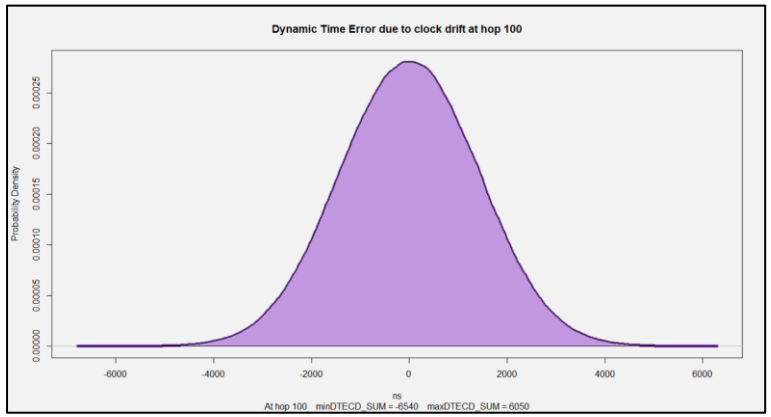
pDelay Interval 1000ms

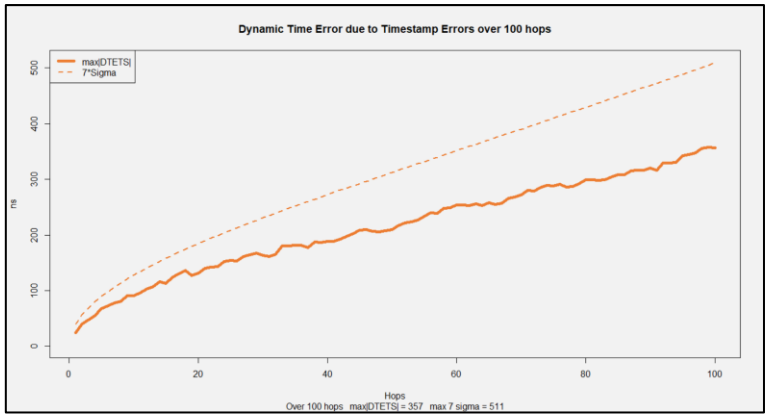


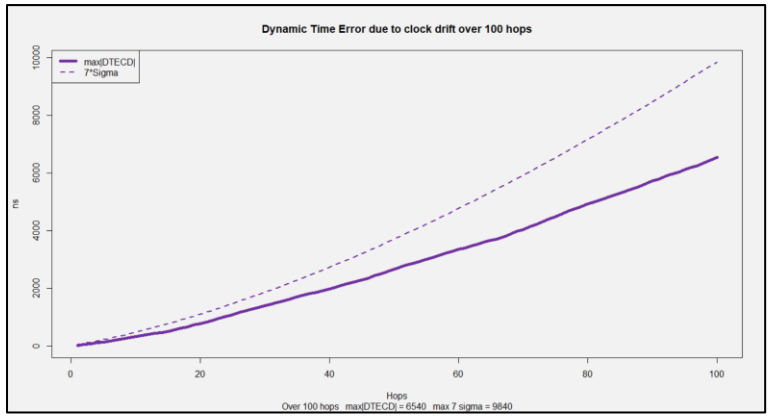
Case F – Clock Drift Halved

pDelay Interval 1000ms









Case F – Clock Drift Halved

pDelay Interval 1000ms