60802 Update on Time Sync

David McCall – Intel Corporation

Version 1

References – 1

- David McCall “60802 Time Sync Ad Hoc 24th October Meeting” https://www.ieee802.org/1/files/public/docs2022/60802-McCall-Time-Sync-Ad-Hoc-Status-Meeting-24-Oct-1022-v1
- David McCall “60802 Time Sync: Reducing dTE – Complexities & Tradeoffs – Ad Hoc Next Steps” https://www.ieee802.org/1/files/public/docs2022/60802-McCall-Time-Sync-Errors-Complexity-Tradeoffs-Ad-Hoc-Next-Steps-0922-v02.pdf
- David “60802 Time Synchronisation – Monte Carlo Analysis: 100-hop Model, “Linear” Clock Drift, NRR Accumulation Overview & Details, Including Equations” https://www.ieee802.org/1/files/public/docs2022/60802-McCall-Monte-Carlo-Multi-Hop-Overview-and-Details-0922-v02.pdf

References – 2

- Dragan Obradovic "ClockSlave PI Controller: Definition and Implementation“ https://www.ieee802.org/1/files/public/docs2022/60802-Obradovic-ClockSlave-1022-v02.pdf
- David McCall "60802 Time Sync Ad Hoc mNRRsmoothing Optimisation Results" https://www.ieee802.org/1/files/public/docs2022/60802-McCall-Time-Sync-mNRRsmoothingN-Optimisation-Results-1122-v1.pdf

References – 3

- Max Turner "Alternative Sync/pDelay Processing" https://www.ieee802.org/1/files/public/docs2022/new-turner-alternateTimeStamping-1022-v01.pdf
- David McCall "60802 Time Sync Ad Hoc mNRRsmoothing Optimisation & Aligning pDelayResp & Sync" https://www.ieee802.org/1/files/public/docs2022/60802-McCall-Time-Sync-mNRRsmoothingN-Optimisation-1022-v1.pdf

References – 4

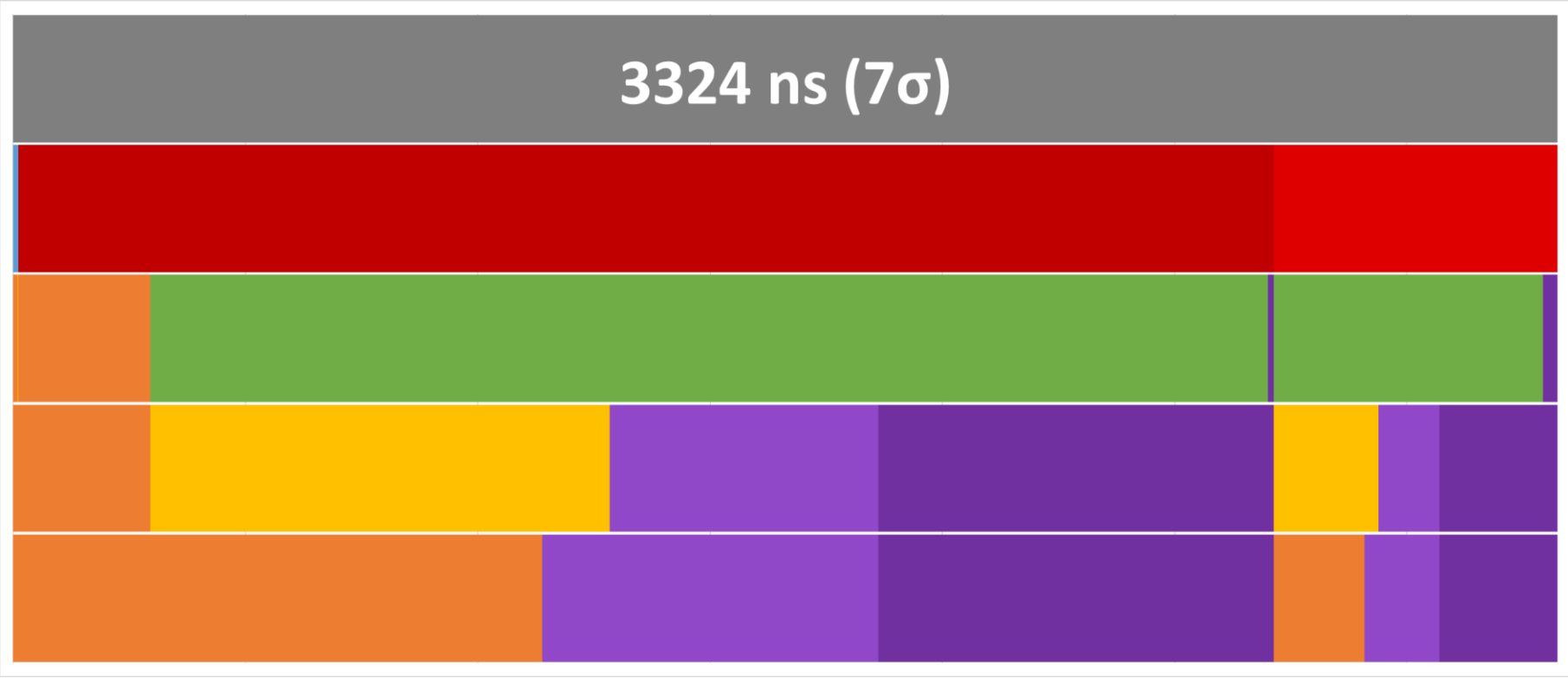
- Geoff Garner, "New Simulation Results for Time Error Performance for Transport over an IEC/IEEE 60802 Network Based on Updated Assumptions Revision 3" https://www.ieee802.org/1/files/public/docs2020/60802-garner-new-simulation-results-dte-updated-assumptions-60802-network-0920-v03.pdf
- Geoff Garner, "Further Simulation Results for Dynamic Time Error Performance for Transport over an IEC/IEEE 60802 Network Based on Updated Assumptions Revision 2" https://www.ieee802.org/1/files/public/docs2020/60802-garner-further-simulation-results-time-sync-transport-1120-v02.pdf
- Geoff Garner, "Effect of a Frequency Perturbation in a Chain of Syntonized Transparent Clocks" whitepaper https://www.ieee802.org/1/files/public/docs2007/as-garner-protocol-synton-chain-freq-offset-accum-0307.pdf
- Geoff Garner, "Effect of a Frequency Perturbation in a Chain of Syntonized Transparent Clocks" presentation https://www.ieee802.org/1/files/public/docs2007/as-garner-protocol-synton-chain-freq-offset-accum-vgs-0307.pdf

Content

- Baseline to “Pain-free”
- More Options (Varying Pain Levels)

Baseline to “Pain-free”

Baseline dTE Breakdown



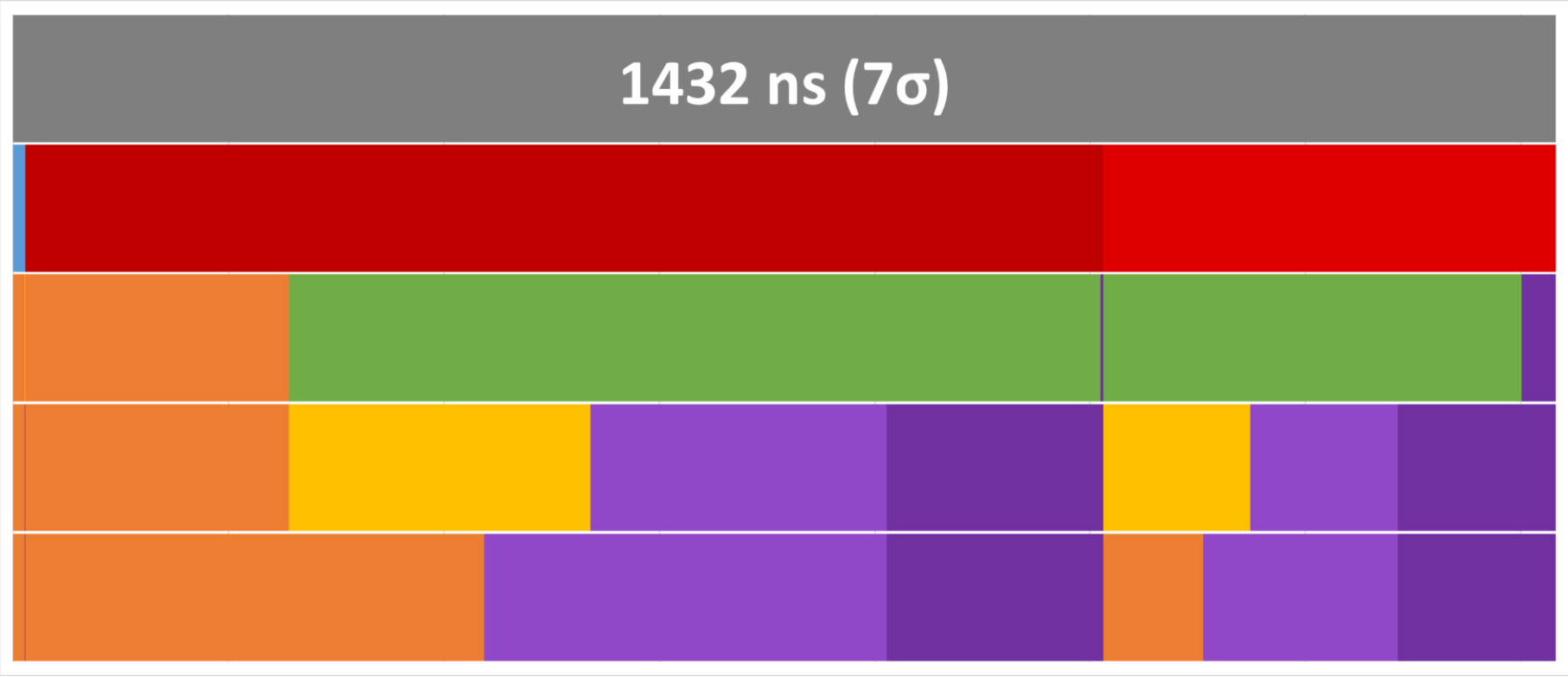
Baseline vs “Pain-free” – No Change

Parameter	Baseline	Pain-free
syncInterval	125ms Gamma distribution	
pDelayInterval	125ms Uniform distribution 90% - 130%	
Timestamp Granularity	8ns	
Dynamic Timestamp Error	±4ns	
meanLinkDelay Error Correction	95%	

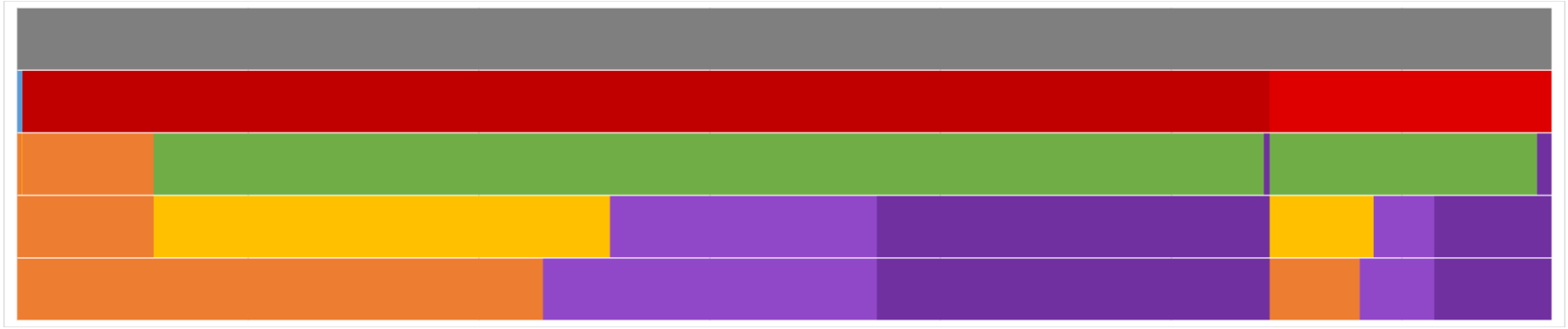
Baseline vs “Pain-free” – Differences

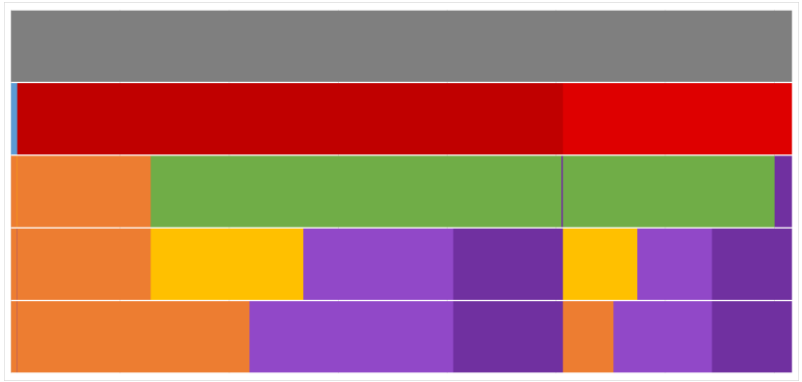
Parameter	Baseline	Pain-free
residenceTime	10ms Always 10ms, i.e. max limit	10ms Gaussian; mean 5ms; 6σ 5ms; min 1ms; max 10ms
pDelayTurnaroud	10ms Always 10ms, i.e. max limit	10ms Gaussian; mean 5ms; 6σ 5ms; min 1ms; max 10ms
mNRRsmoothingN	1	2
Temperature Ramp	Linear -40° to +85°C 1°C/s ; 30s Hold	Quarter-Sinusoidal -40° to +85°C 125s ramp up/down ; 30s hold

“Pain-free” dTE Breakdown



Baseline vs. “Pain-free”





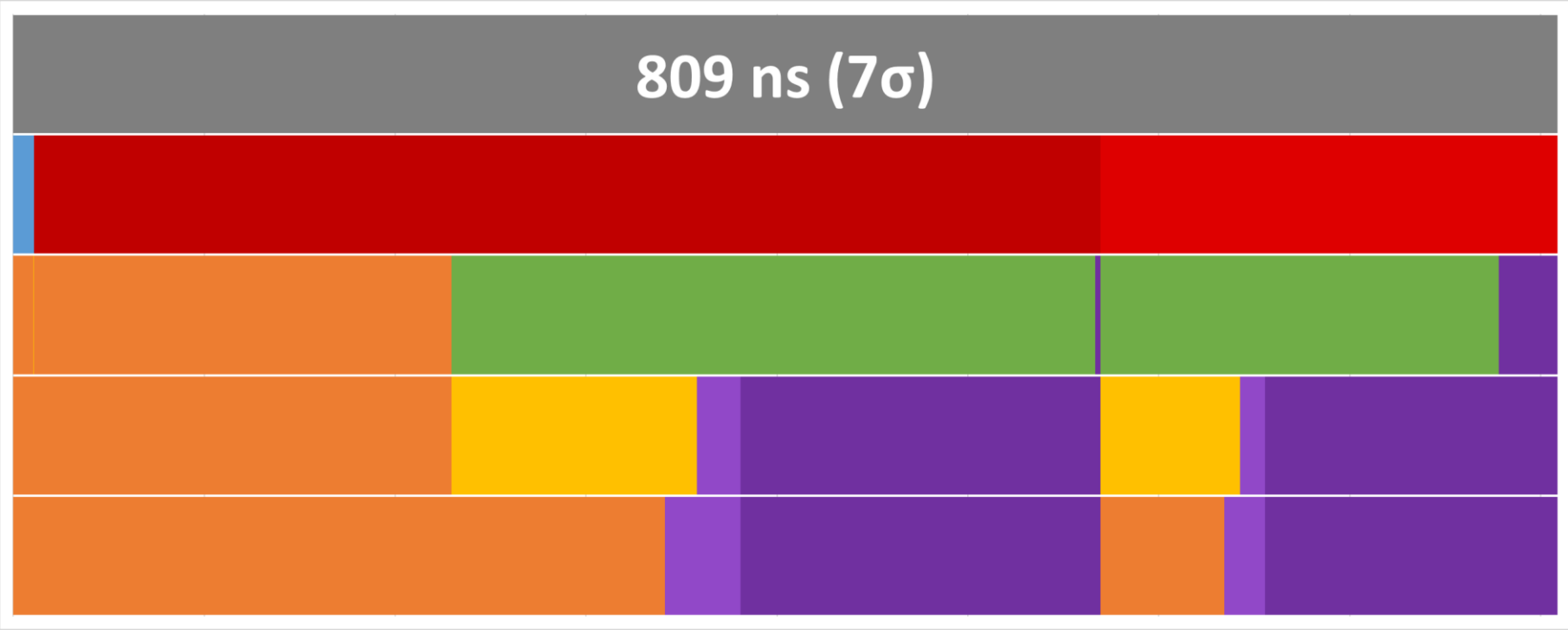
More Options

Varying Pain Levels

Baseline vs More Options

Parameter	Pain-free	More Options
pDelayInterval	125ms Uniform distribution 90% - 130%	125ms Uniform distribution 95% - 105%
NRR Drift Error Correction	0%	90%
mNRRsmoothingN	1	4

Other Options dTE Breakdown



Even More Options

- Align pDelayResp with Sync
- Send TLV with t1out following Sync to allow downstream node to update mNRR just prior to Sync calculation
- RR Error Correction

Thank you!