

ELECTRONICS & DEFENSE

The TSN use case for the MIURA microlaunchers

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Chapter 01

Motivation. TSN for New Space



TSN for New Space

- Standards-driven designs
- Low-cost, COTS components
- Automotive-grade SoC
- Real-time RTEMS
- FPGA-based TSN design
- Low footprint & resource usage

gPTP (802.1AS)	Reservation (802.1Qcc)	Redundancy (802.1CB)
TAS (802.1Qbv)	Preemption (802.1Qbu & Qbr)	



- Early application of TSN in aerospace for microlaunchers
- Development kickstarted before **P802.1DP**

 PLDSPACE™

ÚLTIMO LANZAMIENTO

**MIURA1 SN1 Test
Flight**

TSN as a control & communication backbone for Aerospace

TSN is a promising solution for aerospace. It could supersede the traditional alternatives (e.g., fieldbuses) given its determinism, large data rates, and its interoperability.

Usual alternatives for aerospace

Criteria	MIL-STD 1553B	CAN (CAN FD)	Space Wire	SpaceFibre	Standard GigaEthernet
Reduced Cost	--	+	--	---	++
Speed	- 1 Mbps	- 1 Mbps (8 Mbps)	++ 200 Mbps	+++ 2,500 Mbps	+++ 1,000-10,000 Mbps
Determinism /Reliability	++	++	++	++	-
Cable Length (at max speed)	+ 6.1m for transformer -coupled stubs	+ 40m	- 10m	++ 100m (expected)	++ 200m
Scalability	++	++	+	+	+++



The case for TSN + RTEMS OS

TSN GigabitEthernet	RTEMS RT OS
++	Commonly used in avionics
+++ 1,000-10,000 Mbps	Real-time scheduling coupled with deterministic TSN
++	Open development platform
++ 200m	
+++	

✓ COTS & Standards

✓ Explored in the Miura UC

→ **Other considerations:** sensors, payload, stresses (thermal, mechanical, radiation), ...

Image credit: Ref. [2]



Chapter 02

The Miura Microlaunchers: Miura 1 & Miura 5



Overview of the Miura Vehicles

- Reusable microlaunchers from PLD Space
- Carry payloads of up to 500 kg to the low Earth orbit
- Places Spain as the 10th country with direct access to space

Miura 1: Sounding rocket & demonstrator

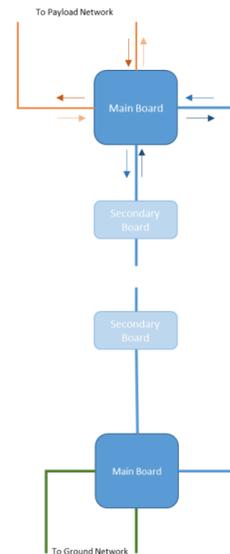
- *Launched on October 7th, 2023!*



Avionics Board

FPGA TSN design

- ✓ 4-Port, FPGA-based switch
- ✓ Real-time RTEMS OS
 - Custom Ethernet drivers
 - Native gPTP integration (**Novelty**)
 - RT task support for avionics
- ✓ Standards-driven design
- ✓ Low-cost, COTS components
- ✓ Automotive-grade Z-7030 SoC
- ✓ “New Space” paradigm of design
- ✓ Single-engine sounding rocket
- ✓ Carry small payloads of up to 300 kg to LEO



Miura 5: Commercial Vehicle

- *Ongoing development*



- ✓ Expected launch at the end of 2025/early 2026
- ✓ Larger payloads (up to 500 kgs) & reusable
- ✓ Larger vehicle with 5 engine modules and correspondingly higher TSN network complexity
- ✓ Same avionics as Miura 1
 - 4-Port FPGA TSN switch with RTEMS OS



Chapter 03

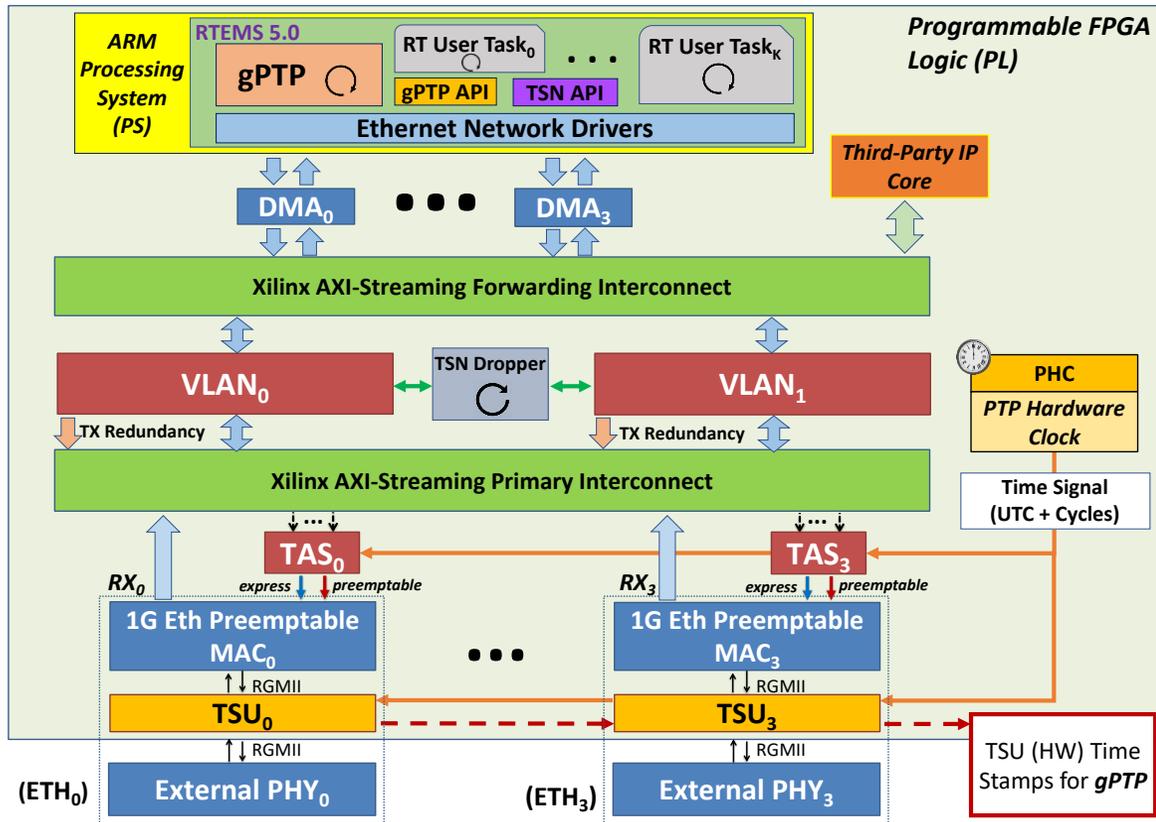
System design & Architecture



Embedded avionics with FPGA-based TSN

- Our TSN nodes for avionics use COTS components and a design approach suitable for the “New Space”: affordability, open and interoperable standards, agile design, and reusability.

System architecture on a Zynq-7000 SoC device



(MIURA 1)



(MIURA 5)

- ✓ Low-cost, COTS-based designs
- ✓ Automotive-grade Z-7030/7045 SoCs
- ✓ Embedded ARM processor for RTEMS.
- ✓ Additional I/O: CAN, GPIO, FMC, ...

Image credit: Ref. [2]

Real-time RTEMS. Determinism down to the “last inch” for TSN

Safe, real-time execution with key differences from other general-purpose OS environments.

Embedded avionics must ...

- Reliably **execute different types of tasks.**
- Harness real-time OS to **schedule transmission during available slots.**

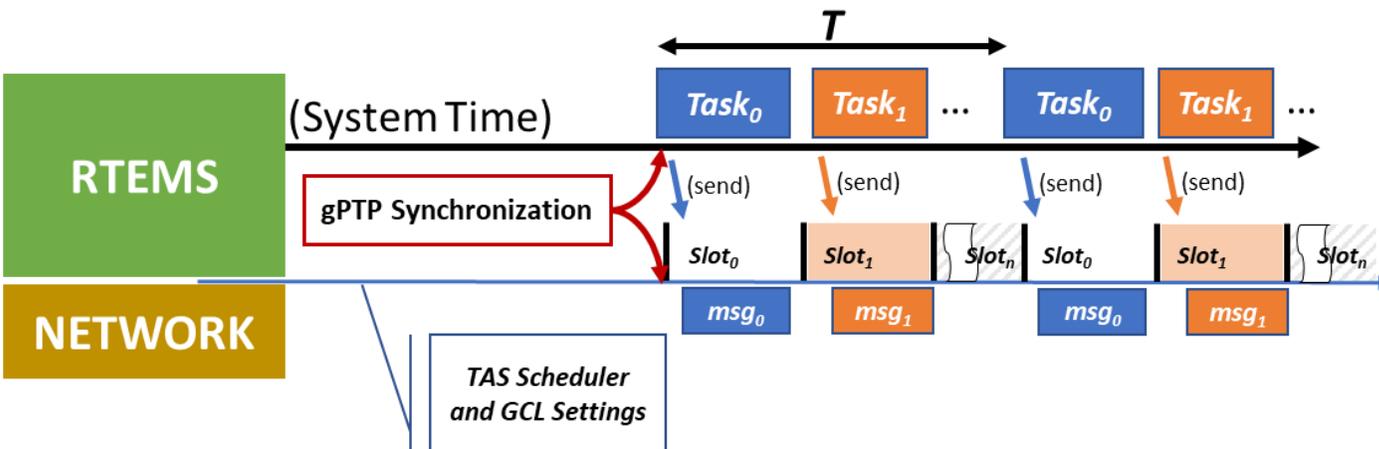
Types of tasks

Periodic

Monitoring, control loops, emission of housekeeping messages, etc.

Sporadic

(one-time) alarms, other system events, network controls, configuration protocols.



- ✓ Synchronize tasks to global system time to align transmissions to the TSN slots.
- ✓ The user should calculate the appropriate GCL and task scheduling settings

Image credit: Ref. [2]



Chapter 04

TSN for Miura: Traffic classes & Topology

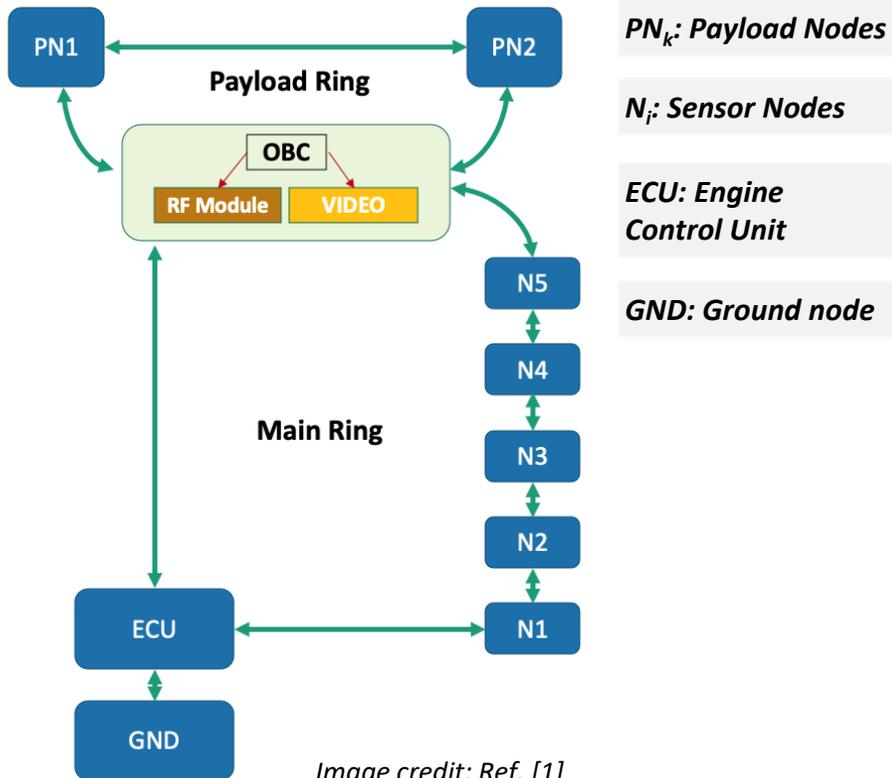


The use case of Miura 1

MIURA 1 Sounding Rocket (ESA GETDEN)

- **New Space Vehicle:** Low-cost mission, standards-based development.
- **Suborbital flight** → No Radiation hardening, automotive-grade components.
- **COTS Platform:** Zynq-7000 SoCs, Ethernet, TSN, low FPGA footprint.

Network topology



Traffic classes

Handle three main traffic classes with different levels of criticality:

Critical Commands

- Express & Redundant Forwarding.
- 10 packets/ms with 400-B payload.
- High priority.

Telemetry

- Express Forwarding.
- 10 packets/ms with 400-B payload.
- Medium priority.

Video

- Preemptable Forwarding
- Best-Effort @ 20 Mbps with 1500-B payload.

Communication requirements

→ Implement robust, deterministic avionics bus

GCL Settings, Routing, TSN Architecture

- Determinism better than 50 μ s (15 hops)
- Latency lower than 500 μ s (10 hops)

TAS, 802.1Qbu & 802.3br

- Reduced jitter
- Bounded delivery

802.1CB

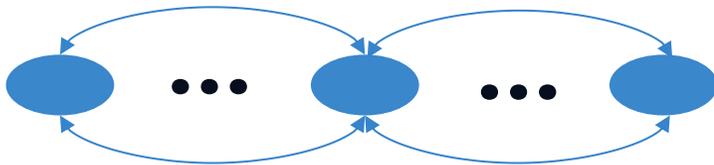
- Data robustness

The use case of Miura 5

- Commercial-grade microlauncher for carrying payloads of up 500 kg to LEO
- Larger, more complex vehicle than the demonstration platform of Miura 1 → Levies new requirements and greater complexity for the control network, traffic classes, system topology

Network topology

- ✓ Two coupled redundant rings
 - 1st & 2nd Stage
- ✓ Payload, OBC, Sensor, and Engine control modules
- ✓ 5-engine vehicle → Larger network & additional traffic classes
- ✓ Convergence of lower-priority monitoring, high-priority control traffic, and mission commands over the same, copper-based Ethernet links



Traffic classes

Critical Commands

- e.g., high-prio telemetry, mission commands, ...

Medium Priority

- e.g, mission commands, telemetry, ...

Best Effort

- e.g, some sensor reports, ...



High-priority gPTP

Communication requirements

- All flows transmitted redundantly using 802.1CB

- Statically configured paths over the network with significant traffic engineering

- TSN to transport highly critical messages for engine control, node reports, ...

- Redundancy & ring-based topology for resilience to single-point of failure for data & synchronization

- Underlying gPTP synchronization with built-in robustness using the best master clock algorithm (BMCA)

Analysis. Miura in the framework of 802.1DP (I)

Communication requirements

Determinism

- Bus determinism of 1 ms with worst-case latency of 1 ms over 15 hops
- Worst-case closed control loop cycle of 50 ms

802.1DP Analysis

- In keeping with ~ [1 – 100] ms range
- Loose jitter requirement up to latency limit

Synchronization

- Less than 0.5 ms
- Realizable: ~ 100 ns with Avnu-based implementation of gPTP
- Built-in resilience with support for BMCA
- Single synchronization domain
- Software service on RTEMS with FPGA support for HW time-stamping

- Within expected performance
- Could add support for additional domains
- Replace BMCA with FTTM

Network resilience

“Detect any change and reconfigure/adapt the network within 2 ms”

- Data traffic → zero-time recovery with FRER
- System synchronization → less than 300 ns during BMCA execution during 1 s

- No network recovery time appears to be specified in the aerospace profile
- Definition of upper/lower bounds could benefit the design of new systems and applications

Analysis. Miura in the framework of 802.1DP (II)

Communication requirements

Number of Hops

- Worst case of 15 hops for end-to-end transmission of all types of traffic

Topology

- Two redundant communication rings per launcher stage
- All flows, including BE, are sent redundantly using 802.1CB between the nodes
- Redundant timing paths also available through topology and BMCA

Number of streams

- 32 streams per switch
- 70 overall flows routed redundantly over the network

802.1DP Analysis

- Within desirable future use for aerospace systems

- Adheres to one of the proposed topologies for aerospace
- P802.1DP could suggest topology templates per vehicle type: e.g., launchers, aircraft, satellites, ...

- Lightweight TSN design with reduced number of flows
- Less than the lower bounds of 802.1DP

Analysis. Miura in the framework of 802.1DP (III)

Communication requirements

802.1DP Analysis

Traffic Shaping & Queueing

- Time-aware traffic shaping with preemption
- Up to eight priority-based queues for traffic shaping

- Synchronous TSN design partially conformant to Type 2 bridges

Stream Isolation & Interference

- VLAN-based traffic flow identification for stream isolation
- Frame preemption for minimizing BE interference on express flows

- Up to 32 streams per switch as expected in lower bound of 802.1DP
- P802.1DP could propose 802.1Qbu & 802.3br to further increase stream isolation

Media type & Frame size

- Ethernet-based copper links for interconnecting different nodes
 - Plastic fiber could also be a fit
- Ethernet frame size range: [60 – 1500] B

- Choice of copper-based links as customary
- No support for jumbo frames or FCoT

Analysis. Miura in the framework of 802.1DP (IV)

Communication requirements

Bandwidth & Link utilization

- Realizable rate on wire of 1-Gb/s Ethernet over copper links
- Utilization threshold below 10% of realizable rate for final application

Security & Integrity

- Data integrity guaranteed through the use of redundant stream transmissions
- No provisions yet for more advanced data integrity and security mechanisms

System Monitoring

- System health information transmitted in-band as specific TSN streams
- This includes debugging messages with the operation of the gPTP synchronization stack

802.1DP Analysis

- Actual utilization well below 50%, as expected in 802.1DP

- Integrity through 802.1CB
- P802.1DP could specify mechanisms such as MACSec or a Root of Trust for data security and to prevent tampering

- Monitoring supplied as additional system data, as expected in 802.1DP

Analysis. Miura in the framework of 802.1DP (V)

Communication requirements

End-to-end determinism

- Real-time applications synchronized to the network
- Determinism down to the "last inch":
 - Network time + TAS Schedule + App scheduling in RTEMS tied to TAS Schedule

Configuration

- Static configuration linked into binaries for the avionics firmware
- Generated at a centralized system configuration module aware of topology & traffic classes

Certification

Common misconception → "There is no ESA certification"

- Studying new programs and missions to further advance our design

802.1DP Analysis

- Compliance with the upper bound of determinism
- P802.1DP could provide interfaces & methods for "last-inch" determinism, e.g., PTM for PCIe-based systems & PTP

- Static, centralized configuration applied offline, as expected in 802.1DP

- P802.1DP could consider the provision of design guidelines to streamline the transition to specialized aerospace certification activities

Opportunities for advancement

a)

Time Synchronization

- Support greater number of synchronization domains
- Implement a specialized FTTM module
- Research **holdover modes** as an alternative to maintain synchronization accuracy during system recovery

d)

RT & Determinism to “the last inch”

- MIURA features the RT RTEMS OS with synchronized apps to the network
- P802.1DP **could benefit from specifying standardized interfaces and methodologies for synchronizing apps to the network and its corresponding GCL schedule.**

b)

Security & Integrity

- Protection against unauthorized tampering and component authentication could be addressed by defining **Root of Trust** mechanisms
- Data Integrity & Security could be addressed through the implementation of **MACSec**

c)

Certification

- **Suggest FPGA/ASIC design rules to streamline subsequent design certification efforts**
- Suggest best practices and design templates for early qualification for certification

e)

Real-time & Critical messages

- Support **802.1Qbu & 802.3br for reduced jitter and enhanced stream isolation**



Chapter 05

Experimental validation & Results

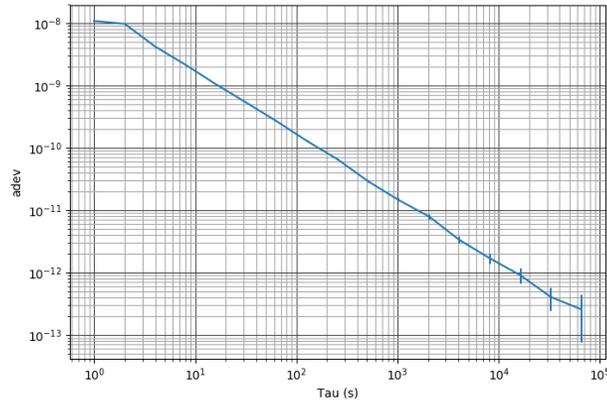


Some results from the Miura boards

Credit: Ref. [2]

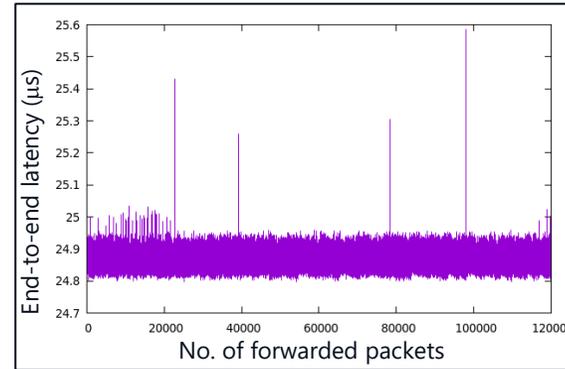
Synchronization

✓ ~ 100 ns accuracy for $\tau = 1$ s (ADEV)

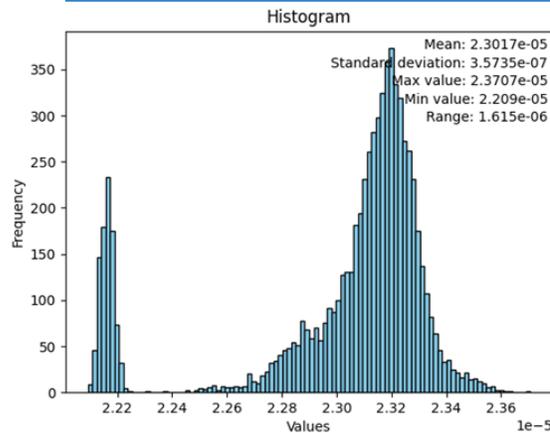


Traffic shaping with preemption

- ✓ Peak-to-peak: 750 ns - Std.Dev.: 20 ns
- ✓ gPTP peak-to-peak < 100 ns
- ✓ No losses with link failures



End-to-end latency



Baseline latency test

- ✓ 4 hops & No GCL shaping
- ✓ ~ 23 μ s @ 60 B (4 hops)
→ 5.75 μ s per hop
- ✓ ~ 35.48 μ s @ 300 B (4 hops)
→ 8.87 μ s per hop

FPGA footprint (Xilinx Z7030 SoC)

FPGA Primitives	VLAN + Redundancy	Dropper	TAS + Preemption	Switching Interconnects	Common Infrastructure (DMA, MAC, TSU,...)	Total Resource Utilization
Slice Registers	4550	2090	3170	1490	12840	39%
Slice LUT	4160	1120	1820	1800	10440	57%
BRAM	3,5	0	20	9	12	53%
DSP	8	34	0	0	0	13%
MMCM + PLL	0	0	0	0	1	40%

- ✓ Overall ~ 50% utilization for Z7030 SoC devices
- ✓ Overall ~30% utilization for Z7045 SoC devices



Chapter 06

Conclusions & Lessons learned



Conclusions



Miura has pioneered an early application of TSN for aerospace with significant performance results which can benefit from including the latest specifications from 802.1DP. Likewise, we believe that some lessons learned from our experience with Miura (and beyond) could further improve the definition of 802.1DP.

Real-time OS	New Space Design	TSN results for aerospace
<ul style="list-style-type: none"> ▪ RTEMS RT OS, as commonly used in avionics ▪ Custom interface to synchronize applications to the network ▪ Native gPTP implementation 	<ul style="list-style-type: none"> ▪ Use of commercial, off-the-shelf elements (COTS) with fast development & standards (TSN, Ethernet) ▪ Industrial- & automotive-grade components 	<ul style="list-style-type: none"> ▪ gPTP synchronization @ ~ 100 ns ▪ E2E latency over 15 hops lower than 200 μs ▪ Worst-case GCL-shaped jitter of up to ~700 ns ▪ Robust timing and data transfer with BMCA and FRER, respectively ▪ Reduced FPGA footprint: 50% (Z7030) & 30% (Z7045)
Preliminary TSN for Space	Certification	Lessons learned for 802.1DP
<ul style="list-style-type: none"> ▪ gPTP, TAS w/preemption, VLAN tagging, FRER, preemptable MAC ▪ Scalable FPGA-based design ▪ Lightweight implementation with 32 streams per node 	<p><i>*There is no ESA certification*</i></p> <ul style="list-style-type: none"> ▪ Ongoing: Trying to locate suitable programs to advance our design ▪ P802.1DP could suggest best practices & design rules to simplify the start of a certification process 	<ul style="list-style-type: none"> ▪ Certification processes & best practices could be addressed ▪ Explore new methods for timing robustness, such as holdover modes ▪ Improve stream isolation and reduce jitter with 802.1Qbu & 802.3 br ▪ Standardize interfaces to synchronize apps with the network for RT OS environments ▪ Consider the use of MAC Sec & Root of Trust

POWERED BY TRUST

References

- [1] J. Sanchez-Garrido et al., "**Implementation of a time-sensitive networking (TSN) Ethernet bus for microlaunchers**," in IEEE Transactions on Aerospace and Electronic Systems, doi: 10.1109/TAES.2021.3061806.
- [2] Jorge Sánchez Garrido, Luis Medina Valdés, Rafael Rodríguez, Javier Díaz, "**Cost-optimized TSN platform for aerospace applications based on RTEMS OS**," presented at TSN/A Conference, [Online], Oct. 7-8, 2020.
- [3] J. Sanchez-Garrido, "**Time-sensitive networks based on ultra-accurate synchronization mechanisms**," Ph.D. dissertation, Dept. Comp. Arch. Tech., Univ. Granada, Granada, Spain
- [4] L. Medina, M. Melara, and L. Cercós. "**An IPCORE for Deterministic Ethernet via Time Sensitive Networking (TSN) light implementation: challenges and opportunities**", in *13th ESA Workshop ADCSS*. Noordwijk, The Netherlands, Nov. 12-14, 2019. [Online]. Available: https://indico.esa.int/event/323/contributions/5043/attachments/3745/5201/12.30_-_An_IPCORE_for_Deterministic_Ethernet_via_TSN_..._.pdf