Frequency Hopping Spread Spectrum PHY of the 802.11 Wireless LAN Standard

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Why Frequency Hopping?

- Frequency Hopping is one of the variants of Spread Spectrum- a technique which enables coexistence of multiple networks (or other devices) in same area
- FCC recognizes Frequency Hopping as one of the techniques withstanding "fairness" requirements for unlicensed operation in the ISM bands.
- 802.11 Frequency Hopping PHY uses 79 nonoverlapping frequency channels with 1 MHz channel spacing.
- FH enables operation of up to 26 collocated networks, enabling therefore high aggregate throughput.
- Frequency Hopping is resistant to multipath fading through the inherent frequency diversity mechanism

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Regulatory requirements for FH

- North America (CFR47, Parts 15.247, 15.205, 15.209):
  - Frequency band: 2400-2483.5 MHz
  - At most 1 MHz bandwidth (at -20 dB re peak)
  - At least 75 hopping channels, pseudorandom hopping pattern
  - At most 1 W transmit power and 4 W EIRP (including antenna)
- Europe (ETS 300-328, ETS 300-339):
  - Frequency band: 2400-2483.5 MHz
  - At least 20 hopping channels
  - At most 100 mW EIRP
- Japan (RCR STD-33A):
  - Frequency band: 2471-2497 MHz
  - At least 10 hopping channels

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802.11 FH PHY vs. Regulations

- 1 MHz Bandwidth
- 79 hopping channels in North America and Europe; pseudorandom hopping pattern.
- 23 hopping channels in Japan.
- At most 1 W power; devices capable of more than 100 mW have to support at least one power level not exceeding 100 mW.
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802.11 FHSS Modulation Objectives

- Achieving at least 1 Mbit/sec rate
- Familiar, field proven, low cost technology - FSK
  - Constant Envelope- Saturated Amplifiers
  - Limiter-Discriminator detection
- Multichannel operation -transmit signal shaping to reduce adjacent channel interference
- Multiple rates - medium use optimization by taking advantage of short-range/good-propagation scenarios to increase rate

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802.11 FHSS Modulation

- Gaussian shaped FSK (GFSK) at F_{clk} = 1 Msymbol/sec
  - NRZ data is filtered with BT=0.5 low-pass Gaussian filter (500 KHz bandwidth at 3 dB) and then FM modulates a carrier
- 1 or 2 Mbit/sec with multilevel GFSK
  - 1 Mbit/sec: 2 level GFSK h_2=0.34
  - 2 Mbit/sec: 4 level GFSK h_4=0.45h_2=0.15
- 1 Mbit/sec operation mandatory; 2 Mbit/sec- optional
  - facilitates production of interoperable lower-rate/lower-cost and higher-rate/higher-cost equipment

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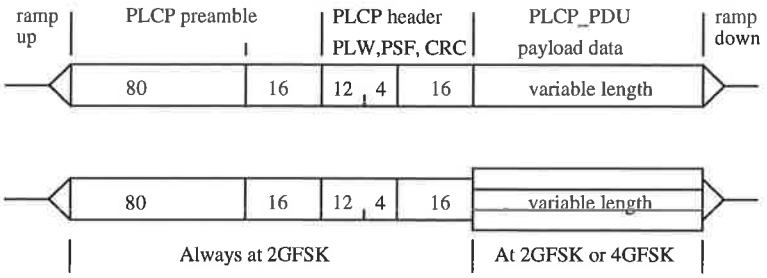
802.11 FHSS Frame Format



- PHY header indicates payload rate and length; CRC16 protected
- Data is whitened by a synchronous scrambler and formatted to limit DC offset variations
- Preamble and Header always at 1 Mbit/sec; Data at 1 or 2 Mbit/sec

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PLCP Preamble

- PLCP preamble starts with 80 bits of 0101 sync pattern, used to
  - detect presence of signal
  - to resolve antenna diversity
  - to acquire symbol timing
- Follows 16 bit Start Frame Delimiter (SFD)
  - the pattern is 0000 1100 1011 1101 (left bit transmitted first)
  - the SFD provides symbol-level frame synchronization
  - the SFD pattern is designed to optimize autocorrelation properties in conjunction with the 0101 pattern in front of it
  - the SFD pattern is balanced

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PLCP Header

- A 32 bit PLCP header consists of PLW (PLCP_PDU Length Word), PSF (PLCP Signaling Field) and 16 bit HEC (Header Error Check)
  - PLW (PLCP_PDU Length Word) is 12 bit field indicating the length of PLCP_PDU in octets, including the 32 bit CRC at the PLCP_PDU end, in the range 0 .. 4095
  - PSF (PLCP Signaling Field) is 4 bit field, of which currently 3 are reserved and the fourth is used to signal the PLCP_PDU data rate (1 or 2 Mbit/s)
  - HEC is a 16 bit CRC with CCITT generator polynomial $G(x)=x^{16}+x^{12}+x^5+1$
- The PLCP header is always transmitted at 1 Mbit/sec.

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PLCP_PDU Formatting

- Delineating data octets into serial stream, LSB first
- Scrambling: the data is XORed with periodic 127 bit LFSR sequence generated by a $1+x^4+x^7$ feedback polynomial
- Dividing serial bit stream into symbols:
  - at 1 Mbit/s, each bit is converted into 2FSK symbol
  - at 2 Mbit/s, each 2 bits are encoded into 4FSK symbol using Gray mapping
- DC offset control:
  - A polarity indication symbol is inserted in front of each 32 symbol block
  - The 33 symbol block is either inverted or not, as to maintain lower cumulative DC bias
  - DC offset control is important in PLL-based transmitters

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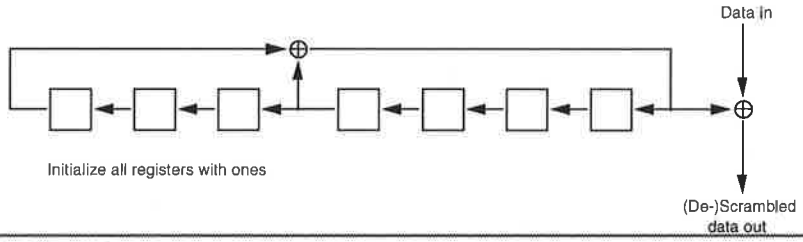
FH PHY Scrambler

- Scrambling is applied just to PLCP_PDU, not to PLCP header
- Scrambling is performed by a bitwise XOR with LFSR sequence with 127 bit period, with $1+x^4+x^7$ feedback polynomial
- Same method is used for scrambling and descrambling



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Bits to Symbol Mapping

- 1 bit (with 2GFSK) or 2 bits with (4GFSK) are mapped to a symbol
- at 2 bits/symbol Gray coded mapping is used, as customary with multilevel modulations.
- 2GFSK and 4GFSK have same RMS frequency deviation

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DC Bias Control

- The DC offset control is instrumental in reducing "baseline wander" in PLL based implementations (problem similar to transformer coupling in wired networks)
- Polarity indication symbol is added in front of each 32 symbol block - "0" for 2GFSK, "00" for 4GFSK (the symbol with most negative frequency offset)
- The sign of DC offset contribution of the 33 symbol block is compared to sign of previous accumulated DC offset; if same sign, the block is inverted (frequency deviation reversed at each symbol).
- At receive side, the polarity of the first (indication) symbol is tested- if positive, next 32 symbols are inverted.

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Transmit Ramp Up and Ramp Down

- The gradual Ramp Up and Ramp Down are required to reduce the splatter (spikes) in adjacent channels at start and ending of the packet.
- Up to 8 microseconds of the PLCP idle pattern and 8 microseconds following the last symbol of the PLCP_PDU are allocated to gradual increase and decrease of transmit power
- The minimal ramp time is dictated by adjacent channel interference specifications, and is not specified directly in the standard

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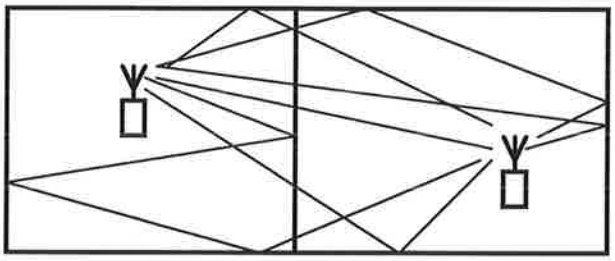
Indoor Environment - Multipath Fading



- Multiple propagation paths, interfering with each other, create a frequency selective fading.
- The fades are correlated at adjacent frequencies and get decorrelated after few megahertz in an indoor environment

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Frequency Hopping Sequences- Reqts.

- Design Criteria:
  - Assured minimum hop distance for multipath diversity performance
  - Minimizing hits and adjacent channel hits between different hopping patterns
  - Minimizing consecutive hits between different hopping patterns
- FCC 15.247 requirement: Pseudorandomly ordered frequency list

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Frequency Hopping Sequences

- Predesigned computer generated pseudorandom list of 79 frequencies
- Minimum hop distance of 6 channels
- Additional hopping sequences derived by modulo 79 frequency offset
- 78 hopping patterns organized in 3 sets of 26 patterns each.
  - Sequences from same set collide 3 times on average, 5 times worst case, over a hopping pattern cycle, including hits and adjacent channel hits.
- Aggregate throughput continues to increase up to about 15 collocated networks, at high load conditions.

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Frequency Hopping Sequences- cont.

- Denote frequency as 2402+b[i], b[i] is the base sequence in range 0.. 78.
- k-th sequence is formed from the base sequence as 2402+(b[i]+k) mod 79
- Example:
  - Base seq: 2402, 2456, 2472, 2447, ...
  - 30-th seq: 2432, 2407, 2423, 2477, ...

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FHSS Transmitter Specifications

- Deviation:
  - Upper bounded by FCC requirements
  - Lower bounded to +/-110 KHz in order to maintain sensitivity
- Shape accuracy:
  - Zero crossing instants accuracy - <+/- 1/8 symbol (at 2GFSK)
  - Level accuracy
- Center Frequency accuracy - 60 KHz (25 PPM)
- Symbol rate - 1 MHz +/- 50 ppm
- Hop Time- transmitter has to settle within 224 microseconds to within 60 KHz off nominal center frequency after

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Receiver Performance Specifications

Parameter	1 Mb/s	2 Mb/s
Sensitivity	-80 dBm	-75 dBm
Desensitization		
@ 2 Mhz offset	30 dB	40 dB
@ 3 Mhz or more	20 dB	30 dB
Intermodulation Protection	30 dB	25 dB

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CCA- Clear Channel Assessment

- CCA is used to:
  - Initiate frame reception
  - Avoid transmitting when the channel is busy
- The Backoff Slot width for FHSS PHY is 50 microseconds. The CCA should detect a signal which started up to 16 microseconds before end of the slot
- CCA Sensitivity:
  - -85 dBm for P_T<20 dBm, reduced by 0.5 dB for each dB of power increase
  - Detection during 0101 pattern within 20 microseconds with 90% probability

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