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Re:	This contribution is for call for contribution about IEEE P802.16e/D5-2004
Abstract	This contribution proposes the MSS buffer capability information for H-ARQ.
Purpose	
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SS's HARQ buffer capability negotiation for DL H-ARQ operation

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1. Problem statements

H-ARQ scheme is an optional and can be enabled on per-terminal basis. This scheme may be supported only for the OFDMA PHY. The signaling of the per-terminal H-ARQ and associated parameters shall be done during initialization procedure. The associated parameters mentioned above are *(M)SS Capability encodings*, *bandwidth allocation support*, *capabilities for construction and transmission of MAC PDUs* and *physical parameters supported* and many others.
For the IR H-ARQ scheme, the MSS shall be able to store the different versions of subpackets to successfully decode the corresponding H-ARQ encoded packet. The MSS shall be capable of supporting the reordering to deliver the received MAC PDUs to the upper layer in order.

If the BS knows the MSS memory ability, the BS may allocate the reasonable amount of downlink H-ARQ resource to the MSS through compact DL-MAP IE. If the BS allocates the downlink H-ARQ bandwidth to the MSS without the MSS buffer ability, the MSS may fail to decode the downlink H-ARQ encoded packet because of lack of memory. The more H-ARQ channels, the more storages the MSS needs.

Without signaling of MSS buffer capability, even though the channel condition is getting enough good, the possibility of retransmission and the traffic latency may be increased because of MSS buffer overflow. Therefore, it needs MSS buffer capability signaling during initialization procedure.

2. Proposed remedy

Add the parameter 'MSS buffer capability' into (M)SS Capability encodings which may be included in SBC-REQ/SBC-RSP or REG-REQ/REG-RSP messages. The H-ARQ enabled MSS informs the BS of its buffer capability during initialization procedure as follows.

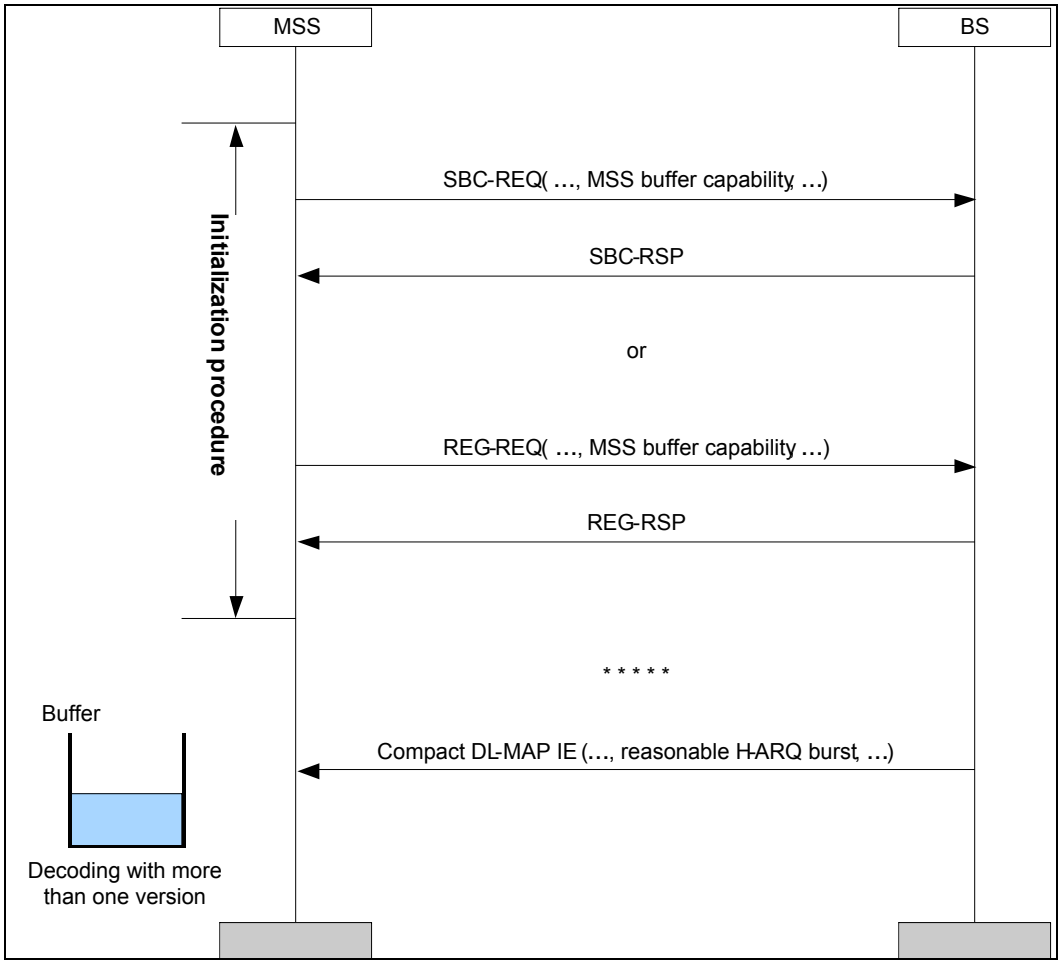

Figure 1. H-ARQ procedure with MAC buffer capability signaling

3. Proposed text change

~~*[Change section 6.3.17 as indicated]*~~

~~Hybrid automatic repeat request (H-ARQ) scheme is an optional part of the MAC and can be enabled on a per-terminal basis. H-ARQ may be supported only for the OFDMA PHY. The per terminal H-ARQ and associated parameters shall be specified and negotiated during initialization procedure. A burst can not have a mixture of H-ARQ and non H-ARQ traffic.~~

~~One or more MAC PDUs can be concatenated and an H-ARQ packet formed by adding a CRC to the PHY burst. Figure 130 shows how the H-ARQ encoder packet is constructed.~~

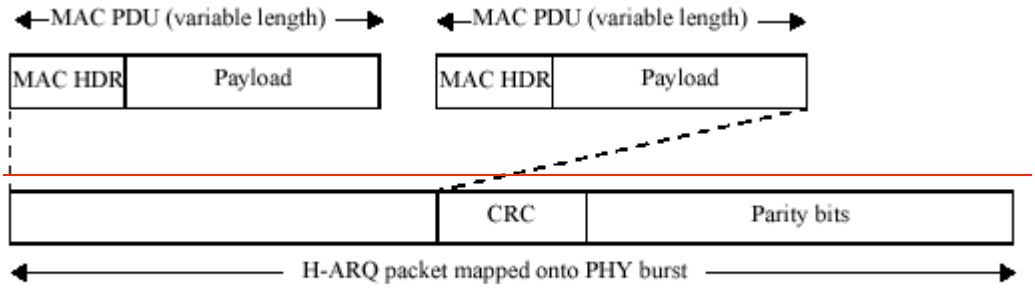

Figure 130—Construction of H-ARQ encoder packet

~~Two main variants of H-ARQ are supported, Chase Combining or Incremental Redundancy (IR). For IR, the PHY layer will encode the H-ARQ packet generating several versions of encoded subpackets. Each subpacket shall be uniquely identified using a subpacket identifier (SPID). For Chase Combining, the PHY layer shall encode the H-ARQ packet generating only one version of the encoded packet. As a result, no SPID is required for Chase Combining.~~

~~For downlink H-ARQ operation, the BS will send a version of the encoded H-ARQ packet. The MSS will attempt to decode the encoded packet on this first H-ARQ attempt. If the decoding succeeds, the MSS will send an ACK to the BS. If the decoding fails, the MSS will send a NAK to the BS. In response, the BS will send another H-ARQ attempt. The BS may continue to send H-ARQ attempts until the MSS successfully decodes the packet and sends an acknowledgement.~~

~~For IR, each H-ARQ attempt may have a uniquely encoded subpacket. The rule of subpacket transmission is as follows:~~

~~1) At the first transmission, BS shall send the subpacket labeled '00'.~~
~~2) BS may send one among subpackets labeled '00','01','10', or '11' in any order.~~
~~3) BS can send more than one copy of any subpacket, and can omit any subpacket except the subpacket labeled '00'.~~

~~In order to specify the start of a new transmission, one bit H-ARQ identifier sequence number (AI_SN) is toggled on every H-ARQ attempt on the same H-ARQ channel. If the AI_SN changes, the receiver treats the corresponding H-ARQ attempt as belonging to a new encoder packet, and discards previous H-ARQ attempt with the same ARQ identifier.~~

~~The H-ARQ scheme is basically a stop-and-wait protocol. The ACK is sent by the MSS after a fixed delay (synchronous ACK) defined by H-ARQ DL ACK delay offset which is specified in DCD message. Timing of retransmission is, however, flexible and corresponds to the asynchronous part of the H-ARQ. The ACK/NAK is sent by the BS using the H-ARQ Bitmap IE, and sent by a MSS using the fast feedback UL subchannel.~~

~~The H-ARQ scheme supports multiple H-ARQ channels per a connection, each of which may have an encoder packet transaction pending. The number of H-ARQ channels in use is determined by BS. These ARQ channels are distinguished by an H-ARQ channel identifier (ACID). The ACID for any subpackets can be uniquely identified by the control information carried in the MAPs.~~

~~H-ARQ can be used to mitigate the effect of channel and interference fluctuation. H-ARQ renders performance improvement due to SNR gain and time diversity achieved by combining previously erroneously decoded packet and retransmitted packet. The MSS which supports H-ARQ scheme shall be equiped with enough buffer ability to perform the combining of several versions of H-ARQ encoded packets and reordering of the successfully decoded H-ARQ~~

~~packets. Therefore, MSS buffer capability associated with H-ARQ shall be specified and negotiated during initialization procedure.~~

[Add the following text to section 11.7.8]

11.7.8.11 HARQ buffer capability

This parameter defines the MSS ability to process the received H-ARQ packets. For IR, the MSS shall have enough memory to store more than one H-ARQ encoded packet and support reordering of the received H-ARQ packets. During the initialization procedure, the MSS needs to inform the BS of its ability for DL-HARQ. After establishment of H-ARQ service connection, the BS shall allocate the downlink resource for the established H-ARQ service based on the signaled MSS buffer ability.

Type	Length	Value	Scope
22	1	Index that defines the MSS buffer capability for DL HARQ connections.	REG-REQ REG-RSP SBC-REQ SBC-RSP

The following table defines the indices above mentioned.

Table 1 xxx- Index for HARQ buffer capability

Index	Buffer capability	Default N_{EP} (Index/16)	Number of H-ARQ channels (N)
0 ... 15	An index means that the MSS has enough buffer to properly process ((Index%16)+1) H-ARQ channels with N_{EP} =144 bits.	144 (Index/16=0)	1 ... 16
16 ... 31	An index means that the MSS has enough buffer to properly process ((Index%16)+1) H-ARQ channels with N_{EP} =192 bits.	192 (Index/16=1)	1 ... 16
32 ... 47	An index means that the MSS has enough buffer to properly process ((Index%16)+1) H-ARQ channels with N_{EP} =288 bits.	288 (Index/16=2)	1 ... 16
48 ... 63	An index means that the MSS has enough buffer to properly process ((Index%16)+1) H-ARQ channels with N_{EP} =384 bits.	384 (Index/16=3)	1 ... 16
64 ... 79	An index means that the MSS has enough buffer to properly process ((Index%16)+1) H-ARQ channels with N_{EP} =480 bits.	480 (Index/16=4)	1 ... 16
80 ... 95	An index means that the MSS has enough buffer to properly process ((Index%16)+1) H-ARQ channels with N_{EP} =960 bits.	960 (Index/16=5)	1 ... 16
96 ... 111	An index means that the MSS has enough buffer to properly process ((Index%16)+1) H-ARQ channels with N_{EP} =1920 bits.	1920 (Index/16=6)	1 ... 16
112 ... 127	An index means that the MSS has enough buffer to properly process ((Index%16)+1) H-ARQ channels with N_{EP} =2880 bits.	2880 (Index/16=7)	1 ... 16
128 ... 143	An index means that the MSS has enough buffer to properly process ((Index%16)+1) H-ARQ channels with N_{EP} =3840 bits.	3840 (Index/16=8)	1 ... 16
144 ... 159	An index means that the MSS has enough buffer to properly process ((Index%16)+1) H-ARQ channels with N_{EP} =4800 bits.	4800 (Index/16=9)	1 ... 16
160 ... 175	An index means that the MSS has enough buffer to properly process ((Index%16)+1) H-ARQ channels with N_{EP} =9600 bits.	9600 (Index/16=10)	1 ... 16
176 ... 191	An index means that the MSS has enough buffer to properly process ((Index%16)+1) H-ARQ channels with N_{EP} =14400 bits.	14400 (Index/16=11)	1 ... 16
192 ... 207	An index means that the MSS has enough buffer to properly process ((Index%16)+1) H-ARQ channels with N_{EP} =19200 bits.	19200 (Index/16=12)	1 ... 16

208 ... 223	An index means that the MSS has enough buffer to properly process ((Index%16)+1) H-ARQ channels with N_{EP} =24000 bits.	24000 (Index/16=13)	1 ... 16

According to table xxx, the default N_{EP} size for index/16=0 is 144, 1 is 192, and so forth. Finally, default N_{EP} size for index/16=13 is 24000. The BS shall not allocate more bits than the (default N_{EP} size that corresponds to the signaled index) * ((Index%16)+1) as the downlink HARQ burst for the MSS. The BS may also assign the downlink HARQ burst to the MSS which has informed its HARQ buffer capability index *i*, *i*=0...223, as follows.

If $M * S \leq$ (default size corresponds to i)*((i%16) +1), BS may allocate M HARQ channels to the MSS and transmit $N_{EP} = S$ bits on each HARQ channel.
Here, M means the number of HARQ channel(s) which the BS may actually allocate to the MSS.
S means the actual N_{EP} size that the BS allocates to the MSS and may not same as the default size for the index the MSS informed to the BS.