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Re:	IEEE P802.16-2004/Cor1-D1	
Abstract	Correct the misfortunate combination of interleaver and permutation	
Purpose	Adopt changes	
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Problem in Interleaver and Permutation Combination in OFDMA

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1. Motivation

The interleaver definition with d=16 might cause a performance degradation in some cases, due to a disastrous combination of interleaving and permutation. This is because, in OFDMA, the permutation actually performs an "interleaving like" operation, which partially reverse the current interleaver operation. This performance degradation occurs with burst allocations having low frequency diversity, for example bursts allocated to a single sub-channel. In these cases, adjacent coded bits might be transmitted on the same sub-carrier. Thus the interleaver operation becomes useless.
Simulation results show, in a worst case scenario, a degradation of about 4 dB at BER of 10^-4, with the current interleaver compared to interleaver bypass scheme. It is unreasonable to use an interleaver which might cause severe performance degradation in some cases, whereas it is supposed to improve the performance.

Thus, we propose modifications to both interleaving scheme and permutation to allow equal (better) performance to all burst allocations.

2. Details

For an interleaver with dimension d, a pair of adjacent coded bits before the interleaver is separated after the interleaver by distance Ncbps/d bits. If a FEC block spans more than one slot duration, then several bits from the same FEC block are transmitted on each sub-carrier. These bits are distributed in the FEC block periodically, where the period equals the number of bits in a single symbol divided by the distance.

With the current interleaver dimension d = 16, for a worst case scenario (DL PUSC, burst allocation of 1 sub-channel, 4 slots in a FEC block, QPSK constellation) this period can be as small as 2 bits !! This example is depicted in Figure 1 where the numbers in brackets are the indices of the coded bits before the interleaver.

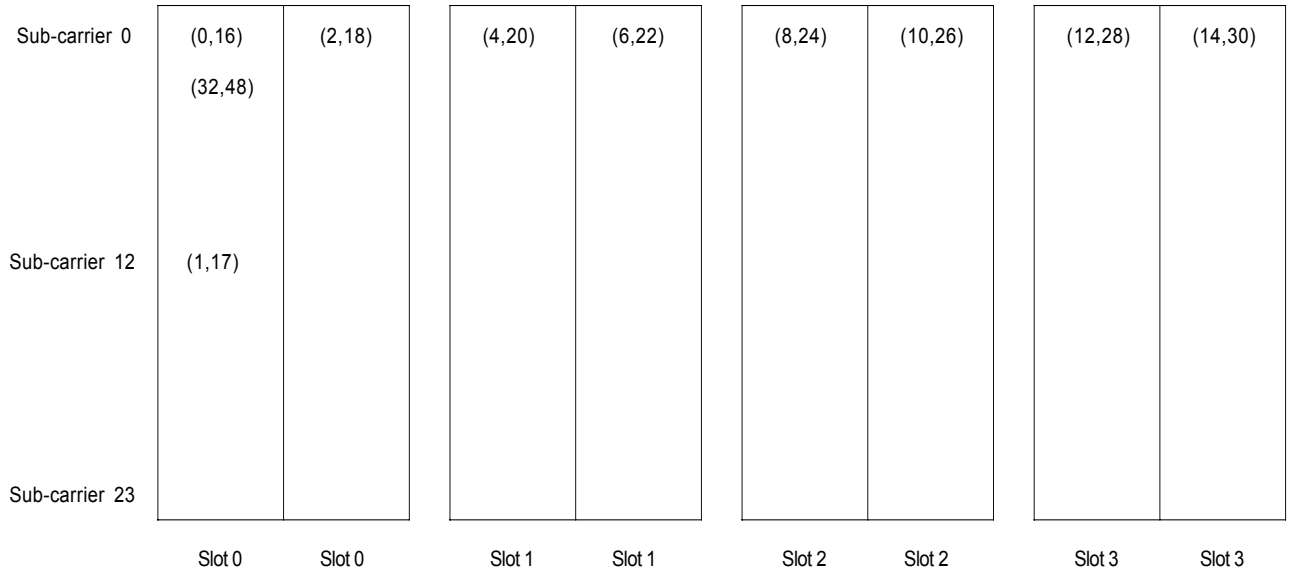

Figure 1: Worst case scenario of permutation-interleaver combination

The reason for this is that the order of subcarriers passed to the de-interleaver (in the receive side) is not a linear frequency-domain order (which the interleaver was designed for), but an order that depends on the permutation, on the way the 48 logical subcarriers are mapped to physical subcarriers the in-slot rotation between subchannels, and the way the slots are aggregated. The following figure shows the correlation structure in a FEC block on which the deinterleaver works (and of which the interleaver is unaware):

Similar colors mean high correlation (of fading):

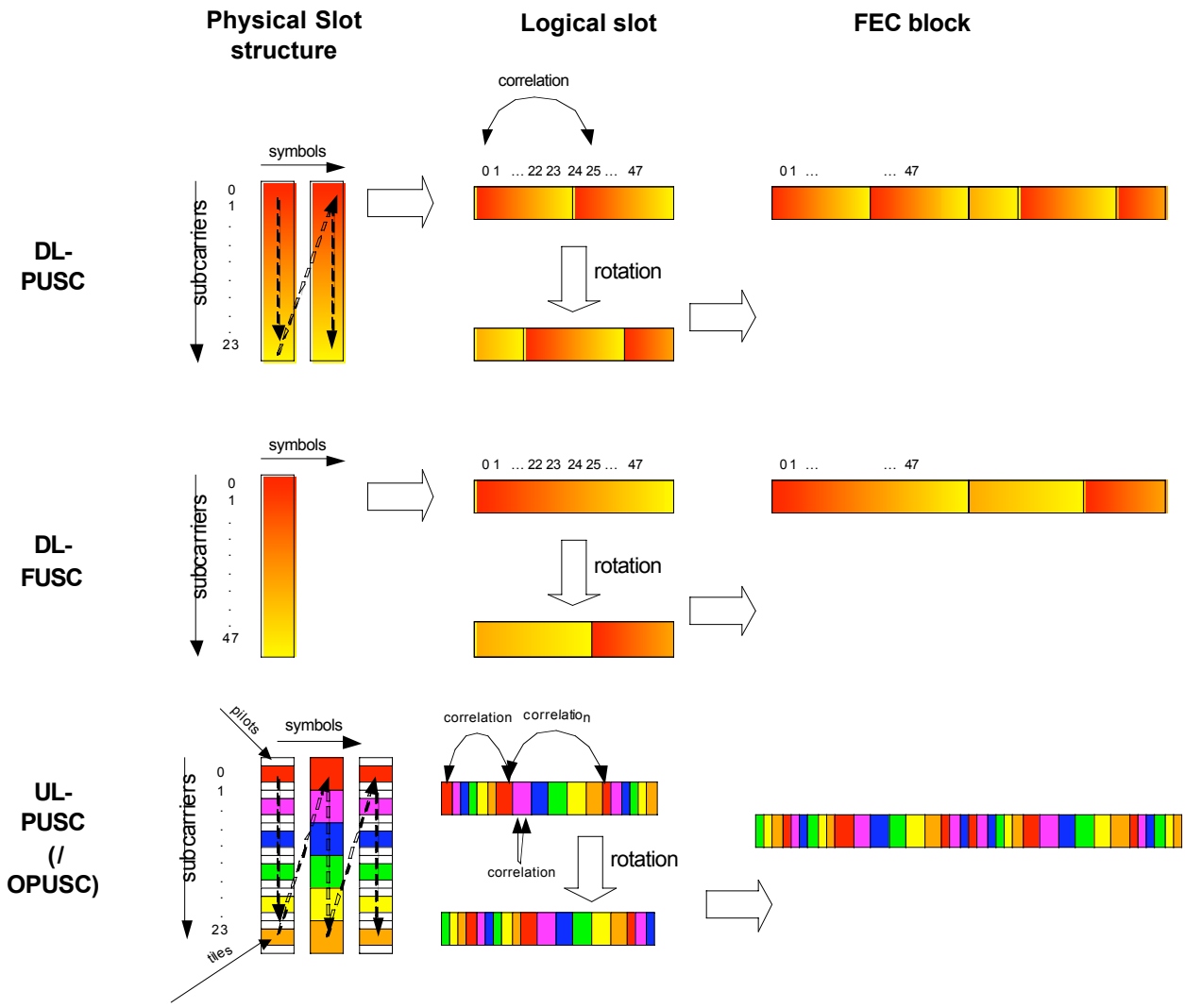

Figure 2: Example of correlation in slot and FEC block

The seemingly "random" structure of correlations in the FEC block are processed by the de-interleaver and create another "seemingly random" correlation structure at the input to the decoder. However, since these sequences are repetitive and not random, there are misfortunate choices of FEC block size for each permutation that create high correlations and reduce the performance significantly.

Our target is to first make this correlation structure similar between permutation, and correct the interleaver or the slot aggregation to solve this problem.

3. Simulation results

To be competed

4. Changes summary

We present two alternatives, which are summarized in the following table:

	Alternative A	Alternative B
Interleaver dimension UL	6N	6
Interleaver dimension DL	12N	12
PUSC time first	+	+
Sub-channel reordering	k+48*n (Stays the same)	k*N+(n-k)modN
In-slot rotation (n+13*s)	Stays the same	Remove
Repetition	Stays the same	Should be changed

where

N – number of allocated slots per FEC block

k – sub-carrier index

n – slot index

4.1. Changes relevant to both alternatives

Both alternatives utilize mapping of the data sub-carriers inside a slot in time-first order, instead of frequency first order. This mapping is relevant to DL PUSC and UL PUSC. By doing so, all permutations (namely: FUSC, DL PUSC and UL PUSC) can be treated the same by the interleaver. The logical subcarriers 0..47 have decreasing order of correlation for subcarriers that are further apart.

4.2. Alternative A

Change the interleaver dimension to be dependent on the number of slots in FEC block (N). Specifically, the interleaver dimension in the UL is 6N, and in the DL is 12N. With these interleaver dimensions the distance between 2 adjacent coded bits is 4 sub-carriers in the DL and 8 sub-carriers in the UL, i.e. 2 adjacent coded bits in the UL resides in 2 different tiles. With the interleaver dimension a multiple of N, we get the effect of interleaving each slot separately. This simple change provides a remedy to the problem, however it does not offer time diversity. The reason for choosing 6N for the uplink is that the diversity order of each slot is 6 (6 tiles), and each 8 subcarriers are correlated, so increasing the dimension above 6N would create couples of adjacent bits that reside in the same tiles and are correlated. In the downlink, the dimension 12N is designed to slightly increase the distance between subcarriers carrying adjacent bits (4 subcarriers compared to 3 subcarriers today).

4.3. Alternative B

Use the same interleaver (with interleaver dimension equals 6 / 12 in the UL / DL respectively), however reorder the sub-carriers in the FEC block. The purpose of this reordering is to gather adjacent sub-carriers in frequency domain and in time domain, so that adjacent sub-carriers in the interleaver input will have significant correlation. The proposed reordering operation is depicted in Figure 2:

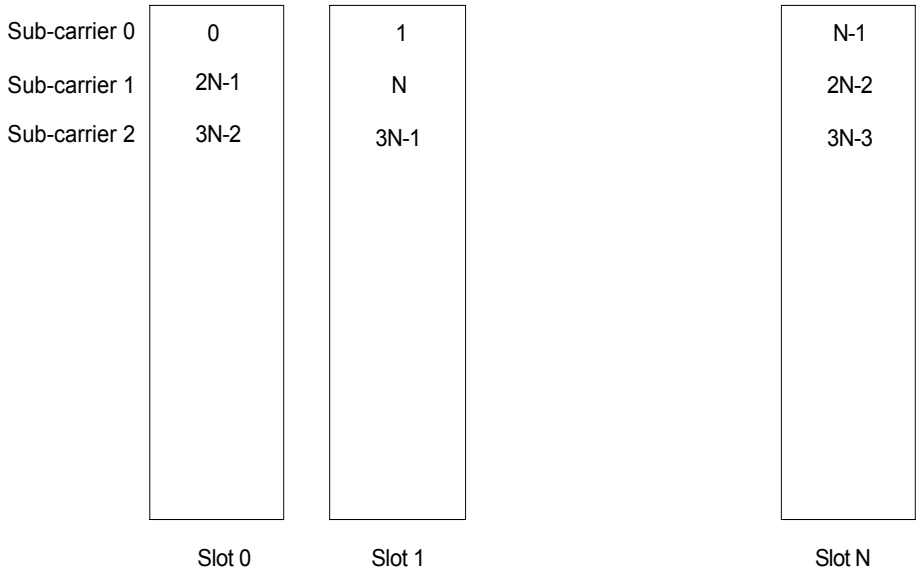

Figure 3: Sub-carrier reordering

In order to do the reordering properly, we need to remove the in-slot rotation, for both DL and UL. Removal of the in-slot rotation requires a change in the way repetition is done. We suggest that each slot shall be rotated by 48·n/R subcarriers where R is the number of repetition and n is the repetition index (0 .. R-1).

After this remedy is applied the correlation structure in a FEC block before de-interleaving will look as follows:

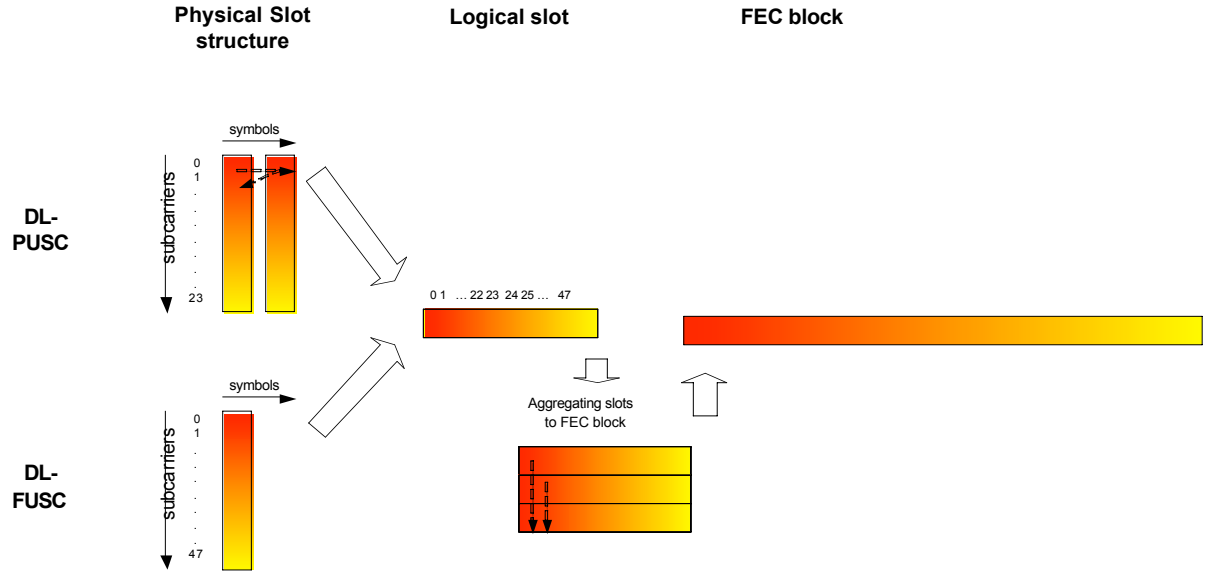

Figure 4: FEC block correlation after correction

5. Text changes

5.1. Changes relevant to both alternatives

8.4.6.1.2.1.1 Downlink subchannels subcarrier allocation in PUSC

[Change the numbered items of the first paragraph]

5) The data subcarriers of each slot shall be mapped to the subchannel such that even numbered data subcarriers (0,2,4,… 46) ~~numbered 0 to 23~~ reside on the first (time wise) symbol of each symbol pair on the subcarriers whose index is 0 to 23 respectively in Equation (111) and the odd numbered data subcarriers (1,3,5,… 47) ~~numbered 24 to 47~~ reside on the second symbol on the subcarriers whose index is 0 to 23 respectively in Equation (111).

8.4.6.2.2 Partitioning of subcarriers into subchannels in the uplink

[Change the first bullet of the enumerated list below Equation (113)]

1. After allocating the pilot carriers within each tile, indexing of the data subcarriers within each subchannel is performed in a time-first order starting from the first symbol at the lowest indexed subcarrier of the lowest indexed tile and continuing in an ascending manner throughout the slot symbols in the same subcarrier, then going to the next subcarrier at the lowest index symbol in the slot, and so on. ~~subchannel's subcarriers in the same symbol, then going to the next symbol at the lowest indexed data subcarrier, and so on.~~ Data subcarriers shall be indexed from 0 to 47.

8.4.9.3 Interleaving

[Delete all d=16 appearances, in formulas (130) - (133)]

5.2. Alternative A

8.4.9.3 Interleaving

[Add the following sentence at the end of the second paragraph]

The value of d shall be set to 12n for the DL and 6n for the UL, where n is the number of allocated slots per FEC block.

5.3. Alternative B

To be completed