Closed loop power control for FDD

Document Number: S80216maint-08_001
Date Submitted: January 17, 2008
Source:
Jaehee Cho(Jaehee1.cho@samsung.com), June Moon, Yongsuk Kim, Kwanhee Rho, Changyoon Oh
Samsung Electronics

Venue:
IEEE 802.16 Session #53 , in Levi, Finland
Base Contribution:
C80216maint-08_001
Purpose:
Discuss and adopt

Contents

Introduction

- Fast power control brings benefit for
  - UL channels having the characteristics of circuit mode
    - CQICH, ACKCH and possibly persistent allocation scheme being considered
- Fast power control needs CLPC in FDD mode
  - OLPC can’t compensate the UL fast fading due to the lack of reciprocity of DL/UL channel in FDD mode
- Frequent Tx of power control command for fast PC
  - Large overhead with the current IEEE PC messages

Benefit of fast power control

- System model
  - OLPC
    - Only compensate long term path loss and shadowing
    - UL channel estimate is obtained from the DL channel estimation and no delay is assumed between DL estimation and applying OLPC to UL
    - Ideal DL (thus ideal UL) channel estimate is assumed
  - Fast CLPC
    - Compensate fast fading as well as path loss and shadowing
    - BS estimate the UL channel and send power control command to MS
    - 1 or 2 frame delay (5 or 10ms power control delay) is assumed between UL estimation and applying CLPC to UL
    - Ideal UL channel estimate is assumed

Benefit of fast power control: Simulation results

- Simulation conditions
  - **Link level simulation for UL CQICH and ACKCH**
  - Target PER of 1%
  - 2 Rx Ant @ BS
  - Fast fading (**Ped-A and Ped-B 3km)** is applied for the simulation
  - Constant Tx power is assumed for the OLPC
  - Power control applied for CLPC in every frame with 1 and 2 frame delay

- SNR gain of fast CLPC over OLPC

Control CH type	Channel type	CLPC (1 frame delay)	CLPC (2 frame delay)
CQICH	Ped-A 3km/h	**4.7dB**	3.5dB
	Ped-B 3km/h	1.9dB	1.6dB
ACKCH	Ped-A 3km/h	**4.0dB**	3.2dB
	Ped-B 3km/h	1.6dB	1.5dB

Proposed solution

Review of the current power control commands

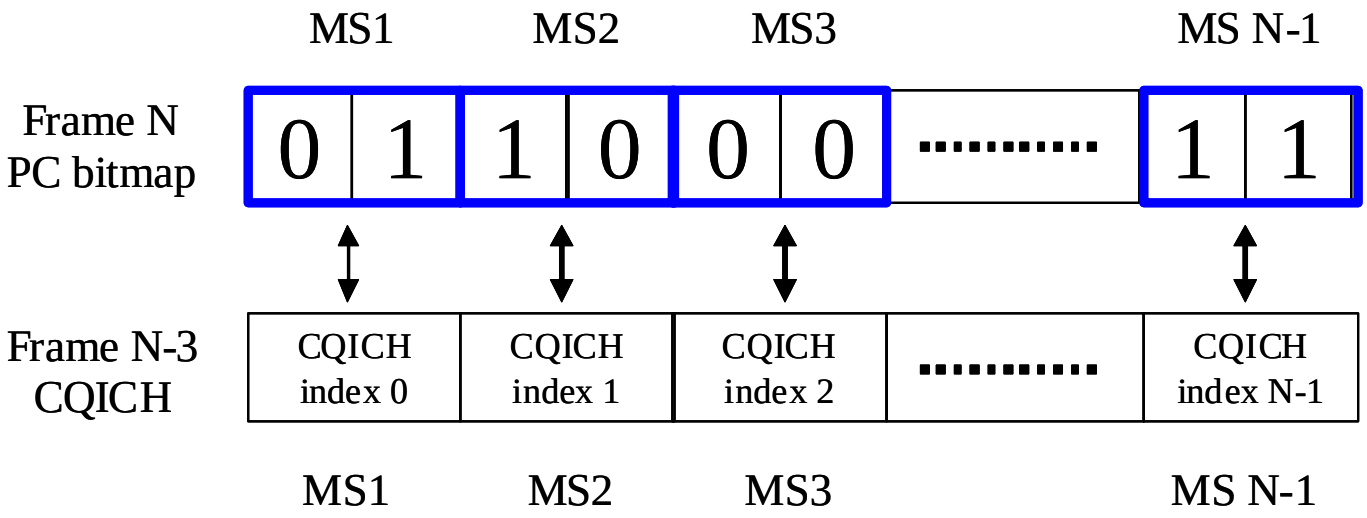
- 802.16e specifications defines the following PC messages:
  - FPC (fast power control) message (6.3.2.3.34)
  - Power Control IE (8.4.5.4.5)
  - UL-MAP Fast Tracking IE (8.4.5.4.22)
    - It is sent to a MS only when there was UL burst for the MS in earlier frame
    - It is not appropriate for CLPC
- Overhead of the current PC messages
  - 25 power control commands per frame
  - QPSK1/2 with 6 repetitions

	No. bits	Req. No. OFDM symbols
Power control IE	1100 bit	9.17 symbols
FPC message	672it	5.60 symbols

Proposed solution

Proposed power control command scheme

- For the conventional Power control messages
  - Overhead mainly comes from CID to identify a MS
- Proposed scheme
  - Use the order of CQICH in CQICH region in the previous frame



Improved overhead performance of the Proposed solution

- Simulation conditions
  - Ped-B 3km
  - 1/2-QPSK with 6 repetitions
  - 25 active MSs
  - FPC is sent only when the accumulation of power control corrections is larger than 1 dB
  - For the proposed scheme, it is assumed that all 25 power control commands are sent in every frame

	No. bits	Avg. Req. No. OFDM symbols
FPC (1dB accumulation)	265 bits	2.21 symbols
UL_PC_Bitmap_IE (B=1)	64 bits	0.53 symbols
UL_PC_Bitmap_IE (B=2)	88 bits	0.73 symbols

Proposed Text

- 8.4.5.4.29 UL_PC_Bitmap_IE

Syntax	**Size**	**Notes**
UL_PC_Bitmap_IE () {		
Extended-2 UIUC	4 bits	Fast power control = 0x0B
Length (L)	8 bits	Length in bytes
Power Control Bitmap	C*(B+1) bits	It is the sequence of power control commands with (B+1) bits each. No. of power control command(C) is Round[(8*length(L))/(B+1)] Depending on 'B', (B+1) bits power control command shall be interpreted as follows: B=0x00: 1 bit, '0':-0.5dB, '1':+0.5dB; B=0x01: 2 bits, '00':-0.5dB, '01': 0dB, '10':+0.5dB, '11':+1.0dB B=0x02: 3 bits, '000':-1.5dB ~ '111':+2.0dB, step size=0.5dB B=0x03: 4 bits, '0000':-3.5dB ~'1111':+4.0dB, step size=0.5dB
Reserved	*R bits*	Shall be set to zero R is 8*Length(L) – C*(B+1)
}		

- Power Control Bitmap
- It is the sequence of C power control commands with (B+1) bits each. The j-th power control command is a power adjustment to the MS corresponding to the MS that transmitted the i-th CQICH on CQICH region in the (N-Frame offset)-th frame. N is the frame number of the current frame carrying this UL_PC_Bitmap_IE. No. PC command bits (B) and Frame offset are sent in UCD.
- [Add the following text at the end of table 610 on page 1171]

Name	Type (1 byte)	Length	Value
Frame offset	214	1	The offset between corresponding CQI channel and current frame. 0x0 shall not be used.
No. PC command bits (B)	215	1	0x00: 1 bits, '0':-0.5dB, '1':+0.5dB; 0x01: 2 bits, '00':-0.5dB, '01': 0dB, '10':+0.5dB, '11':+1.0dB 0x02: 3 bits, '000':-1.5dB ~ '111':+2.0dB, step size=0.5dB 0x03: 4 bits, '0000':-3.5dB ~'1111':+4.0dB, step size=0.5dB 0x04~0xFF: Reserved

Conclusions

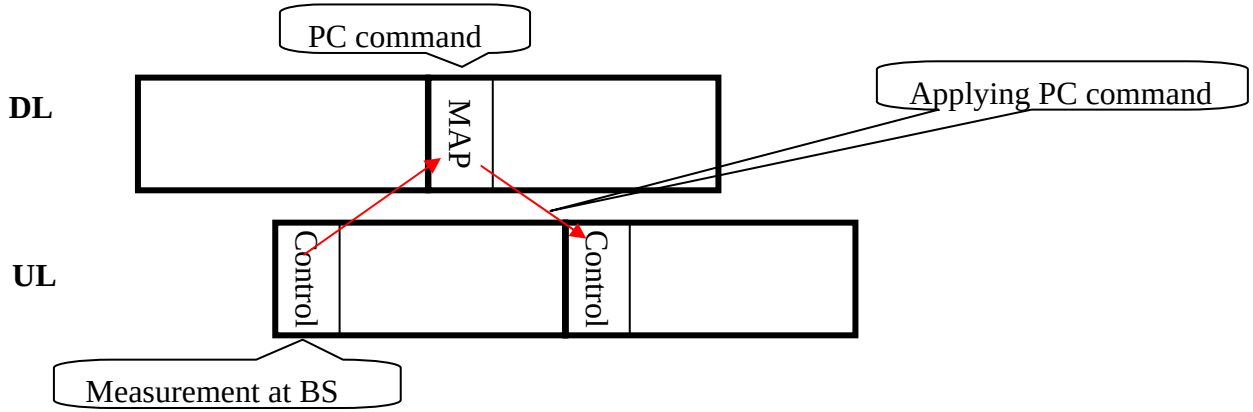
- Fast CLPC is needed for FDD
  - Fast CLPC shows gain over OLPC in FDD mode
  - For the circuit like UL, ~4dB SNR gain is observed in low speed
- Efficient power control commanding scheme is proposed
  - It does not need to identify MS explicitly
  - Instead, it uses order of CQICH in the CQI region
- The proposed scheme shows acceptable OH for CLPC
  - 0.5~1 OFDM symbol
  - 25%~33% of OH of the conventional power control scheme

Thanks!

Appendix: CLPC delay

- PC command delay for CLPC
  - Optimal timing: 1 frame delay (5ms)
  - Sub-optimal timing: 2 frame delay (10ms)

Optimal case



Suboptimal case