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Re:	This contribution is submitted in response to call for contributions from the IEEE 802.16 chair for submissions of PHY proposals for BWA, Session #7.		
Abstract	The following PHY proposal is submitted for consideration of the group developing a PHY standard for BWA systems. It is the best TDD/FSDD/FDD based approach developed by the proposing members until now. The proposing members invite all IEEE 802.16 participants to study the proposal and propose enhancements.		
Purpose	This proposal should be used as a baseline for a PHY standard for BWA		
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Policy & Procedures	Early disclosure to the Working Group of patent information that might be relevant to the standard is essential to reduce the possibility for delays in the development process and increase the likelihood that the draft publication will be approved for publication. Please notify the Chair < <u>mailto:r.b.marks@ieee.org</u> > as early as possible, in written or electronic form, of any patents (granted or under application) that may cover technology that is under consideration by or has been approved by IEEE 802.16. The Chair will disclose this notification via the IEEE 802.16 web site
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1 SCOPE

The purpose of this document is to describe the Physical Layer (PHY) parameters.

- Provide a detailed description of the PHY aspects for the Base Station and CPE
- Provide a broad description of the PHY layer functionality.
- Provide some performance requirements for a modem design implementing the proposed PHY

The Physical Layer in this proposal exploits the latest developments in modulation, encoding, and filtering to provide the most adaptive wireless communication links for BWA frequency allocations. The proposed adaptive modulation scheme permits the highest possible data throughput for a given user's location and propagation environment. The proposed PHY can operate in any known duplex mode (FDD, Half-duplex FDD and TDD). In TDD the PHY supports asymmetric traffic scenarios. The PHY allows the implementation of efficient bandwidth allocation schemes providing service with varying QoS to many users while optimizing spectral efficiency of the allocated spectrum.

- it defines and specifies the channel multiplexing;
- it defines and specifies the channel coding;
- it defines and specifies the modulation;
- it defines and specifies the radio transmission and reception;
- it defines and specifies the synchronization and control over the radio link;
- it defines and specifies the minimum performance requirements.

2 NORMATIVE REFERENCES

This PHY Specification incorporates by dated and undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references, subsequent amendments to or revisions of any of these publications apply to this PHY Specification only when incorporated in it by amendment or revision. For undated references, the latest edition of the referred publication applies.

Ref. #	Document No.	Name	Date

3 DEFINITIONS, SYMBOLS, AND ABBREVIATIONS

3.1 DEFINITIONS

Downlink	RF transmissions from the BS to the CPE
Frame	PHY basic time periodicity
Low Level Media Access Arbitration	Performs bandwidth allocation on an individual physical channel
Hyper frame	32 multiframes
High Level Media Access Arbitration	Performs bandwidth allocation and load leveling across physical channels
Modulation Transition Gap	A gap in the DL frame structure to allow for a change in modulation type.
Multiframe	16 frames
Physical Channel	A frequency, sector pair
Physical Slot (PS)	The smallest subdivision of the PHY layer made of 4 symbols. PSs are used for Radio Time Management.
PHY Information Element (PI)	One FEC encoded block of information with no additional shortening or zero padding.
Reed Solomon coding	FEC encoding scheme where data bits are converted into 8-bit symbols, grouped into blocks and parity bits calculated on these blocks. An (m/n) RS block is made of m total symbols, n data symbols, and m-n parity symbols.
Reed Solomon coding TC Data Unit (TDU)	grouped into blocks and parity bits calculated on these blocks. An (m/n) RS
-	grouped into blocks and parity bits calculated on these blocks. An (m/n) RS block is made of m total symbols, n data symbols, and m-n parity symbols.
TC Data Unit (TDU)	grouped into blocks and parity bits calculated on these blocks. An (m/n) RS block is made of m total symbols, n data symbols, and m-n parity symbols. A data block used for transport between the MAC and PHY layers A duplex scheme where the UL and DL transmissions alternate in time while
TC Data Unit (TDU) Time Division Duplex (TDD) Frequency Division Duplex	grouped into blocks and parity bits calculated on these blocks. An (m/n) RS block is made of m total symbols, n data symbols, and m-n parity symbols. A data block used for transport between the MAC and PHY layers A duplex scheme where the UL and DL transmissions alternate in time while sharing the same RF channel A duplex scheme where the UL and DL transmissions use different RF
TC Data Unit (TDU) Time Division Duplex (TDD) Frequency Division Duplex (FDD) Frequency Switched Division	grouped into blocks and parity bits calculated on these blocks. An (m/n) RS block is made of m total symbols, n data symbols, and m-n parity symbols. A data block used for transport between the MAC and PHY layers A duplex scheme where the UL and DL transmissions alternate in time while sharing the same RF channel A duplex scheme where the UL and DL transmissions use different RF channels A duplex scheme where the UL and DL transmissions use different RF
TC Data Unit (TDU) Time Division Duplex (TDD) Frequency Division Duplex (FDD) Frequency Switched Division Duplex (FSDD)	grouped into blocks and parity bits calculated on these blocks. An (m/n) RS block is made of m total symbols, n data symbols, and m-n parity symbols. A data block used for transport between the MAC and PHY layers A duplex scheme where the UL and DL transmissions alternate in time while sharing the same RF channel A duplex scheme where the UL and DL transmissions use different RF channels A duplex scheme where the UL and DL transmissions use different RF channels A duplex scheme where the UL and DL transmissions use different RF channels A duplex scheme where the UL and DL transmissions use different RF channels but users do not transmit and receive instantaneously A gap in the frame structure to allow for the transition from DL to UL

3.2 SYMBOLS AND ABBREVIATIONS

- BCB Bandwidth Contention Burst
- BCCH Bandwidth Request Control CHannel
- BS Base Station
- SYSTEM System

CPE	Customer Premise Equipment
DL	Downlink
DLB	Downlink Burst
DQM	Digital Quadrature Mixing
FEC	Forward Error Correction
LL-MAA	Low Level Media Access Arbitration
HL-MAA	High Level Media Access Arbitration
LMDS	Local Multi-point Distribution Service
MAC	Media Access Control
MCCH	MAC Control CHannel
MMDS	Multi-Megabit Distribution Service
PCCH	PHY Control CHannel
PHY	Physical Layer
PI	PHY Information Element
PS	Physical Slots
QAM	Quadrature Amplitude Modulation
RCB	Registration Contention Burst
RCCH	Registration Request Control CHannel
RS	FEC
RTG	Rx/Tx Transmission Gap
тс	Transmission Control
TDU	TC Data Unit
TTG	Tx/Rx Transmission Gap
UDB	Uplink Data Burst
UL	Uplink

4 PHY OVERVIEW

This section is an introduction to the Physical Layer (PHY) aspects of a IEEE 802.16.1 air interface. It consists of a general description of the organization of the PHY radio-related functions with reference to the sections where each part is specified in detail.

4.1 INTRODUCTION

This section is an introduction to the radio aspects of a system using the proposed PHY. It consists of a general description of the organization of the radio-related functions with reference to the sections where each part is specified in detail. Furthermore, it introduces the reference configuration that will be used throughout this PHY proposal.

4.2 **REFERENCE CONFIGURATION**

For the purpose of elaborating the specification of the radio-related functions, a reference configuration of the transmission chain is used as shown in Figure 4-1.

NOTE: Only the transmission part is specified, the receiver being specified via overall performance requirements.

With reference to this configuration, the radio sections address the following functional units:

- Section 4: PHY Overview (this Section)
- Section 5: Multiple Access and Channel Multiplexing;
- Section 6: Channel Coding, Interleaving, and Scrambling;
- Clause 7: Modulation;
- Section 8: RF Transmission and Reception
- Section 9: Radio Sub-system Control and Synchronization;
- Clause 10: Minimum Performance;

This reference configuration also defines a number of points of vocabulary in relation to the names of bits at different levels in the configuration.



Figure 4-1 Reference Configuration

4.3 ERROR CONTROL SCHEMES

The error control scheme used in the proposed is based on a Reed Solomon block code concatenated with a bit wise parity check. The error control scheme is described in detail in Section6.2.2.1.

4.4 BAUD RATES AND CHANNEL BANDWIDTH

This PHY proposal supports different spectrum arrangements as explained in Chapter 5. For **simplification** only, we consider the US LMDS case of a **25 MHz RF channel** scheme. The recommended baud rate for operation is **20 MBaud**. These parameters hold regardless of the duplex scheme. In the case of FDD, 2 RF channels would be used, one for uplink and one for downlink, while in the case of TDD only one channel is used by sharing it in time between uplink and downlink.

4.5 MULTIPLE ACCESS AND TIME SLOT STRUCTURE

The access scheme for the uplink is TDMA with dynamically sized allocations. The downlink is TDM (Time Division Multiplexed) hence all the data of different users served by the RF channel are multiplexed in time. An optional mode of TDMA on the downlink is supported as well. In this option a user is pointed to the exact location of its data portion of the downlink similar to the way it is pointed to exact location to use the uplink.

The following subsections briefly introduce the structures of hyper-frame, multi-frame, frame, timeslot, and burst, as well as the mapping of the logical channels onto the physical channels. The appropriate specifications are found in Section 5.

4.5.1 Duplexing

The proposed PHY utilizes either FDD or TDD schemes. In the case of FDD both uplink and downlink use an identical framing structure and both are synchronized one to each other. In the case of TDD a frame is sub divided into 2 subframes, one for downlink and one for uplink. The duration of the downlink and uplink subframes within a frame may vary yet the total frame size is constant. Allowing users to transmit bursts on the uplink and receive bursts on the downlink when reception and transmission periods do not overlap supports frequency Switched Division Duplex.

4.5.2 Frames, Multi-frames, and Hyper-frames

For the LMDS case a frame has duration of 1 mSec and consists of 5,000 Physical Slots (PSs). Each PS has a duration of 200 nSec.

16 frames consist of one multi-frame, which has duration of 16 ms.

The hyper-frame level defines the top-level frame hierarchy. One hyperframe is subdivided into 32 multiframes and has a duration of 512 ms.

4.6 LOGICAL CHANNELS

The radio subsystem provides a certain number of logical channels as defined in Section 5. The logical channels represent the interface between the protocol and the radio.

Logical Channel	Direc- tion	Description
PCCH	DL	PHY Control Channel
MCCH	DL	MAC Control Channel
DL TCH4	DL	Downlink Traffic Channel, QPSK
DL TCH16	DL	Downlink Traffic Channel, QAM-16
DL TCH64	DL	Downlink Traffic Channel, QAM-64
TTG		Transmit / Receive Transition Gap
RCCH	UL	Registration Request Control Channel
BCCH	UL	Bandwidth Request Control Channel
UL TCH4	UL	Uplink Traffic Channel, QAM-4 or CQPSK
UL TCH16	UL	Uplink Traffic Channel, QAM-16
UL TCH64	UL	Uplink Traffic Channel, QAM-64
CTG	UL	CPE Transition Gap
RTG		Receive / Transmit Transition Gap

 Table 4-1 Mapping of Logical Channel into Physical Channels

4.7 CODING, INTERLEAVING, AND SCRAMBLING

The coding, interleaving, and scrambling schemes associated with each logical channel shall be as specified in Section 6.

4.8 MODULATION AND SLAM

The modulation scheme proposed is multi level QAM. The levels supported are QAM-4 (QPSK), QAM-16 and QAM-64. The pulse shape used is a root-raised cosine with a roll-off factor of 0.25. Therefore for a 25 MHz channel, the modulation rate is 20 MS/s.

This modulation scheme is supported by both the uplink and the downlink. For the uplink a reduced cost terminal option is supported by using CQPSK which is a constant envelope modulation scheme providing high power efficiency. The modulation rate is 3/4 of the QAM-4 scheme, that is 30 Mbps/s. More information on this issue is found mainly in chapter 7.

The PHY supports subscriber level adaptive modulation (SLAM) hence the modulation level for each subscriber is set according to its link conditions, both for the uplink and the downlink independently. In the case of the reduced cost terminal, the uplink modulation is fixed as it is not designed for supporting multi-level QAM transmissions. This type of terminal can support SLAM on the downlink only.

Base stations must support both uplink modulation options but will use only one of the options for a given frequency carrier per sector.

4.9 TRANSMISSION AND RECEPTION

The modulated stream is transmitted on a RF carrier.

The specific RF channels, together with the requirements on the transmitter and the receiver characteristics are specified in Section 5.

The PHY may utilize polarization diversity at the antenna complex for increasing deployment capacity or reducing interference.

4.10 OTHER RADIO-RELATED FUNCTIONS

Transmission involves other functions. These functions, which may necessitate the handling of specific protocols between BS and CPE, are the radio subsystem synchronization and the radio subsystem link control.

The synchronization incorporates:

- frequency and time acquisition by the CPE receiver
- adjustment of the time base of the CPE (ranging).

The requirements on synchronization are specified in Section 6.

The radio link adaptive power control adjusts the RF transmit power, in order to ensure that the required quality of transmission is achieved with the least possible radiated power. This function is managed by the CPE during the initial access, and by the CPE and BS during operational use. Adaptive power control provides for the reduction of interference levels.

4.11 PERFORMANCE

Section 10 defines the minimum performance parameters for the proposed PHY.

5 MULTIPLE ACCESS AND CHANNEL MULTIPLEXING

5.1 INTRODUCTION

This section defines the physical channels of the radio sub-system required to support the logical channels. It includes a description of the logical channels and the definitions of TDMA frames, physical slots and bursts. A Transmission Convergence (TC) Layer has been defined for the mapping of MAC channels to PHY layer resources. This section defines the interaction of the PHY layer and the TC sub-layer.

5.2 THE PHYSICAL RESOURCE

5.2.1 General

The physical resource available to the radio sub-system is an allocation of part of the radio spectrum. This resource is partitioned in time only. The total available spectrum for deployment shall be partitioned by RF channels divided into bands as defined in Section 8. Timeslots and TDMA frames as defined in this subsection shall partition time.

The access scheme shall be TDMA. The TDMA structure shall be composed of hyper-frames, multi-frames, frames, physical slots and symbols.

5.2.2 RF channels

A RF channel is defined as a specified portion of the RF spectrum. In the case of FDD, there is actually a pair of RF carriers of equal bandwidth, one for uplink and one for downlink communications. In the case of TDD a single channel is used by sharing it in time by uplink and downlink. The Downlink (DL) is defined as RF bursts used in the BS to CPE direction. The Uplink (UL) is defined as RF bursts used in the CPE to BS direction.

The PHY layer is designed around a 1 mSec time base frame. Each frame is segmented into 5,000 Physical Slots (PSs). See Figure 5-1 for an illustration of a frame. Each Physical Slot is defined as a 200 nSec time element. A PS contains 4 Symbols in the case of a 20 MBaud QAM transmission (50 nSec per symbol) or 6 bits in the case of a CQPSK transmission.

5.2.3 Framing and Formatting

Downlink frames are structured according to modulation type into four groups: QPSK Frame Control Header, QPSK data block, QAM-16 data block, and QAM-64 data block. This structure is detailed in Section 5.4.2.1. A downlink TDMA option (similar to the uplink) where individual user data is not multiplexed with other user data is supported as well.

Uplink frames are structured according to modulation type into five groups: QPSK Registration Request Contention slot, QPSK Bandwidth Request Contention slot, QPSK data bursts, QAM-16 data bursts, and QAM-64 data bursts. Each burst is separated by a transition gap for ramping down and ramping up transmissions. This structure is detailed in Section 5.4.2.1. In the case of a reduced cost terminal CQPSK is used for all burst types.

Addressing a specific starting point for a user uplink transmission is done by reference to a PS As pointed earlier the PS granularity is required to simplify radio time management over the frame.

The FEC output bits are converted to modulation symbols according to the modulation scheme chosen. Although the FEC operation is block oriented (requires a specific information size to operate on) there would be cases where the FEC operates on a shorter block due to efficiency. In these cases, the information before the FEC operation is effectively prefixed with zero byte padding. The resulting FEC operation would contain a zero byte prefix padding which are discarded for transmission and are padded back at the receiver.

5.2.4 FDD

In this mode of operation the downlink and uplink are using 2 different carrier frequencies. Both carriers are equal in channel bandwidth *and* instantaneous baud rate. The frequency separation between carriers is set either according to the target spectrum regulations or to some value sufficient for complying with radio channel transmit/receive isolation and desensitization requirements. In the time domain both uplink and downlink are frame *synchronized*.

A subscriber capable of full duplex FDD operation, meaning it is capable of transmitting and receiving at the same instant, imposes no restriction on the base station controller regarding its uplink bandwidth allocation management. On the other hand, a subscriber that is limited to Frequency Switched Division Duplex operation imposes a restriction on such a controller not to allocate uplink bandwidth for the subscriber, which may force it to instantaneously transmit and receive. It is mandatory that both types of subscribers could co-exist in a FDD deployment, meaning that radio channels could address both type of subscribers instantaneously.

The following figure describes the basics of the FDD and FSDD based operation. Frames are either even numbered or odd numbered. A subscriber limited to FSDD operation is designated to operate either on even frames or odd frames. Those that are receiving downlink on even frames are using odd frames for uplink and vice versa. A user that is capable of full duplex FDD ignores the even/odd structure and may utilize the system on both even and odd frames.



In order to increase statistical gain a user may change its even-odd frame relationship according to traffic requirements. When a user has no uplink bandwidth it is required to receive all frames. When bandwidth is being allocated for it then the user limits itself by the frame assigning its

bandwidth. If the frame assigning bandwidth on the downlink is even numbered than its uplink frames would be odd numbered and vice versa.

5.2.5 TDD and Supporting Varying Traffic Asymmetry Conditions

In the case of TDD, uplink and downlink share the same frequency in time. A TDD frame has a 1 mS duration and contains one downlink and one uplink subframe. Each frame contains 5,000 PS as shown in Figure 5-1. The TDD framing is adaptive in that the number of PS allocated to downlink versus uplink can vary. The split between uplink and downlink is a system parameter and is controlled at higher layers within the system.



Figure 5-1 Frame Structure

5.2.5.1 Tx / Rx Transition Gap (TTG)

The TTG is a gap between the Downlink burst and the Uplink burst. This gap allows time for the BS to switch from transmit mode to receive mode and CPEs to switch from receive mode to transmit mode. During this gap, BS and CPE are not transmitting modulated data but simply allowing the BS transmitter carrier to ramp down, the Tx / RX antenna switch to actuate, and the BS receiver section to activate. After the TTG, the BS receiver will look for the first symbols of QPSK modulated data in the uplink burst. The TTG has a variable duration which is an integer number of PSs. The TTG starts on a PS boundary.

5.2.5.2 Rx / Tx Transition Gap (RTG)

The RTG is a gap between the Uplink burst and the Downlink burst. This gap allows time for the BS to switch from receive transmit mode to transmit mode and CPEs to switch from transmit mode to receive mode. During this gap, BS and CPE are not transmitting modulated data but simply allowing the BS transmitter carrier to ramp up, the Tx / RX antenna switch to actuate, and the CPE receiver sections to activate. After the RTG, the CPE receivers will look for the first symbols of QPSK modulated data in the downlink burst. The RTG is an integer number of PSs. The RTG starts on a PS boundary.

5.2.5.3 CPE Transition Gap (CTG)

The CTG is a gap between Uplink bursts. This gap allows time for one CPE to ramp down its transmission while the next CPE is ramping up its transmission. The CTG consists of an integer number of physical slots. The CTG starts on a PS boundary.

5.3 LOGICAL CHANNELS

A logical channel is defined as a logical communication pathway between two or more parties. The logical channels represent the interface between the protocol and the radio subsystem.

The definition of the logical channels supported by the radio subsystem is given below.

5.3.1 Logical channels hierarchy

There are two categories of logical channels: the traffic channels carrying speech or data information and the control channels carrying signaling messages. The logical channels supported by the PHY and MAC are described here with their hierarchical relationship.

5.3.2 Traffic channels

The traffic channels shall carry user information. Three traffic channels are defined for four different modulation types. If the propagation environment allows, the BS assigns higher modulation types to CPEs on an individual basis independently on uplink and downlink. The Traffic CHannels are defined as follows:

- TCH4 QPSK or CQPSK (Uplink, reduced cost terminal) data;
- TCH16 QAM-16 data;
- TCH64 QAM-64 data.

The length of each type of traffic channel in a downlink burst and an uplink burst is dynamically assigned by the BS. A map of the assignments is included in the MAC Control Channel that is read and interpreted by the CPEs.

The downlink data sections are used for transmitting data and control messages to the CPEs. The uplink data sections are used for transmitting data and control messages to the BS. This data is always FEC coded and is transmitted at the current operating modulation.

The downlink frame can operate either in a TDM mode or in TDMA mode. In the TDM mode channels are grouped by modulation type. The PHY Control portion of the Frame Control Header contains fields stating the PSs at which modulation will change. Data is transmitted in modulation order QPSK, followed by QAM-16, followed by QAM-64. The structure of the data sections are the same, the only difference is the modulation type.

If the downlink data does not fill the entire downlink subframe, the downlink subframe is padded with fill data (0x55). If one or more TC data units (TDUs) remain to be filled, the MAC performs the fill on a specific connection ID. If less than one TDU remains to be filled, the TC performs the fill.

In the case of FSDD filling is replaced by transmitter shut-down in order to allow parallel uplink allocations and preferably a TDMA burst mode of operation is used in this case for the downlink.

Within the uplink subframe, bursts are of the modulation type assigned to the CPE. The first portion of each uplink burst is a preamble, followed by MAC data from the CPE. The Uplink Map

in the previous downlink burst regulates the length of the data section. If the uplink data does not fill the entire given uplink burst allocation, the burst is padded with fill data (0x55). If one or more TDUs remain to be filled, the MAC performs the fill on a specific connection ID. If less than one TDU remains to be filled, the TC performs the fill or shortening.

5.3.2.1 TCH4

The TCH4 QPSK data channels transport data at a rate of 2 bits per symbol.

5.3.2.1.1 QPSK Downlink Data

On the downlink, the most robust modulation scheme used is QAM-4 (QPSK). Data is transported at a rate of 2 bits per symbol.

5.3.2.1.2 QPSK/CQPSK Uplink Data

On the uplink, the most robust modulation scheme used is QAM-4 (QPSK). Data is transported at a rate of 2 bits per symbol.

In the case of the reduced cost terminal CQPSK transports data at a rate of 2 bits per symbol yet the baud rate is 3/4 of the one used for regular QAM hence the effective transport data rate is 3/2 bits per symbol.

5.3.2.2 QAM-16 Data (TCH16)

The TCH16 QAM-16 data channels transport data at a rate of 4 bits per symbol.

5.3.2.3 QAM-64 Data (TCH64)

The TCH64 QAM-64 data channels transport data at a rate of 6 bits per symbol.

5.3.3 Control CHannels (CCH)

5.3.3.1 General

The CCH shall carry signaling messages. Four categories of control channels are defined:

- PHY Control CHannel (PCCH);
- MAC Control CHannel (MCCH);
- Registration Request CHannel (RCCH);
- Bandwidth Request CHannel (BCCH).

The downlink burst has two categories of control channel defined:

- PHY Control CHannel (PCCH);
- MAC Control CHannel (MCCH).

These two channels are the first two sections of the DL burst and are not separate bursts from the DL traffic channels.

The uplink burst has two categories of control channel defined:

- Registration Request CHannel (RCCH);
- Bandwidth Request CHannel (BCCH).

Each message on these two channels is a separate burst from the UL traffic channels. Each channel can support multiple bursts per frame from multiple CPEs.

5.3.3.2 PHY Control CHannel (PCCH)

The PCCH occupies the first bytes of the first TDU in the downlink burst following the preamble.

The PHY Control portion of the downlink subframe is used for physical information destined for all CPEs. The PHY Control information is FEC encoded. The information transmitted in this section is always transmitted in QPSK.

5.3.3.3 MAC Control CHannel (MCCH)

The MAC Control portion of the downlink subframe is used for MAC messages destined for multiple CPEs. For information directed at an individual CPE, MAC messages are transmitted in the established control connection at the operating modulation of the CPE to minimize bandwidth usage. The MAC Control messages are FEC encoded. The information transmitted in this section is always transmitted in QPSK.

5.3.3.4 Registration Request Contention CHannel (RCCH)

Periodically, a portion of the uplink burst is allocated for registration request message contention. The Registration Request Contention Channel allows unregistered users a portion of the uplink frame to attempt transmission of registration requests without interfering with ongoing traffic. Registration request messages transmitted in the Registration Request Contention Channel are transmitted using QPSK modulation (or CQPSK in the case of the reduced cost terminal).

For more details of the Registration Request Contention slot, see Section 5.4.2.2.2.1.

5.3.3.5 Bandwidth Request Contention CHannel (BCCH)

Periodically, a portion of the uplink burst is allocated for bandwidth or connection requests. The Bandwidth Request Contention Channel allows registered users a portion of the uplink to attempt transmission of bandwidth requests without interfering with ongoing traffic. Bandwidth request messages transmitted in the Bandwidth Request Contention Channel are transmitted using QPSK modulation (or CQPSK in the case of the reduced cost terminal).

For more details of the Registration Request Contention slot, see Section 5.4.2.2.2.2.

5.4 Types of Physical Channels

5.4.1 General

A physical channel is defined by a burst on a radio carrier frequency. There shall be one physical channel per radio frequency/burst.

5.4.2 Types of Physical Channels

Three types of physical channels are defined:

- Downlink subframe burst
- Uplink subframe Control Channel bursts
- Uplink subframe Traffic Channel bursts

5.4.2.1 Downlink Burst

The structure of the downlink burst used by the BS to transmit to the CPEs is shown in Figure 5-2. This burst structure defines the single, downlink physical channel. It starts with a Frame Control Header that is always transmitted in QPSK. This frame header contains a preamble used by the PHY for synchronization and equalization. It also contains control sections for both the PHY and the MAC. Within the downlink subframe, transmissions are grouped by modulation type. Preambles are not FEC. There is a Tx/Rx Transmission Gap (TTG) separating the downlink subframe from the uplink subframe in the case of TDD.

5.4.2.1.1 Downlink Traffic Channels

The downlink traffic channels are used for transmitting data and control messages to the CPEs. There are 2 options supported by the downlink traffic channels: TDM and TDMA. While using the TDM option, each CPE continuously receives the entire downlink burst. The CPE decodes the data in the DL burst and looks for MAC headers indicating data for that CPE. While using the TDMA option, an allocation map similar to the uplink allocation map (for scheduled uplink transmissions) is transmitted in the frame control header. This allows an individual CPE to decode a specific portion of the downlink without the need to decode the whole DL burst. In this particular case, each transmission associated with different CPEs is required to start with a short preamble for phase re-synchronization. For TDD the preferred option is TDM and for FSDD the preferred option is TDMA.

This data is always FEC coded and is transmitted at the current operating modulation of the individual CPE. Data is transmitted in modulation order QPSK, followed by QAM-16, followed by QAM-64 in the TDM case. The PHY Control portion of the Frame Control Header contains fields stating the PS at which modulation will change.



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Figure 5-2 Downlink Subframe Structure

5.4.2.2 Uplink Bursts

The structure of the uplink subframe used by the CPEs to transmit to the BS is shown in Figure 5-3. There are three main classes of MAC/TC messages transmitted by the CPEs during the uplink frame:

- Those that are transmitted in contention slots reserved for station registration;
- Those that are transmitted in contention slots reserved for response to multicast and broadcast polls for bandwidth needs;
- Those that are transmitted in bandwidth specifically allocated to individual CPEs.

The bandwidth allocated for contention slots is grouped together and is transmitted using QPSK /CQPSK modulation. The remaining, scheduled bandwidth is grouped by CPE. During its scheduled bandwidth, a CPE transmits with a fixed modulation, determined by the effects of environmental factors on transmission to and from that CPE. CPE Transition Gaps (CTG) separate the transmissions of the various CPEs during the uplink subframe.

5.4.2.2.1 CPE Transition Gaps (CTGs)

CPE Transition Gaps (CTG) separate the transmissions of the various CPEs during the uplink subframe. The CTG time length is an integer number of PSs sufficient for preamble (long) and ramp up time. The transmitting CPE transmits the preamble at the ending portion of the CTG ending where the CTG ends allowing the BS to synchronize to the new CPE. CTGs are considered part of the subsequent burst.





5.4.2.2.2 Uplink Control Channels

5.4.2.2.2.1 Registration Contention Slots

A portion of the uplink bandwidth is periodically be allocated for registration contention slots. Registration contention slots are used to allow CPEs to register with the BS and to perform ranging. CPEs wishing to register and range must have acquired downlink synchronization with the BS, but do not know their Tx timing advance or an appropriate power level. Additionally, they do not yet have a basic connection ID assigned for direct communication with the BS. The registration contention slots allow access under these conditions, allowing CPEs to finalize their uplink physical synchronization with the BS and to establish a logical connection for control communication.

Due to propagation delays, the registration contention bursts from the CPEs are not aligned to the symbols or PSs of the downlink burst. The BS must use a sliding window to accurately detect the preamble of each request burst. The window is incremented in ½ symbol increments.

Multiple CPEs may transmit in the registration contention period simultaneously, potentially causing collisions. When a collision occurs, the BS does not respond. If the BS successfully receives a registration message from a CPE, it responds with a registration results message in the QPSK portion of the downlink subframe.

The round trip delay for a 5 km cell causes a CPE with no Tx timing advance to transmit up to 150 PSs late, not including delays through the modem. Therefore, the minimum length of the registration contention period is 150 + modem delay (in integer number of PSs) + n PS, where n is the number of PS required to transmit a registration or ranging message. More PSs may be allocated to reduce the likelihood of collision or to allow larger cells. Figure 5-4 shows the relationship between the registration contention slot window and the various parameters

governing the timing of messages within the window. The registration contention slots must preserve PS boundary.



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5.4.2.2.2.2 Bandwidth Request Contention Slots

A portion of the uplink bandwidth is periodically allocated for bandwidth or connection requests. Since a CPE must be registered and have achieved uplink synchronization with the BS before it is allowed to request bandwidth, there is no Tx time uncertainty to be allowed for in the length of the bandwidth request contention period. Therefore the bandwidth request contention period requires some number of PSs to transmit the request command, plus a CTG. As with registration requests, if a collision occurs, the BS does not respond. If the BS successfully receives a bandwidth request message, it responds by allocating the CPE (additional) bandwidth in the Uplink Map. Polling and piggybacking help to minimize the need to use bandwidth request contention slots.

5.4.2.2.3 Scheduled Uplink Traffic Channels

Scheduled uplink traffic bandwidth is allocated to specific CPEs for the transmission of control messages and user data. These scheduled bursts are the Traffic Channels (TCHs) for the CPEs. The CPE UL bursts are preferably ordered by modulation. The bandwidth is requested by the CPE and granted by the BS. All bandwidth within a given frame, allocated to an individual CPE, is grouped into a contiguous block. The CTG PS count is included in the allocation to the CPE in the Uplink Map. The CPE transmits a preamble located at the CTG end. The preamble is not part of the FEC process. The TDU packets transmitted are always

FEC coded. As indicated previously, the pointer for the beginning of a scheduled transmission uses a PS number.

5.4.2.2.4 Scheduled Downlink Traffic Channels

This mode of downlink operation (as mentioned previously) is advantageous in the case of supporting FSDD allowing the scheduling of individual users on the downlink. The reasoning for this approach is minimizing latency and controlling efficiently and tightly the allocation process for both uplink and downlink together as in the FSDD case users are forbidden to transmit and receive at the same instant.

Therefore scheduled downlink traffic bandwidth is allocated to specific CPEs for the transmission of control messages and user data. All bandwidth within a given frame, allocated to an individual CPE, is grouped into a contiguous block. In the downlink it is assumed that the user is capable of listening to the control portion at the beginning of the frame hence only a short preamble is required prior to the scheduled downlink transmission of an individual CPE, mainly for phase sync. In this case only a short 12 symbol preamble is used. There is no requirement for ramping power as downlink is assumed to be continuous within its subframe.

The existence of a downlink allocation map is identified in the control portion of each frame. There could be both TDM and TDMA downlink assignments. In this case, the TDM portion with all its modulation schemes would be transmitted first. In the case of FSDD, if a downlink map exists and the map does not address a specific user then this user is required to receive the TDM downlink portion if it exists. Only if the user has its uplink scheduled overlapping the TDM portion, it can assume that the base station MAC has not multiplexed any information for the user on the TDM portion and it can skip to the next frame.

5.4.3 Bursts

5.4.3.1 General

A burst is a period of RF carrier that is modulated by a data stream. A burst therefore represents the physical content of a timeslot or subslot.

The description of a physical channel is made in terms of physical slots (PSs) and symbols. As described in section 5.2.2, each Physical Slot is defined as 3 Symbols for the QAM based modulation and 5 bits in the case of CQPSK.

In general, the FEC is programmed to work on a N byte block prior to encoding. The FEC output is defined as the PHY Information Element (PI). Each PI provides the payload to the TC for transport of MAC messages, control information, and data. The TC provides to the MAC a data block defined as a TC Data Unit (TDU). The modulation within the frame may vary, and determines the number of PS and symbols required for transmission.

A shortened PI is supported as well by zero padding prior to FEC and discarding the pads at transmission. The receiver pads back the discarded zeros prior to decoding.

5.4.3.2 Modulation symbol numbering

A PS has a duration of 150 nSec. In the case of QAM a PS shall be divided into 3 modulation symbol durations, each one with a duration of 50 nSec. A particular modulation symbol within a burst shall be referenced by a Symbol Number (SN), with the first modulation symbol numbered SN0 and the last modulation symbol numbered SNmax.

In the case of the uplink when CQPSK is used, a PS maintains the same time length (150 nSec) yet contains only 5 bits each one with a duration of 30 nSec.

Different types of bursts are defined, having different durations.

5.4.3.3 Modulation bit numbering

A particular modulation bit within a burst shall be referenced by a Bit Number (BN), with the first modulation bit numbered BN0 and the last modulation bit numbered BNmax.

At the modulator the modulation bits shall be grouped into groups of one, two, four, or six depending upon the modulation type (CQPSK, QPSK, QAM-16, or QAM-64) and each group shall be converted into one modulation symbol as described in section 7.

5.4.3.4 Burst timing

The symbol time is defined as the instant at which the transmitted symbol waveform is at a maximum for the symbol of interest. The beginning of a symbol is defined as one half a symbol period before the instant at which the transmitted symbol waveform is at a maximum for the symbol of interest.

5.4.3.5 Burst Preambles

Table 5-1 defines the preambles for the different burst types. The preamble is always at the first part of a burst. QPSK, CQPSK and QAM-16 use 24 symbol preambles. QAM-64 uses a 48 symbol preamble. In the case of the TDMA mode on a downlink, user bursts are transmitted with a shortened preamble of 12 symbols for QPSK, QAM-16 and QAM-64.

Burst type	Preamble Type	Modulation Type
Downlink burst, Frame begin	1	QPSK
Uplink Registration Request burst	1	QPSK/CQPSK
Uplink Bandwidth Request burst	1	QPSK/CQPSK
Uplink QPSK Data burst	2	QPSK/CQPSK
Uplink QAM-16 Data burst	3	QAM-16
Uplink QAM-64 Data burst	4	QAM-64
Downlink TDMA burst	5	QPSK

 Table 5-1
 Burst Preamble Types

5.4.3.5.1 Burst Preamble 1

Table 5-2 defines the bit sequence for burst preamble 1 (TBD).

Symbol	I	Q	B(1)	B(2)
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				
17				
18				
19				
20				
21				
22				
23				
24				
25				

Table	5-2	Burst	Preamble 1
	-		

5.4.3.5.2 Burst Preamble 2

Table 5-4 defines the bit sequence for burst preamble 2 (TBD).

Symbol	I	Q	B(1)	B(2)
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				
17				
18				
19				
20				
21				
22				
23				
24				

Table 5-4 Burst Preamble 2

5.4.3.5.3 Burst Preamble 3

Table 5-5 defines the bit sequence for burst preamble 3 (TBD).

Symbol	I	Q	B(1)	B(2)	B(3)	B(4)
1						
2						
3						
4						
5						
6						
7						
8						
9						
10						
11						
12						
13						
14						
15						
16						
17						
18						
19						
20						
21						
22						
23						
24						

Table 5-5 Burst Preamble 3

5.4.3.5.4 Burst Preamble 4

Table 5-6 defines the bit sequence for burst preamble 4 (TBD).

 Table 5-6
 Burst Preamble 4

Symbol	I	Q	B(1)	B(2)	B(3)	B(4)	B(5)	B(6)
1								

Symbol	I	Q	B(1)	B(2)	B(3)	B(4)	B(5)	B(6)
2								
3								
4								
5								
6								
7								
8								
9								
10								
11								
12								
13								
14								
15								
16								
17								
18								
19								
20								
45								
46								
47								
48								

5.4.3.5.5 Burst Preamble 5

Table 5-7 defines the bit sequence for burst preamble 5 (TBD).

Symbol	I	Q	B(1)	B(2)
1				
2				
3				
4				

Table 5-7 Burst Preamble 1

Symbol	I	Q	B(1)	B(2)
5				
6				
7				
8				
9				
10				
11				
12				

5.4.4 Types of bursts

5.4.4.1 General

8 types of bursts shall exist in the system. Figure 5-5 summarizes the description of the bursts and their timing with respect to the timeslot.



Figure 5-5 Types of Bursts

Burst type	Channel ID	Logical Format	Definition
Downlink	DLB	Preamble, PCCH, MCCH DL TCH4, DL TCH16, DL TCH64	subsection 5.4.4.2
Uplink Registration Contention	RCB	Preamble, RCCH	subsection 5.4.4.3
Uplink Bandwidth Request Contention	BCB	Preamble, BCCH	subsection 5.4.4.4
Uplink Scheduled Traffic, QPSK/CQPSK	UDB4	Preamble, UL TCH4	subsection 5.4.4.5
Uplink Scheduled Traffic, QAM-16	UDB16	Preamble, UL TCH16	subsection 5.4.4.5
Uplink Scheduled Traffic, QAM-64	UDB64	Preamble, UL TCH64	subsection 5.4.4.5

Table 5-3 Burst Types

5.4.4.2 Downlink Burst (DLB), TDM and TDMA modes

The downlink burst is composed of up to three sections: the QPSK section, the QAM-16 section, and the QAM-64 section. In the case of the TDMA option on the downlink each user data in the TCH logical channels are prefixed with a short preamble. If both TDM and TDMA options exist on a specific carrier, then the TDM traffic is transmitted first similar to the situation of being the only option supported. If only TDMA is supported there is no particular need to preserve the modulation order with the exception that PCCH and MCCH control channels are transmitted first at the beginning of each frame using QPSK. The following sections address the TDM mode.

5.4.4.2.1 QPSK

Every downlink burst always contains a QPSK section. This section contains at minimum the preamble, the PCCH and MCCH control channels. If present, the TDM stream using TCH4 QPSK user data section is transmitted immediately afterwards.

The preamble, PCCH, MCCH, and TCH4 logical channels are concatenated into one continuous QPSK symbol stream. The preamble shall be as defined in Section 5.4.3.5. The PHY Control message and MAC Control message are defined in the MAC Specification.

Downlink traffic packets consist of concatenated MAC control messages and MAC data packets.

5.4.4.2.2 QAM-16

The QAM-16 section is used to transport CPE user data with QAM-16 modulation. Downlink traffic packets consist of concatenated MAC control messages and MAC data packets. If QAM-16 data is present in the frame, the TCH16 channel will follow the TCH4 channel.

5.4.4.2.3 QAM-64

The QAM-64 section is used to transport CPE user data with QAM-64 modulation. Downlink traffic packets consist of concatenated MAC control messages and MAC data packets. If QAM-64 data is present in the frame, the TCH64 channel will follow the TCH16 channel.

5.4.4.3 Uplink Registration Request Contention Burst (RCB)

5.4.4.3.1 Preamble

The first portion of the Uplink Registration Request Message burst shall be a 24 symbol preamble as defined in Section 5.4.3.5.

5.4.4.3.2 Registration Request Burst

The registration burst is sent by CPEs in the registration contention slot when performing registration. The payload is FEC protected in a shortened format. QPSK/CQPSK modulation scheme is used.

5.4.4.4 Uplink Bandwidth Request Contention Burst (BCB)

5.4.4.4.1 Preamble

The first portion of the Uplink Bandwidth Request Message burst shall be a 24 symbol preamble as defined in Section 5.4.3.5.

5.4.4.4.2 Bandwidth Request Burst

The Bandwidth Request burst is sent by the CPE to the BS in the Bandwidth Contention Slot to request bandwidth in which to send data for a specific connection. The payload is FEC protected in a shortened format. QPSK/CQPSK modulation scheme is used.

5.4.4.5 Uplink Schedule Data Burst (UDB4, UDB16, & UDB64)

The uplink data packet bursts provide the physical channel for the uplink TCH4, TCH16, and TCH64 logical channels using, respectively, QPSK (or CQPSK), QAM-16, or QAM-64 modulation. Although the first scheduled uplink burst is assigned to a PS boundary, the latter may be assigned to a specific symbol location. When allocations using the same modulation level are ended, a PS boundary maybe forced for the next allocation.

5.4.4.5.1 Preamble

Uplink MAC data packets burst shall start with one of three preambles as defined in Section 5.4.3.5 depending on the type of modulation in use by the CPE.

5.4.4.5.2 Uplink Traffic Data Packets

The uplink traffic data packets are used to transport CPE user data to the BS using the appropriate modulation type. The data packets consist of concatenated MAC control messages and MAC data packets.

The CPE must fill the data packet so the burst uses all of its granted allocation as indicated in the Uplink Map.

5.4.5 Transmission modes

5.4.5.1 BS continuous transmission

When the BS is in continuous transmission mode, normal downlink bursts shall be transmitted on the main carrier. When the BS does not have enough downlink traffic to fill the downlink burst, the BS shall stop transmit for the remaining duration of that downlink subframe.

5.4.5.2 CPE discontinuous transmission

Each CPE may be granted a portion of the uplink spectrum for transmission of scheduled data traffic (UL TCHx). These uplink transmission bursts shall be transmitted on the main carrier.

5.4.5.3 BS discontinuous transmission

Similar to 5.4.5.2, supporting the TDMA downlink option.

5.5 MAPPING OF LOGICAL CHANNELS INTO PHYSICAL CHANNELS

In the case of TDD, the PHY uses only one RF channel that carries both uplink and downlink traffic data and control data. In the case of FDD, the PHY uses a pair of RF channels, one for the uplink and one for the downlink. The RF channel is subdivided into physical channels as defined in Section 5.4. These physical channels transport the logical channels defined in Section 5.3.

5.5.1 General mapping of logical channels

Table 5-4 defines the mapping in time of logical channels into physical channel types.

Logical Channel	Direction	Burst Type	FN	PSN
PCCH & MCCH	DL	DLB	All	1 to a
DL TCH4	DL	DLB	As Required	a to b
DL TCH16	DL	DLB	As Required	b to c
DL TCH64	DL	DLB	As Required	c to d
TTG			All (TDD only)	d to e
RCCH	UL	RCB	As Required	e to f
BCCH	UL	BCB	As Required	f to g
UL TCH4	UL	UDB4	As Required	g to h
UL TCH16	UL	UDB16	As Required	h to k
UL TCH64	UL	UDB64	As Required	k to 5000-x
RTG			All (TDD only)	5000-x to 5000
DLB = Downlink Burst, B	CB = Bandwidth C	ontention Burst, R	CB = Registration Content	ion Burst, UDB = Uplink

 Table 5-4 Mapping of Logical Channel into Physical Channels - TDD

Data Burst

Logical Channel	Direction	Burst Type	FN	PSN
PCCH & MCCH	DL	DLB	All	1 to a
DL TCH4	DL	DLB	As Required	a to b
DL TCH16	DL	DLB	As Required	b to c
DL TCH64	DL	DLB	As Required	c to 5000
RCCH	UL	RCB	As Required	0 to f
BCCH	UL	BCB	As Required	f to g
UL TCH4	UL	UDB4	As Required	G to h
UL TCH16	UL	UDB16	As Required	H to k
UL TCH64	UL	UDB64	As Required	k to 5000

Table 5-5 Mapping of Logical Channel into Physical Channels - FDD

Each frame may contain each type of logical channel. The allocation of PSs and symbols to each type of logical channel is based on current subscriber demands. Figure 5-6 depicts the division of the frame into logical sub-channels as listed in Table 5-4.

The Registration Control Channel (RCCH) and the Bandwidth Control Channel (BCCH) can be located any where within the uplink subframe. In practice, they are the first and second slots, respectively, in the uplink subframe.
0	0 1	l	á	a t		c 	d (e
RT G	Pr ea m ble	PHY Control QPSK	MAC Control QPSK	Data QPSK	Data QAM-16	Data QAM-64	TT G	



0 1	1	a	a k	2	C .	5000
Pr ea m ble	PHY Control QPSK	MAC Control QPSK	Data QPSK	Data QAM-16	Data QAM-64	



Figure 5-6 Logical Channel Mapping (TDD/FDD)

6 CHANNEL CODING AND SCRAMBLING

6.1 INTRODUCTION

A reference configuration of the PHY transmission chain is given in Section 4. According to the reference configuration, this section defines the error control process which applies to the information bits packed in MAC blocks, and which provides multiplexed bits packed in multiplexed blocks.

This section includes the specification of encoding but does not specify any data processing on the receive part. A definition of the error control process is provided for each kind of logical channel. The definition of logical channels is given in Section 5.

6.2 GENERAL

6.2.1 Interfaces in the error control structure

The definition of interfaces within the error control structure is given by Figure 6-1.

Each burst shall have its own, independent error correction. For each one, the information bits (eventually including a MAC header) are referred to as type-1 bits. The type-1 bits are packed in MAC blocks, which are referred to as type-1 blocks, this defines interface (1) in Figure 6-1.

The processing in the transmit part shall be as follows:

- The type-1 bits shall be segmented into type-2 blocks of N byte length which. The N segmented bytes are referred to as type-2 bytes and shall be packed in a type-2 block, this defines interface (2);
- The type-2 bits shall be processed into type-3 blocks by adding a 1 byte header and appending a 16 bit CRC (2 byte). The header, payload and CRC (N+3, total) bytes are referred to as type-3 bytes and shall be packed in a type-3 block, this defines interface (3);
- the type-3 bits shall be scrambled, into type-4 bits, which compose type-4 blocks, this defines the interface (4).
- the type-4 bits shall be encoded by a FEC block code. The block-encoded bits and are
 referred to as type-5 bits and shall be packed in a type-5 block, this defines interface (5);
 These bits shall then be mapped into multiplexed blocks.

All these operations are made on a per type-1 block basis. The sizes of type-1 blocks and of type-3 blocks and multiplexed blocks depend on the logical channel with which they are associated.



Figure 6-1 Interfaces in the Error Control Structure

6.2.2 Definition of error control codes

The FEC is based on a concatenation of 2 codes. A Reed Solomon GF(256) code is used as the outer code. An inner code is chosen to expose the decoding process to soft input without a requirement of interleaving which is essential for burst communications. The FEC code is used on all control channel and traffic channel data but not on the burst preambles.

6.2.2.1 FEC Code

The input to the FEC is a P byte block of data. A Reed Solomon code is applied first. The inner code is applied afterwards.



There are actually 4 options:

- (1) No inner code, RS only: This case is useful either for a large data block or when high coding rate is required (i.e., P=188). The protection could vary between t=1 to t=16.
- (2) Parity check: This case is useful for moderate to high coding rates with small to medium size blocks (i.e., P=16, 53 or 128). The code itself is a simple bit wise parity check operating on byte (8 bit) level.
- (3) Block code (soft decodable): This case is useful for low to moderate coding rates providing good C/N enhancements. The coding rate is 4/5.
- (4) Block code (soft decodable): This case is useful for low to moderate coding rates providing good C/N enhancements. The coding rate is 2/3.

6.2.2.1.1 RS Encoding

A shortened code RS(P+2t,P) GF(256) is applied to the block resulting in a P+2t RS symbol block. The code is systematic and the redundant symbols are appended to the end of the entering block prior to encoding. The RS code could be used without an inner code.

6.2.2.1.2 Parity Check

A parity check bit is added to each RS symbol individually as the MSB. The parity is an exclusive-or operation on all 8 bits within the symbol. Each RS symbol is translated into a 9 bits. The result is a 9(P+2t) block of bits, symbol after symbol, MSB first. It is recommended to soft decode the parity check code at the receiver.

6.2.2.1.3 Block Code (Option 1)

A (40,32) block code capable of soft decoding is applied over 4 bytes of the RS output resulting in 40 bits (5 bytes).

6.2.2.1.4 Block Code (Option 2)

A (48,32) block code capable of soft decoding is applied over 4 bytes of the RS output resulting in 48 bits (6 bytes).

REMARK: As in these options (Block code, option 1,2) the coding efficiency and capacity are reduced in exchange for better coding gain a separate contribution would be submitted to discuss its merits.

6.2.2.1.5 Shortening

When the number of bytes entering the FEC process M is less than P bytes, the following operation is performed:

- (1) (P-M) zero bytes are added to the M byte block as a prefix
- (2) RS Encoding is performed
- (3) The (P-M) zero RS symbols not associated with the original data are discarded
- (4) Inner coding is performed on remaining symbols
- (5) The resulting byte block is converted to bit block

It is expected that the receiver having knowledge of the expected data length, would properly zero pad the received block and decode it afterwards.

6.2.2.1.6 Variable Length FEC

When the number of bytes entering the FEC process M is greater than P bytes, the following operation is performed:

- (1) Let K=M
- (2) Next P bytes entering the FEC are encoded
- (3) Subtract P from K, meaning Let K=K-P
- (4) If K<P go to (5) otherwise go to (2)
- (5) Shortened FEC is applied to the remaining bytes as described by 6.2.2.1.3

It is expected that the receiver having knowledge of the expected data length, would properly zero pad the received block and decode it afterwards.

6.2.2.1.7 PHY Information Element block (PI)

One FEC block is called PHY Information Element block (PI). The data unit presented to the FEC encoder is called a TC Data Unit (TDU). Depending on modulation, the PI requires a different number of PSs.

The following tables lists the number of PSs required per PI for the parity check case and for the RS only case.

Modulation	PSs required per PI
QPSK	N+3+2t
CQPSK	Ceil[4(N+3+2t)/3]
QAM-16	Ceil[(N+3+2t)/2]
QAM-64	Ceil[(N+3+2t)/3]

Remark: Ceil is a ceiling function returning the highest integer closest to the argument

Modulation	PSs required per PI
QPSK	Ceil[9(N+3+2t)/8]
CQPSK	Ceil[3(N+3+2t)/2]
QAM-16	Ceil[9(N+3+2t)/16]
QAM-64	Ceil[3(N+3+2t)/8]

6.2.2.1.8 Scrambling

The scrambling sequence is constructed from the primitive polynomial:

$$P(x) = TBD$$

(1)

Figure 6-2 shows a block diagram of a typical Scrambler. The Scrambler is essentially a Linear Feedback Shift Register with a few taps. Each tap corresponds to an element of the primitive polynomial P(x). Data is fed to the scrambler from the Transmit FIFO interface.



Figure 6-2 Example of a Scrambling Sequence Generator

6.2.3 FEC Parameters

The FEC has 2 parameters: P – the block size in bytes prior to encoding and t – the number of correctable byte errors. Fixed configuration parameters are:

- (1) The PHY and MAC control portions and data transport (downlink, TDM) use P=128, t=6.
- (2) The PHY and MAC control portions and data transport (TDMA) use P=64, t=5.
- (3) The Registration portion uses P=14, t=2.
- (4) The Contention based access portion uses P=5, t=3.

In all options the parity check code is used as the inner code. Only for data transmission, FEC parameters **may** be programmable. In all cases the TC operation adds a 16 bit CRC for reducing the probability of miss detected errors to a minimal value.

7 MODULATION

7.1 INTRODUCTION

To maximize utilization of the airlink, the PHY proposes to use a multi-level modulation scheme. The modulation constellation is selected based on the quality of the RF channel per subscriber, independently on uplink and downlink. If link conditions permit, then a more complex modulation scheme can be utilized hence maximizing airlink throughput while still allowing reliable data transfer. If the airlink degrades over time, possibly due to environmental factors, the system will revert to the less complex constellations to allow more reliable data transfer.

The following subsections apply to the baseband part of the transmitter.

7.2 MODULATION TYPE

The modulation used by the BS in the downlink shall be QPSK, QAM-16, and QAM-64. In the uplink, the modulation used by CPE shall be one of the following: QPSK, QAM-16, or QAM-64. In the case of the reduced cost terminal CQPSK is used.

7.3 MODULATION RATE

Modulation	Symbol or Bit Rate
QPSK, QAM-16, QAM-64	20 MS/s
CQPSK	30 Mbps

For CQPSK the baud rate is 3/4 of the QAM baud rate.

7.4 MODULATION SYMBOL DEFINITION

The sequence of modulation bits shall be mapped onto a sequence of modulation symbols S(k), where k is the corresponding symbol number. The number of bits per symbol is result from the modulation type, for QPSK n=2, for QAM-16 n=4, for QAM-64 n=6. B(m) denotes the modulation bit of a sequence to be transmitted, where m is the bit number (m=1..n).

The complex modulation symbol S(k) shall take the value I +jQ.

As CQPSK is based on phase filtered version of MSK it is actually a binary modulation scheme with QPSK equivalent efficiency.

7.4.1 Bits to Symbol Mapping for QPSK

Figure 7-1 and Table 7-1 describe the bit mapping for QPSK modulation.





Table 7-1	QPSK Bits to Symbol	Mapping
-----------	----------------------------	---------

B(1)	B(2)	I	Q
0	0	1	1
0	1	-1	1
1	0	1	-1
1	1	-1	-1

7.4.2 Bits to Symbol Mapping for QAM-16

Figure 7-2 and Table 7-2 describe the bit mapping for QAM-16 modulation.



Figure 7-2 QAM-16 Constellation

B(1)	B(2)	B(3)	B(4)	I	Q
0	0	0	0	1	1
0	0	0	1	1	3
0	0	1	0	1	-1
0	0	1	1	1	-3
0	1	0	0	3	1
0	1	0	1	3	3
0	1	1	0	3	-1
0	1	1	1	3	-3
1	0	0	0	-1	1
1	0	0	1	-1	3
1	0	1	0	-1	-1
1	0	1	1	-1	-3
1	1	0	0	-3	1
1	1	0	1	-3	3
1	1	1	0	-3	-1
1	1	1	1	-3	-3

Table 7-2 QAM-16 Bits to Symbol Mapping

7.4.3 Bits to Symbol Mapping for QAM-64

Figure 7-3 and Table 7-3 describe the bit mapping for QAM-64 modulation.

B(1)	B(2)	B(3)	B(4)	B(5)	B(6)	I	Q
0	0	0	0	0	0	3	3
0	0	0	0	0	1	3	1
0	0	0	0	1	0	1	3
0	0	0	0	1	1	1	1
0	0	0	1	0	0	3	5
0	0	0	1	0	1	3	7
0	0	0	1	1	0	1	5
0	0	0	1	1	1	1	7
0	0	1	0	0	0	5	3
0	0	1	0	0	1	5	1
0	0	1	0	1	0	7	3
0	0	1	0	1	1	7	1
0	0	1	1	0	0	5	5
0	0	1	1	0	1	5	7

Table 7-3	QAM-64	Bits to	Symbol	Mapping
-----------	--------	---------	--------	---------

10円10	10円00	100100	100110	000110	000000	00A00	00H10	
101010	101000	100000	100010	000010	000000	001000	001010	
101011 O	101001 O	100001	100011	000011	000001	001001	001011	
111011 O	111001	110001	110011	010011	010001	011001 O	011011	Ι
111010	111000 O	110000	110010	010010	010000	011000 O	011010	
¹¹ Ц10	11000	110100	110110	010110	010100	01400	01U10	
111111	11101	110101	110111	010111	010101	01U01	011111	

Q

100111 000111

000101 00Ц01 00Ц11

100101

10Ц11 10Ц01

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Figure 7-3	QAM-64	Constellation
		Constenation

B(1)	B(2)	B(3)	B(4)	B(5)	B(6)	I	Q
0	0	1	1	1	0	7	5
0	0	1	1	1	1	7	7
0	1	0	0	0	0	3	-3
0	1	0	0	0	1	3	-1
0	1	0	0	1	0	1	-3
0	1	0	0	1	1	1	-1
0	1	0	1	0	0	3	5
0	1	0	1	0	1	3	-7
0	1	0	1	1	0	1	-5
0	1	0	1	1	1	1	-7
0	1	1	0	0	0	5	-3
0	1	1	0	0	1	5	-1
0	1	1	0	1	0	7	-3
0	1	1	0	1	1	7	-1
0	1	1	1	0	0	5	-5
0	1	1	1	0	1	5	-7
0	1	1	1	1	0	7	-5
0	1	1	1	1	1	7	-7
1	0	0	0	0	0	-3	3
1	0	0	0	0	1	-3	1
1	0	0	0	1	0	-1	3
1	0	0	0	1	1	-1	1
1	0	0	1	0	0	-3	5
1	0	0	1	0	1	-3	7
1	0	0	1	1	0	-1	5
1	0	0	1	1	1	-1	7
1	0	1	0	0	0	-5	3
1	0	1	0	0	1	-5	1
1	0	1	0	1	0	-7	3
1	0	1	0	1	1	-7	1
1	0	1	1	0	0	-5	5
1	0	1	1	0	1	-5	7
1	0	1	1	1	0	-7	5
1	0	1	1	1	1	-7	7
1	1	0	0	0	0	-3	-3
1	1	0	0	0	1	-3	-1

B(1)	B(2)	B(3)	B(4)	B(5)	B(6)	I	Q
1	1	0	0	1	0	-1	-3
1	1	0	0	1	1	-1	-1
1	1	0	1	0	0	-3	-5
1	1	0	1	0	1	-3	-7
1	1	0	1	1	0	-1	-5
1	1	0	1	1	1	-1	-7
1	1	1	0	0	0	-5	-3
1	1	1	0	0	1	-5	-1
1	1	1	0	1	0	-7	-3
1	1	1	0	1	1	-7	-1
1	1	1	1	0	0	-5	-5
1	1	1	1	0	1	-5	-7
1	1	1	1	1	0	-7	-5
1	1	1	1	1	1	-7	-7

7.4.4 QAM signal definition

The modulated signal, at carrier frequency fc, shall be given by:

$$M(t) = \operatorname{Re}\{s(t) \exp(j(2\pi f_{c}T + \phi))\}$$
(2)

where:

 ϕ = an arbitrary phase;

s(t) = the complex envelope of the modulated signal defined as:

$$\mathbf{S}(\mathbf{t}) = \sum_{k=0}^{K} \mathbf{S}(k)\mathbf{g}(\mathbf{t}-\mathbf{t}_{\mathbf{k}})$$
(3)

where:

K = the maximum number of symbols;

T = the symbol duration;

 $t_k = kT = is$ the symbol time corresponding to modulation symbol S(k);

g(t) = the ideal symbol waveform, obtained by the inverse Fourier transform of a square root raised cosine spectrum G(f), defined as follows:

G(f) = 1
G(f) =
$$\sqrt{0.5(1 - \sin(p(2|f|T-1)/2a))}$$
 for $\frac{1-a}{2T} \le |f| \le \frac{1+a}{2T}$ (4)

$$G(f) = 0 \qquad \qquad \text{for } |f| \le \frac{1+a}{2T}$$

where:

 α = the roll-off factor, which determines the width of the transmission band at a given symbol rate. The value of α shall be 0.25.

7.4.5 CQPSK signal definition

In MSK, each data bit (+1 or -1) shifts the phase carrier by 90 or -90 degrees according to the bit value. In CQPSK these transitions are filtered resulting in a very compact spectrum.

Table 7-4 CQPSK Bits to Symbol Mapping

B(1)	S
0	-1
1	1

The modulated signal, at carrier frequency fc, shall be given by:

$$M(t) = Re\{exp(j(2\pi f_c T + \phi(t)))\}$$
(5)

where:

 $\phi(t)$ = The filtered phase response to data bits defined as:

$$\phi(t) = \sum_{k=0}^{K} S(k)g(t-t_k)$$
(6)

where:

K = the maximum number of symbols;

T = the bit duration;

 $t_k = kT = is$ the symbol time corresponding to modulation symbol S(k);

g(t) = the ideal phase filter waveform defined as follows:

$$g(t) = \frac{1}{8}g_0(t-T) + \frac{1}{4}g_0(t) + \frac{1}{8}g_0(t+T)$$

$$g_0(t) \approx \sin\left(\frac{\mathbf{p}t}{T}\right) \left[\frac{1}{\mathbf{p}t} - \frac{2 - \frac{2\mathbf{p}t}{T} \cot\left(\frac{\mathbf{p}t}{T}\right) - \frac{\mathbf{p}^2 t^2}{T^2}}{\frac{24\mathbf{p}t^3}{T^2}}\right]$$

This filtering provides an equivalent spectrum efficiency of QPSK with a roll-off factor of approximately 0.5.

A block diagram of the modulation process is shown on the following figure. This diagram is for explanatory purposes and does not prescribe a specific implementation. The modulation filter excited by the complex Dirac impulse function $S(k)d(t-t_k)$ ideally has an impulse response g(t). The filter output enters a VCO and directly modulates it.



Figure 7-4 Block Diagram of the Modulation Process

7.5 QAM MODULATION FILTER DEFINITION

The ideal modulation filter shall be a linear phase filter which is defined by the magnitude of its frequency response | H(f) | = G(f).

7.6 QAM MODULATION BLOCK DIAGRAM

A block diagram of the modulation process is shown on the following figure. This diagram is for explanatory purposes and does not prescribe a specific implementation. The modulation filter excited by the complex Dirac impulse function $S(k)d(t-t_k)$ ideally has an impulse response g(t).



Figure 7-5 Block Diagram of the Modulation Process

7.7 MANDATORY AND OPTIONAL MODULATION SCHEMES

For the downlink QAM-4 and QAM-16 modulation schemes are mandatory while QAM-64 is optional. For the uplink modulation schemes depend on the target cost and capabilities of the end user. For high end users both QPSK and QAM-16 are mandatory while QAM-64 is optional. For reduced cost terminals CQPSK is mandatory.

8 RADIO TRANSMISSION AND RECEPTION

8.1 FREQUENCY BANDS AND CHANNEL ARRANGEMENT

8.1.1 GENERAL

IEEE 802.16.1 is considering millimeter wave frequencies as the target operational frequency band, specifically those above 10 GHz. Line of Sight (LOS) communications is mandatory at these frequencies. Typical cell radius in a PMP deployment is limited to a few kilometers due to radio technology (i.e., power amplifiers) and susceptibility to rain attenuation. One outcome of these conditions is the fact that channel bandwidth could be large, hence enabling high bit rates with low to moderate modulation schemes.

The vast amount of available spectrum options worldwide points out additional requirements:

- There are frequency bands that historically follow ETSI recommendations. Recommended relevant channel bandwidths for BWA are 14 MHz, 28 MHz and 56 MHz.
- Other frequency bands and new worldwide spectrum allocations favor channel bandwidths of either 20 MHz and 40 MHz or 25 MHz and 50 MHz.
- Both FDD and TDD should be supported.

We are not considering smaller channels due to the fact that it would require complex modulation schemes to enable very high bit rates. Complex modulation schemes are much more susceptible to co-channel interference which is a major problem in PMP deployments.

The following table recommends modem baud rates and channel sizes. The proposed pulse shape is Nyquist Root-Raised Cosine with a roll-off factor of 0.25.

Baud Rate (MBaud)	US Channel Size [MHz]	Frame size (mSec)	Number of PSs/Frame
40	50	0.5	5000
32	40	0.5	4000
20	25	1	5000
16	20	1	4000
10	12.5	2	5000

8.1.2 LMDS A Block (27.5-28.35, 29.1-29.25, 31.075-31.225)

Figure 8-1 below is the allocation for the LMDS A Block which went to a single carrier in approximately 350 of the 463 BTAs in the United States (some licenses in smaller towns were not purchased). The specific channelization of the frequency is not designated by the FCC, rather the allocations are block allocations that can be used for any terrestrial wireless

application. The only restriction is that the 29.10-29.3 GHz band can only be used for transmissions from the base station to the subscriber on a point to multipoint basis. Below, the diagram shows not using it to serve end users but rather using it for point to point radio backhaul that is also allowed.



LMDS_A_Band.vsd 9/7/99



- 8.1.3 Other Bands
- 8.2 FREQUENCY PERFORMANCE PARAMETERS
- 8.2.1 Receive and Transmit Frequency Parameters

The BS shall operate on any of the frequency channels specified in Table 8-1.

Transmitter	Number of Channels	Channel Numbers	Minimum Center Channel Frequency (GHz)	Maximum Center Channel Frequency (GHz)	Center Frequency Calculation (GHz)
BS/CPE	34	$1 \le N \le 34$	27.5125	28.35	0.025N + 27.4875
BS Only	6	$35 \le N \le 41$	29.1125	29.25	0.025(N-35) + 29.1125
BS/CPE	6	$42 \le N \le 47$	31.0875	31.225	0.025(N-42) + 31.0875
Note: 27.500 – 28.350 GHz shared with Fixed Satellite Service (FSS) 29.100 – 29.250 GHz shared with non-Geostationary Orbit Mobile Satellite Service (NGO/MSS) 31.075 – 31.23 GHz shared with Private point-to-point Microwave					

Table 8-1	LMDS Block A Channel Identification & Allocation
-----------	--

In a TDD based deployment any channel could be used besides 35 to 41. In an FDD arrangement channel pairs could be designated according to ODU capabilities.

8.2.2 Receive Frequency Tunability

The BS receiver **shall** be tunable to any frequency channel defined in Table 8-1.

The BS RF Front End **shall** be tunable over the frequency range of 850 MHz in TBD MHz steps.

8.2.3 Transmit Frequency Tunability

The BS transmitter **shall** be tunable to any frequency channel defined in Table 8-1.

The BS RF Front End **shall** be tunable over the frequency range of 850 MHz in TBD MHz steps.

8.2.4 Frequency Parameters in Other Bands

9 RADIO SUB-SYSTEM CONTROL AND SYNCHRONIZATION

9.1 INTRODUCTION

This section defines the requirements for synchronization on the system radio sub-system. It does not define the synchronization algorithms to be used in the BS and CPE. These are up to the manufacturer to specify.

9.2 TIMING AND SYNCHRONIZATION

9.2.1 General Description of Synchronization System

This subsection gives a general description of the synchronization system. Detailed requirements are given in the subsequent subsections.

The BS downlink signal modulation symbols enable the CPE to synchronize itself to the BS and if necessary correct its frequency standard to be in line with that of the BS.

The timings of PSs, downlink and uplink bursts, TDMA frames, multiframes, and hyperframes are all related to a common set of counters which run continuously whether the CPE and BS are transmitting or not (see subsection 9.2.2). Thus, once the CPE has determined the correct setting of these counters, all its processes are synchronized to the current serving BS.

The CPE must time its transmissions to the BS in line with those received from the BS. This process is called "CPE time base adjustment".

The main synchronization sources which could be made available are:

- Modem Symbol clock (a.k.a. 20 MHz or Symbol Clock) this clock provides reference and synchronization to the modem, ODU and CPE;
- Frame clock this is a 1 kHz clock providing 1 ms reference timing;
- Network clock
 – this is the network timing reference used to drive service interfaces that
 need synchronization, e.g. T1/E1 interfaces. This clock does not apply to the Airlink PHY
 layer.

9.2.2 Time Base Counters

9.2.2.1 Timing Counters

The timing state of the signals transmitted by a BS or CPE shall be defined by the following counters:

- QAM Symbol Number (SN) (0 3);
- CQPSK Bit Number (CN) (0 –5);
- Physical Slot Number (PSN) (0 5000);

9.2.2.2 Values of the Counters

The relationship between these counters shall be as follows:

- SN increments every 50 nanoseconds modulo 3
- CN increments every 30 nanoseconds modulo 5
- In general PSN increments modulo 5001 whenever either SN or CN changes to zero.
- The PSN reset to zero when it holds 5000 and the SN value is changed to 2.
- Frame Number (FN) increments whenever PSN value resets to zero.

The simultaneous change of state of these counters, plus the multiframe and hyperframe counters, to zero defines the time base reference.

9.2.3 Timing of Transmitted Signals

The timing of modulation symbols transmitted by the CPE and BS is defined in section 9.

The CPE may use the timing of receipt of the downlink preamble to set-up its time base counters. If it does, it shall do so as follows:

• augmentation of PSN shall be given by:

PSN: = PSN mod (5,000);

(7)

9.2.4 BS Requirements for Synchronization

TBD

9.2.5 CPE Time and Frequency Acquisition

TBD

9.3 **RF POWER CONTROL**

Adaptive RF power control shall be used by the CPE. By minimizing the transmit power levels, interference to co-channel and adjacent channel users is reduced and CPE power consumption is reduced. See Sections 9.5.3 and 9.5.4 for more details.

The BS does not use adaptive power control. The BS output power is adjustable over the range +20 dBm to -30 dBm.

9.4 RADIO LINK MEASUREMENTS

The radio link measurements include signal power, signal quality and round-trip CPE-BS path delay.

9.4.1 Received Signal Strength Indication (RSSI)

9.4.2 Signal Quality

TBD

9.4.3 Round-trip CPE-BS path delay

The path delay of the CPE is a representation of the distance of the CPE to the serving BS. This distance may be used to prevent CPE grossly exceeding the planned cell boundaries. This information may be sent by the BS to the CPE when appropriate. The allowable distance may be restricted on a cell to cell basis by the network operator, as required.

9.4.3.1 Equalizer

9.5	Additional PHY Related Registration Functions
9.5.1 TBD	Ranging
9.5.2 TBD	Tx Timing Error and Timing Advance
9.5.3 TBD	Power Leveling
9.5.4 TBD	Power Control and Power Offset
9.5.5 TBD	Registration and Ranging Contention Resolution
9.5.6 TBD	CPE Uplink Modulation Change
9.5.7 TBD	CPE Downlink Modulation Change

9.6 PHY / MAC SERVICE ACCESS POINTS

9.6.1 PHY Primitives

The PHY Layer provides the primitives to the TC layer for monitoring and control of the PHY resources:

TBD

9.6.2 PHY Control Message

10 MINIMUM PERFORMANCE

This section details the minimum performance requirements for proper operation of the system for the LMDS A Band frequencies. The values listed in this section apply over the operational environmental ranges of the SYSTEM equipment and measured per subsection 10.1.

PHY Layer Requirement	Specification Section
Reference Test Planes	10.1
Transmitter Minimum Requirements	10.2
- Introduction	10.2.1
- Tap-Gain Process Types	10.2.2
- Propagation Models	10.2.3
Transmitter Minimum Requirements	10.3
– Output Power	10.3.1
– Emission Spectrum	10.3.2
- Unwanted Conducted Emissions	10.3.3
- Unwanted Radiated Emissions	10.3.4
- RF Tolerance	10.3.5
- Required Oscillator Performance	10.3.5.1
- Frequency Stability	10.3.5.2
- Power Stability	10.3.6
- RF Output Power Time Mask	10.3.7
- Intermodulation attenuation	10.3.8
- CPE Channel Switching Time	10.3.9
- Tx / Rx Carrier Switching Time	10.3.10
- Off to On Carrier Switching Time	10.3.11
- On to Off Carrier Release Time	10.3.12
- Special Co-Location Requirements - Transmitter	10.3.13
Receiver Minimum Requirements	10.4
- Blocking Characteristics	10.4.1
- Spurious Response Rejection	10.4.2
- Intermodulation Response Rejection	10.4.3
- Unwanted Conducted Emissions	10.4.4
- Unwanted Radiated Emissions	10.4.5
- Received Signal Strength Indication	10.4.6

Table 10-1	PHY	Layer	Requirements
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PHY Layer Requirement	Specification Section
- Special Co-Location Requirements - Receiver	10.4.7
Transmitter / Receiver Performance	10.5
- Modulation Accuracy	10.5.1
- Receiver Performance	10.5.2
- Nominal Error Rates	10.5.2.1
- Static Reference Sensitivity Performance	10.5.2.2
- Dynamic Reference Sensitivity Performance	10.5.2.3
- Reference Interference Performance	10.5.2.4
- CPE receiver performance for synchronization acquisition	10.5.2.5

10.1 REFERENCE TEST PLANES

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10.2 PROPAGATION CONDITIONS

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10.2.1 Propagation Models

In this subsection, the propagation models that are referred to in this PHY Specification are defined.

Table 10-2 Propagation Models

Propagation model	Tap number	Relative delay (ηs)	Average relative power (dB)	Tap-gain process
Static				
Dynamic				

10.3 TRANSMITTER CHARACTERISTICS

Unless stated otherwise, the transmitter requirements are referenced to the antenna output port and apply with the transmitter tuned to any channel in Section 8.1.

10.3.1 Output Power

In the following subsections, power is defined as the average power, measured through the square root raised cosine filter defined in Section 7 over the scrambled bits of one transmitted burst as defined in Section 5.

The power at which CPEs or BSs may operate are specified in the following subsections.

10.3.1.1 BS

The BS transmitter maximum output power shall be as defined in Table 10-3.

Table 10-3 Maximum BS Transmitter Power

Power class	Maximum power per carrier
1	

The output power shall be adjustable over the range +20 dBm to -30 dBm via a configurable software parameter.

10.3.1.2 CPE

The CPE maximum power shall be as defined in Table 10-4.

 Table 10-4
 Maximum CPE Transmitter Power

Power class	Maximum power
1	

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Step Level	Power
0	
1	
2	
* * *	
98	
99	
100	

10.3.2 Emissions Spectrum

TBD

10.3.3 Unwanted Conducted Emissions

Unwanted radiated emissions 10.3.4 TBD 10.3.5 Intermodulation Attenuation TBD 10.3.6 Power Stability TBD 10.3.7 **RF** Output Power Time Mask TBD Tx / Rx Carrier Switching Time Requirements 10.3.8 TBD 10.3.9 CPE Channel Switching Time TBD 10.3.10 Special Co-Location Requirements - Transmitter TBD 10.4 **RECEIVER CHARACTERISTIC** TBD 10.4.1 **Blocking Characteristics** TBD 10.4.2 **Spurious Response Rejection** TBD Intermodulation Response Rejection 10.4.3 TBD Unwanted Conducted Emissions 10.4.4 TBD

10.4.5 Unwanted Radiated Emissions

10.4.6 Received Signal Strength Indication (RSSI)

TBD

10.4.7 Special Co-Location Requirements - Receiver

TBD

10.5 TRANSMITTER / RECEIVER PERFORMANCE

TBD

10.5.1 Modulation Accuracy

TBD

10.5.2 Receiver Performance

11 SYSTEM GAIN

As expected modem performance depends on modulation scheme used. The following table shows the Es/No required for post coding BER of 10^{-6} and 10^{-10} :

Modulation Scheme	Es/No 1 [dB]	Es/No 2 [dB]
CQPSK	9	10
QPSK	8	9
QAM-16	14	16
QAM-64	20	22

The back-off requirements are approximately 0, 4, 6 and 8 dB for CQPSK, QPSK, QAM-16 and QAM-64 respectively. For a 0 dBW "ideal" transmitter the expected power output is +30 dBm, +26 dBm, +24 dBm and +22 dBm for CQPSK, QPSK, QAM-16 and QAM-64 respectively. For the recommended channel bandwidth operation in the LMDS block A band (25 MHz) the noise floor is about -100 dBm (assuming an ideal LNA with 0 dB NF). The system gain (normalized, RSG) is therefore:

Modulation Scheme	RSG1	RSG2
	[dB]	[dB]
CQPSK	121	120
QPSK	118	117
QAM-16	110	108
QAM-64	102	100

Remarks:

- The results are given for the 128 byte case, RS+Parity
- If the block code option is used instead of the parity, the RSG would be increased by about 2 dB for (40,32) and by 3.5 dB for (48,32) @10⁻¹⁰

12 CRITERIA LIST

The following is a discussion regarding the 802.16 criteria list:

1	Meeting System Requirements	This proposal is believed to meet system requirements of IEEE 802.16
2	Spectrum Efficiency	The use of SLAM (Subscriber Level Adaptive Modulation) balances between range and capacity. The average bps/Hz in a typical deployment (FDD or TDD) would be about 3 bps/Hz without the penalty of shrinked cell sizes due to modulation complexity. In TDD mode correct balance between uplink and downlink could be maintained hence increasing spectrum efficiency. This PHY allows efficient implementation of uplink TDMA taking into account dynamic of user traffic.
3	Implementation Simplicity	The core functions of this PHY (i.e., QAM modulation, Reed-Solomon FEC) are well known technologies with simple implementations.
4	CPE Cost Optimization	The PHY supports either FSDD or TDD, which allow low cost ODU implementation.
5	Spectrum Resource Flexibility	The PHY can be used for any worldwide available spectrum. Modem baud rate can be easily modified to support channels between 10 to 50 Mbaud following well known channel scheme.
6	System Diversity Flexibility	The PHY may be used for various spectrum allocations (as explained in (5)) and is protocol agnostic meaning that it may support various network architectures.
7	Protocol Interfacing Complexity	The PHY uses information elements which are small enough to efficiently carry variable length packets such as IP and efficiently carry fixed length packets as ATM or STM.
8	Implication on Network Interfaces	As explained in (7) the PHY may be combined with higher layer protocols to transport either ATM, IP or STM. Frame structure is designed for low delay and fast recovery from failure.
9	RSG	Actual values are presented in this proposal. These values allow cell radius of a few miles even when availability is set to a high target. SLAM allows to trade-off almost 20 dB between range and capacity. The additional FEC options allow to increase the RSG further up to 3.5 dB
10	Robustness to Interference	The short packet format supported by the PHY (and by the TC/MAC) offers fast recovery if packet loss occurs. SLAM capability of the modem to back-off to QPSK modulation offers robustness to interference.
11	Robustness to Channel Impairments	The short packet format supported by the PHY and the SLAM capability of the modem to back-off to QPSK modulation offers robustness to channel impairments. Equalization procedures are easily implemented at the receiver (or pre-equalization at transmitter) to cope with typical multi-path scenarios in PMP/LOS deployments.

This proposal either fulfills mandatory requirements or does not preclude items which were pointed out as part of mandatory requirements.