Project	**IEEE 802.16 Broadband Wireless Access Working Group <http://ieee802.org/16>**
Title	**An Amendment to MODE B of IEEE 802.16.1pc-00/19**
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Re:	Call for Evaluations and Improvements, IEEE 802.16.1, Session #7.
Abstract	The following ECC proposal is submitted as further improvement to the ECC coding scheme of the PHY proposal **802.16.1pc-00/19.** The proposal is consistent with previous contribution **802.16.1pc-00/18**, which applies to two main current PHY proposals**.**
Purpose	To provide a description of a proposed ECC for Mode B of proposal **IEEE 802.16.1pc-00/19.**
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An Amendment to Mode B of IEEE 802.16.1pc-00/19

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1.0 Introduction

This document specifically addresses an amendment to the adaptive modulation mode proposed in **802.16.1pc-00/19** denoted there MODE B. In compliance with our previous proposal **802.16.1pc-00/18** [1] we propose to replace the traditional Reed-Solomon (RS) codes by binary block product codes and use Soft-in\Soft-out (SISO) iterative decoders (i.e. "Block Turbo Codes", BTC). Compatibility with baseline downstream modes of the 802.16.1pc-00/19 [2] includes: Transmission Convergence (TC) layer, scrambling for energy dispersal, preamble prepend and baseband pulse shaping. The bit mapping to Gray coded QPSK, 16QAM and optionally 64QAM constellation are compatible with 802.16.1pc-00/20 [3].

1.1 Background

Iterative Soft-in\Soft-out (SISO) decoders ("Turbo Codes") and especially BTC are subjected to further consideration as ECC scheme for the PHY layer of the IEEE802.16.1.

Compared to traditional Error Control Coding (ECC) schemes such as Reed-Solomon (RS) codes, convolutional codes, concatenation of both (i.e. Reed-Solomon Viterbi, RSV), or concatenation of RS with other binary inner block codes (i.e., [3]) the BTC techniques are more appealing in BWA applications. ECC schemes based on Turbo Decoding outperform the legacy ECC in terms of coding gain. Furthermore, SISO iterative decoders have inherent ingredient that allow the highest performance when compared to other decoding strategies. Technological limitation of the two stage concatenated coding scheme, including the recent one [3] is far from optimal performance.

We propose a binary product code based on shortened Hamming codes for the downstream PHY layer, which match the framing format requirements of MODE B in proposal [2].

1.2 Convention and notations

(n, k, d) is a linear block code of length n dimension k and minimum Hamming distance d. The ratio k/n is the code rate. In many cases we shall drop the last parameter and we shall refer to (n, k) block code.

$(n_1, k_1, d_1) \times (n_2, k_2, d_2)$ is a general representation of a block code with length $n=n_1n_2$ dimension $k= k_1k_2$ and minimum distance $d=d_1d_2$. The code constructed in this way is called a "product code" (or 2-D array code), and (n_i, k_i) for i=1,2 are called the components codes. The codewords of the product code can be described by an n_1 times n_2 rectangular array, where the columns are a codewords of code (n_1, k_1) and the rows are codewords of (n_2, k_2).

The general product code based on shortened binary Hamming codes as component codes is given by

$(2^m - S1, 2m - m - 1 - S1, 4) \times (2^m - S2, 2^m - m - 1 - S2, 4)$.

This code is called a Hamming Product Code, **HPC(m, S1,S2).**

The case where S1=S2 leads to a highly symmetric case since the columns encoder is identical to the rows encoder. Symmetric HPC codes are highly desired since they result in implementation reduction.

Examples:

1. An MPEG package contains 188 bytes of 8 bits each. Thus, a product code which contains exactly these 188x8=1504 bits is realized with the following parameters:

   m = 6, S1 = 25, S2 = 10.

This implies (39, 32) and (54, 47) shortened Hamming components codes which constitute the binary product code (39x54, 32x47, 4x4) = (2106, 1504, 16) with code rate 0.714.

2. Symmetric HPC for the MPEG frame (see [1]) can have the following parameters

   HPC(m=6, S1=S2=18) = (46,39) x (46,39) = (2116, 1521,16)

3. Symmetric HPC for 128 Bytes frame

   HPC(m=6, S1=S2=25) = (39,32) x (39,32) = (1521, 1024,16)

The shortened Hamming code (64-S, 57 - S) with shortening parameter S shall be implemented by appending S bits, all set to zero, before the information bits at the input of (64,57) extended Hamming encoder. This encoder shall be implemented by appending a parity check column the generator matrix of the Hamming code (63,57) generated by the primitive polynomial of degree 6:

$$g(x) = X^6 + X^1 + 1$$

2.0 Mode B Downstream Physical Media Dependent (PMD) sublayer

The encoding and decoding functions for the MODE B downstream physical layer is based on burst type architecture for the PMD sublayer. As a result, a sequence of 1 ms frames is transmitted. The underlying frame structure assumes integer number of physical slots (PS) each consists of 4 modulation symbols, where 4,16,64-QAM modulation are allowed. Thus PS for QPSK consists of 1byte while for 16QAM and 64QAM the PS consists of 2, 3 bytes, respectively. The proposed ECC in ref [2] for MODE B is RS(192,164).

The RS(192,164) can be replaced by HPC as follows:
Option 1: HPC(m=6, S1= 25, S2=18) = (39,32) x (48,41) = (1872, 1312,16)

Option 2: Symmetric HPC based on HPC(m=6,S1=S2=21) = (43,36) x (43,36) = (1849,1296,16)

3.0 Summary and Recommendations

SISO iterative decoders based on Hamming Product codes (HPC) are suggested as an amendment to the PHY proposals of [2]. Since the code presented have almost the same code rate as given for the codes presented in [1] the resulted error performance versus normalized signal-to-noise ratio are almost the same.

References

[1] IEEE 802.16.1pc-00/18

[2] IEEE 802.16.1pc-00/19

[3] IEEE 802.16.1pc-00/20