Project	**IEEE 802.16 Broadband Wireless Access Working Group <http://ieee802.org/16>**
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Source(s)	Alok Gupta Ensemble Communications, Inc. 6256 Greenwich Dr., Ste 400 San Diego, 92122 Voice: 858 458 1400 ext. 133 Fax: 858 458 1401 mailto:alok@ensemblecom.com
Re:	This is a response to the BWA FEC call for contributions IEEE 802.16.1p-00/06
Abstract	The codes proposed in this documents are well suited for BWA applications, specifically those of burst nature. As explained in the attached document they are provide excellent balance between complexity and performance.
Purpose	To be part of an FEC survey for BWA
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>>>> *Remark: Requested tables are attached at the end of this document*

Introduction

This paper presents the concatenated channel coding scheme for applications to Broadband Wireless Access. The outer code is Reed-Solomon (RS) code over GF(2^8) with variable number of redundancy. The inner codes are low complexity, short binary block codes. Depending upon the overall code rates, there are two choices for the inner codes.

(a) (9,8) Parity Check Code

(b) (24,16) Block code derived from 4-states non-systematic rate ½ convolutional code punctured to rate 2/3 with tailbiting trellis, which eliminates the overhead for trellis termination.

The inner codes have very simple trellises. Hence they are decoded with soft-decision maximum likelihood Viterbi decoders. The parity check code has only two-states trellis of length 8. (24,16) code would require 4 4-states trellises of length 16 for decoding.

The performance of the concatenated system is presented for four different overall code rates and 3 different packet sizes. The overall code rates selected are 5/6, ¾, 2/3 and ½. The packet sizes selected are 1 ATM cell (53 bytes), 2 ATM cells and 3 ATM cells. The performance of the system in AWGN for BPSK/QPSK modulation is presented in terms of required Eb/No as well as C/N for a specified output BER. Note that these two parameters are simply related by overall code rate r and modulation symbol size M as follows.

$$C/N = 10 \log_{10}[M] + 10 \mathrm{Log}_{10}[r] + E_b/N_o$$

Even though E_b/N_o is the most commonly used parameters for comparing different digital communication systems, C/N is actually used in link budget calculations making it a more practical performance parameter. Also note that different code rates result in larger variation in required C/N than E_b/N_o, emphasizing the usefulness of flexible channel coding schemes to deal with varying link conditions.

Note that for larger block sizes, large number of RS redundancy is added just to achieve the target overall rate. In practice, additional coding gain achieved is very little beyond certain RS redundancy (e.g. 32). Hence when the final decision is taken, the RS redundancy can be limited to some appropriate maximum number. This would result in improving the overall code rates for larger block sizes without much degradation in performance.

For comparing the proposed coding scheme with turbo based schemes, Frame Error Rate (FER) is a more

appropriate parameters for fair comparison. This is because of the following reasons. When a convolutional turbo code employing iterative decoding makes a decoding errors, the most probable error events contains only 2, 3 or 4 bit errors per block resulting in smaller BER for a comparable FER. Similar argument holds for product codes also. For a packet based system, a decoded block in error is useless irrespective of the number of bit errors it contains.

Performance Analysis

The BER performance is computed using semi-analytical method. The symbol and bit error rates at the output of the inner decoders are obtained from the simulation with very high accuracy and the BER at the output of RS decoder is analytically computed.

Let P_b and P_{byte} denote the bit and byte error probabilities at the output of Viterbi decoder for the inner code. The RS decoder either corrects t or less number of byte errors or passes the code word unchanged when it contains more than t errors. The probability of misdecoding is quite small for reasonably high t (for example 8) and hence it can be ignored. Thus we can say that the bit error rate to the byte error rate ratio at the input and output of RS decoder is the same. Then the BER at the output of t-error correcting RS decoder for a message block length of M bytes is given by the following expression

$$(P_e)_{RS} = \frac{P_b}{P_{byte}} \frac{1}{N} \sum_{i=t+1}^{N} i \binom{N}{i} (P_{byte})^i (1 - P_{byte})^{N-i}$$

where N = M + 2t is the code word length.

The analysis is slightly more complicated for (24,16) inner code, since the byte errors are not completely uncorrelated for this case. Let P_b and P_{byte} denote the bit and byte error probabilities at the output of inner code decoder. Also, let P_w and P_x denote the probabilities of 1 and 2 byte errors, respectively, in a 16-bit decoded word at the output of inner code decoder. Then the BER at the output of t-byte correcting RS decoder is given by the following expression

$$(P_e)_{RS} = \frac{P_b}{P_{byte}} \sum_{\substack{w+2x>t \\ w+x\le N \\ 0\le w,x\le N}} \frac{w+2x}{2N} \binom{N}{w} \binom{N-w}{x} P_w{}^w P_x{}^x (1 - P_w - P_x)^{N-w-x}$$

where N = (M+2t)/2, M is the message size in bytes.

The probabilities P_b, P_{byte}, P_w and P_x were obtained from the simulation for different E_b/N_o. To ensure the

accuracy of these probabilities from the simulation, simulation was run to collect at least 500 error events of each type. Since there are a large number of terms in the above summation, computer was used to evaluate the above expression.

The performance of the concatenated system is summarized in the table below. The E_b/N_o and C/N numbers are in dB. The corresponding Frame Error Rate (FER) is also provided.

Table 01. Performance of the Concatenated System

	Target Code Rate 5/6			Target Code Rate 3/4		Target Code Rate 2/3		Target Code Rate ½	
Block Size	(57,53) & (9,8) Rate = 0.8265			(63,53) & (9,8) Rate = 0.7477		(73,53) & (9,8) Rate = 0.645		(72,53) & (24,16) Rate = 0.490	
53 Bytes		10^{-6}	10^{-9}	10^{-6}	10^{-9}	10^{-6}	10^{-9}	10^{-6}	10^{-9}
	E_b/N_o	6.66	7.80	5.85	6.67	5.50	6.13	4.90	5.62
	C/N	8.84	9.98	7.59	8.41	6.60	7.23	4.81	5.53
	FER	10^{-4}	810^{-8}	510^{-5}	510^{-8}	10^{-5}	310^{-8}	210^{-5}	310^{-8}
106 Bytes	(114,106) & (9,8) Rate = 0.8265			(126,106) &(9,8) Rate = 0.7477		(144,106) & (9,8) Rate = 0.654		(142,106) & (24,16) Rate = 0.4976	
	E_b/N_o	6.08	6.92	5.30	5.88	4.97	5.46	4.29	4.78
	C/N	8.26	9.10	7.04	7.62	6.13	6.62	4.26	4.75
	FER	10^{-4}	810^{-8}	510^{-5}	510^{-8}	210^{-5}	310^{-8}	210^{-5}	310^{-8}
159 Bytes	(171,159) & (9,8) Rate = 0.8265			(189,159) &(9,8) Rate = 0.7477		(215,159) & (9,8) Rate = 0.657		(212,159) & (24,16) Rate = 0.50	
	E_b/N_o	5.77	6.46	5.04	5.53	4.72	5.16	4.08	4.46
	C/N	7.95	8.64	6.78	7.27	5.90	6.34	4.08	4.46
	FER	10^{-4}	810^{-8}	510^{-5}	510^{-8}	210^{-5}	310^{-8}	210^{-5}	310^{-8}

All the schemes presented here are applicable for both uplink and downlink channel.

Low Encoder and Decoder Complexity

The proposed scheme offers great advantage in terms of all aspects of implementation complexity : gate counts, simplicity of hardware architecture, design and verification and simplicity of the encoding and decoding algorithms. It adds very minimal complexity over a systems employing only the RS code which is in ubiquitous use today in almost all digital communications systems. The inner code Viterbi decoders have only 2 or 4 states and can run at either bit rate or multiple of bit rates by combining several stages in the trellis together. The outer code decoder can use only the byte clock. Also since the Viterbi decoder for the inner code terminates after 8 or 16 stages, shift registers and register exchange method can be used for storing the path memory and path memory updates. Thus the implementation of inner code Viterbi decoder is quite trivial. The gate count estimates for inner code encoder and decoder is about 8K. Assuming the maximum number of RS redundancy limited to 32, the gate count estimate for outer code encoder and decoder is about 24K at BWA data rates.

Low Latency

The proposed system offers another major advantages in terms of latency compared to turbo based system or traditional concatenated system employing more complex convolutional codes and interleaving. The only delay in the proposed system is due the decoding delay of RS decoder which is roughly equal to (assuming a parallel Euclidean implementation) R+2N clock cycles where R is the redundancy and N is the code word length.

Free Error Detection

Another advantage of the proposed scheme is that it does not require a separate CRC code for error detection. RS code with 32 symbol redundancy would provide a very strong error detection capability and it can be quantified. On the other hands, the turbo based systems will require use of CRC code.

Performance Improvement Possible With Very Small Interleaving Depth

Lastly, we want to add that the performance of the proposed system for overall code rate of ½ can be improved by 0.4 to .75 dB (depending upon the block size) if interleaving of depth 2 can be used. This can easily be used in the down link channel for Mode A.

Conclusions

A concatenated coding scheme suitable for both uplink and downlink channels for BWA is presented. The

scheme provides very good coding gain. The implementation complexity is only slightly higher than a system employing only RS codes and latency is the same as RS only system. The difference in required C/N between rate ¾ and rate ½ code is about 3 dB, indicating that the flexible coding scheme can be quite useful in the system with different link margins.

Finally, we want to mention that if the BER and FER performance of different FEC schemes are computed for the same aggregate code rate and block size, then the comparison of different schemes becomes straightforward task. If the FEC committee has different aggregate code rates and block size in mind than the ones presented here, then we would be glad to provide an updated performance table for those rates and block sizes.

>>>> *Requested tables on next page.*

Code	Code 1	Code 2	Code 3	Code 4
Aggregate Code Rate	0.8265	0.7477	0.645	0.490
Uplink/Downlink/ Both	Both	Both	Both	Both
Eb/No Required at Pe = 10E-6	6.66 dB	5.85 dB	5.50 dB	4.90 dB
Eb/No Required at Pe = 10E-9	7.80 dB	6.67 dB	6.13 dB	5.62 dB
Encoder Complexity (QPSK)	2 K	2 K	2 K	2 K
Encoder Complexity (64 QAM)	Same	Same	Same	Same
Decoder Complexity (QPSK)	28 K	28 K	28 K	28 K
Decoder Complexity (64 QAM)	Same	Same	Same	Same
Block Size, in payload data bits	424	424	424	424

Latency (end to end), in payload data bits	880	880	880	880
Code	Code 1	Code 2	Code 3	Code 4
Aggregate Code Rate	0.8265	0.7477	0.654	0.4976
Uplink/Downlink/ Both	Both	Both	Both	Both
Eb/No Required at Pe = 10E-6	6.08 dB	5.30 dB	4.97 dB	4.29 dB
Eb/No Required at Pe = 10E-9	6.92 dB	5.88 dB	5.46 dB	4.78 dB
Encoder Complexity (QPSK)	2 K	2 K	2 K	2 K
Encoder Complexity (64 QAM)	Same	Same	Same	Same
Decoder Complexity (QPSK)	30 K	30 K	30 K	30 K
Decoder Complexity (64 QAM)	Same	Same	Same	Same
Block Size, in payload data bits	848	848	848	848

Latency (end to end), in payload data bits	1728	1728	1728	1728
Code	Code 1	Code 2	Code 3	Code 4
Aggregate Code Rate	0.8265	0.7477	0.657	0.50
Uplink/Downlink/ Both	Both	Both	Both	Both
Eb/No Required at Pe = 10E-6	5.77 dB	5.04 dB	4.72 dB	4.08 dB
Eb/No Required at Pe = 10E-9	6.46 dB	5.53 dB	5.16 dB	4.46 dB
Encoder Complexity (QPSK)	2 K	2 K	2 K	2 K
Encoder Complexity (64 QAM)	Same	Same	Same	Same
Decoder Complexity (QPSK)	32 K	32 K	32 K	32 K
Decoder Complexity (64 QAM)	Same	Same	Same	Same
Block Size, in payload data bits	1272	1272	1272	1272

Latency (end to end), in payload data bits	2576	2576	2576	2576