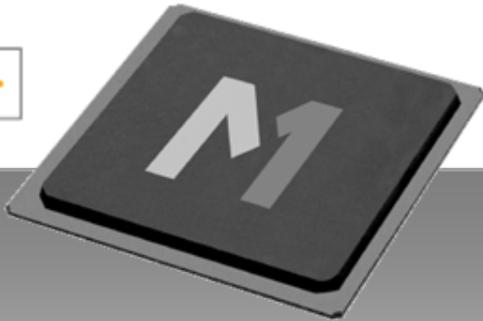


CAUI Loss Budget



July 26 2012

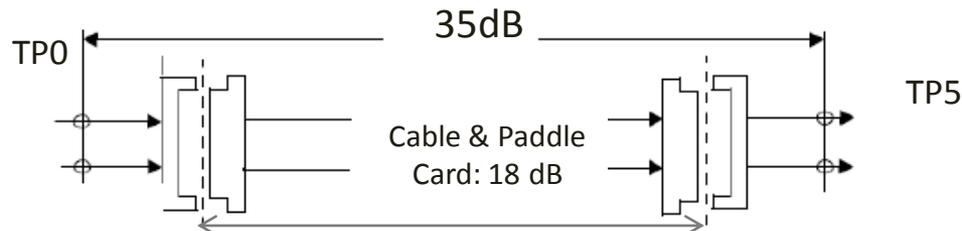
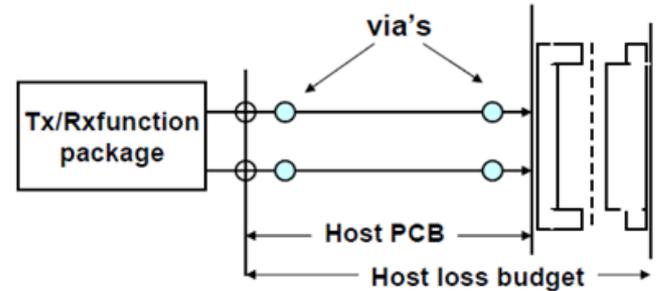
M1NDSPEED

Agenda

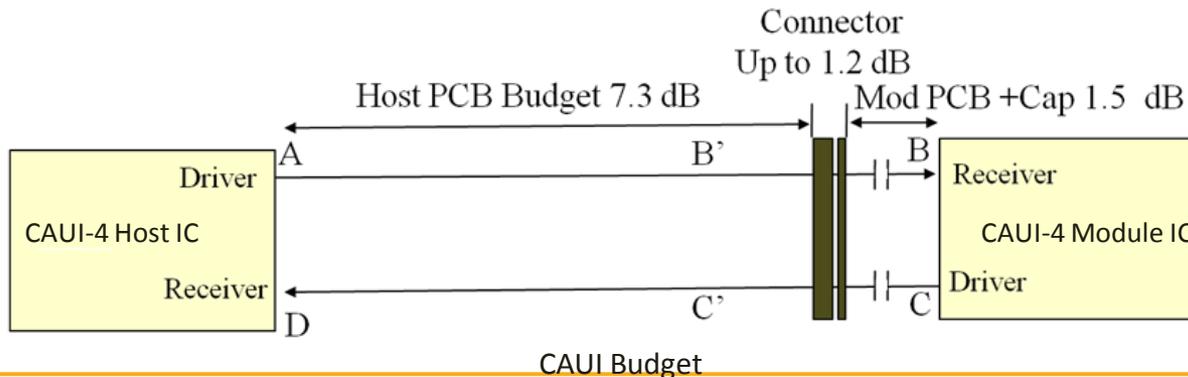
- Recap and new presentations
 - [latchman_01_0312.pdf](#)
 - [ghiasi_02a_0712.pdf](#)
 - CAUI4 options (Tom Palkert)
- Discussion

Latchman_01_0312 Recommendation

- Host Loss Budget: 8.5dB at 12.89GHz
 - includes PCB loss, two sets of vias and mated connector



CR4 Budget: 5 m cable assembly link budget example with 8.5 dB host loss: 35 dB @12.89 GHz (FEC Required)

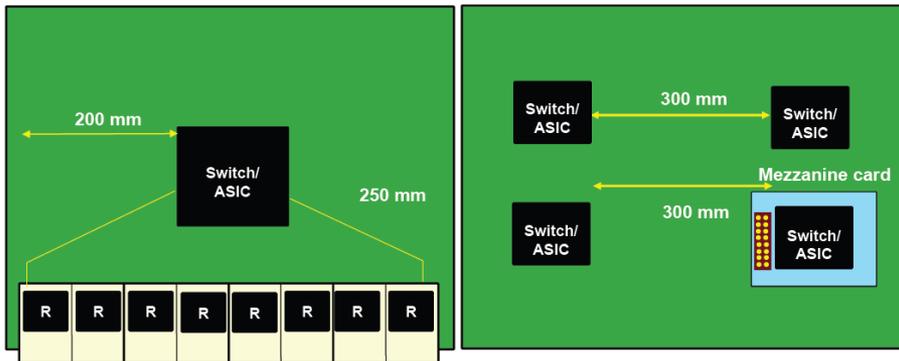


Ghiasi_02a_0712 Summary

CAUI-4 Applications



- Chip to module applications supporting 250 mm
- Chip to chip applications supporting 300 mm



A. Ghiasi

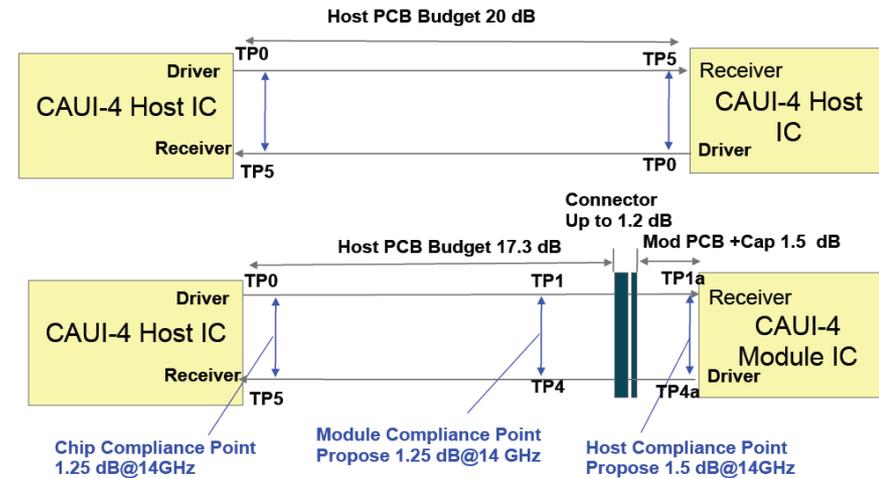
IEEE 100GNGPTX

8

Proposed CAUI-4 Architecture and Reference Points



- Following 802.3 CL83A/B (CAUI) where common I/O supports chip to chip and chip to module



A. Ghiasi

IEEE 100GNGPTX

15

Conclusion

- Have a nice day



Discussion

- Keep chip-module CAUI 4 budget as is and have one budget
 - Repeaters for channels which do not meet budget
 - Keeps common port for copper and optics
- Increase CAUI 4 chip-module budget
 - Higher power module unless asymmetric interface is possible
 - Lose common port with CR4 for that port type (interop issues)
 - Consensus that a solution which is interoperable is required
- Add another CAUI 4 chip-module budget
 - Lose common port with CR4 for that port type (interop issues)
- Make chip to chip spec different loss from chip to module
 - Compliance points would be different relative to chip-module but would allow for higher loss budgets