PCS, FEC and PMA Overview

100 Gb/s Wavelength Short Reach PHYs Study Group

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Introduction

This describes the PCS/FEC/PMA architectures that are in use at 100Gb/s per lane today for re-use by this group.
### Standards Map/Summary

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RS(544,514) used for 50/100G per lane technology
RS(528,514) is used for 25G technology
802.3bs Architecture – 200GbE and 400GbE

- Adopted architecture and possible implementations are shown below for 400GbE
  - 200GbE is identical except for # lanes and MAC rate
- FEC is part of the PCS sublayer utilizing the RS(544,514) aka “KP4” FEC code.
- An extender sublayer is also defined

*FEC is part of the PCS sublayer
802.3bs PCS

- PCS processing flow is shown in the figure
- The PCS distributes data to 16 PCS lanes for 400GbE and 8 PCS lane for 200GbE
- Pre-FEC distribution plays the data out to two FEC codewords
From a muxing point of view, the PMA is simple, m input lanes are bit muxed to n output lanes.

Bit muxing is blind, lanes can move around, the RX PCS sorts things out.

4:1 muxing is used for 100G per lane interfaces.
802.3cd Architecture – 100GbE

> Adopted architecture and possible implementations are shown below for 100GbE
> FEC is in the FEC sublayer, RS(544,514) aka “KP4” FEC
> - An AUI may exist between the FEC and PCS sublayers

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**IEEE Arch**

- MAC/RS
- PCS
- FEC
- PMA
- 100GAUI-x
- PMA
- PMD

**Possible Implementation**

- MAC Device (MAC/PCS/FEC/PMA)
- Module
- Chip to Module I/F
- 100GAUI-2

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**Possible Implementation**

- MAC Device (MAC/PCS/FEC/PMA)
- Module
- Chip to Chip I/F
- 100GAUI-2
- Retimer/Mux
- Chip to Module I/F
- 100GAUI-2

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**Medium**

- MDI
- Medium
802.3cd PCS/FEC Sublayers

PCS processing flow is shown in the figure to the left, FEC to the right.
From a muxing point of view, the PMA is simple, m input lanes are bit muxed to n output lanes.

Bit muxing is blind, lanes can move around, the RX PCS sorts things out.

4:1 muxing is used for 100G per lane interfaces.
Direction in 802.3ck (in draft 1.0)

- Adopted 802.3bs PCS/FEC/PMA structure for all interfaces for 400G/200G PHYs
- Adopted 802.3cd PCS/FEC/PMA structures for all interfaces, with the exception:
  - 100GBASE-KR1/CR1, which also have an interleaved option for the FEC in addition to the above
  - This interleaved FEC is not important to this group since the C2M interface does not support this FEC option
The existing 100G per lane BER budget is split out across AUI interfaces and the PMD budget

- $1 \times 10^{-5}$ for the AUI interfaces
- $2.4 \times 10^{-4}$ for the PMD interface

  - (for 200/400GbE): Provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.223) of less than $1.7 \times 10^{-12}$ for 64-octet frames with minimum interpacket gap when processed according to Clause 120 and then Clause 119.
  
  - (for 100GbE): Provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.275) of less than $9.2 \times 10^{-13}$ for 64-octet frames with minimum interpacket gap when additionally processed by the FEC (Clause 91) and PCS (Clause 82).

- Any new PMD would need to match these requirements, if they do, then the current 802.3 architecture and PCS/FEC is directly applicable to this project
Example Configurations

Seamless Clause 91 FEC end to end, backwards compatible

Seamless Clause 119 FEC end to end, backwards compatible

Clause 119 FEC
Thoughts on the Re-Use

There has been a big investment in the 802.3bs/cd architectures in the industry
- They are already used for 100G per lane optical interfaces for 100GBASE-DR and 400GBASE-DR4 interfaces
- 802.3cu is re-using these architectures

This group should re-use these industry investments as is
- RS(544,514) FEC with 4:1 bit muxing
Thanks!