1.4.330b PoDL Regulated PSE: A PSE that is required to regulate the DC voltage at the PSE MDI/PI over the required range of PD load current.

1.4.330c PoDL Unregulated PSE: A PSE that is not required to regulate the voltage at the PSE MDI/PI over the required range of PD load current.

Insert the following definitions after 1.4.418 "Type 2 PSE" as follows:

1.4.418a Type A PoDL System: A system comprising a PSE, PSE MDI/PI, link segment, PD, and PD MDI/PI, that are compatible with 100BASE-T1 PHYs.

1.4.418b Type B PoDL System: A system comprising a PSE, PSE MDI/PI, link segment, PD, and PD MDI/PI, that are compatible with 1000BASE-T1 PHYs.

1.4.418c Type C PoDL System: A PSE, PSE MDI/PI, link segment, PD, and PD MDI/PI, that are compatible with both 100BASE-T1 and 1000BASE-T1 PHYs. Type C PoDL system elements are compatible with both 100BASE-T1 and 1000BASE-T1 PHYs.

1.5 Abbreviations

Insert the following new abbreviations into the list, in alphabetical order:

MFVS	Maintain Full Voltage Signature
PD	Powered Device
PoDL	Power over Data Lines
PSE	Power Sourcing Equipment
SCCP	Serial Communication Classification Protocol
PPS	Plug-and-Play System
FSS	Fast Startup System

1.4.418d Plug and Play PoDL System(PP System): A PoDL system that uses classification to ensure compatibility between the PSE and PD

1.4.418e Fast Startup System (FS System): A PoDL system that uses detection to rapidly assess whether or not to apply power and requires system engineering to ensure compatibility between PSE and PD because it does not perform classification.

30. Management

Change the first paragraph of Clause 30 as follows:

This clause provides the Layer Management specification for DTEs, repeaters, MAUs, and Midspans based on the CSMA/CD access method. The clause is produced from the ISO framework additions to Clause 5, Layer Management; Clause 19, Repeater Management; and Clause 20, MAU Management. It incorporates additions to the objects, attributes, and behaviours to support 100 Mb/s, 1000 Mb/s and 10 Gb/s, full duplex operation, MAC Control, Link Aggregation, DTE Power via MDI, Power over Data Lines, subscriber access networks, and the Link Layer Discovery Protocol (LLDP) IEEE 802.3 Organizationally Specific TLVs. The objects, attributes, and behaviours to support Link Aggregation are deprecated by IEEE Std 802.1AX-2008.

30.2 Managed objects

30.2.2 Overview of managed objects

30.2.2.1 Text description of managed objects

Change the entry for oPHYEntity as follows:

oPHYEntity — If oOMPEmulation is implemented, oPHYEntity is contained within oOMPEmulation. Otherwise oPHYEntity is contained within oMACEntity. Many instances of oPHYEntity may coexist within one instance of oMACEntity; however, only one PHY may be active for data transfer to and from the MAC at any one time. oPHYEntity is the managed object that contains the MAU, PAF, ~~and~~ PSE, and PoDLPSE managed objects in a DTE.

Insert the following new entry for oPoDLPSE into the list, in alphabetical order:

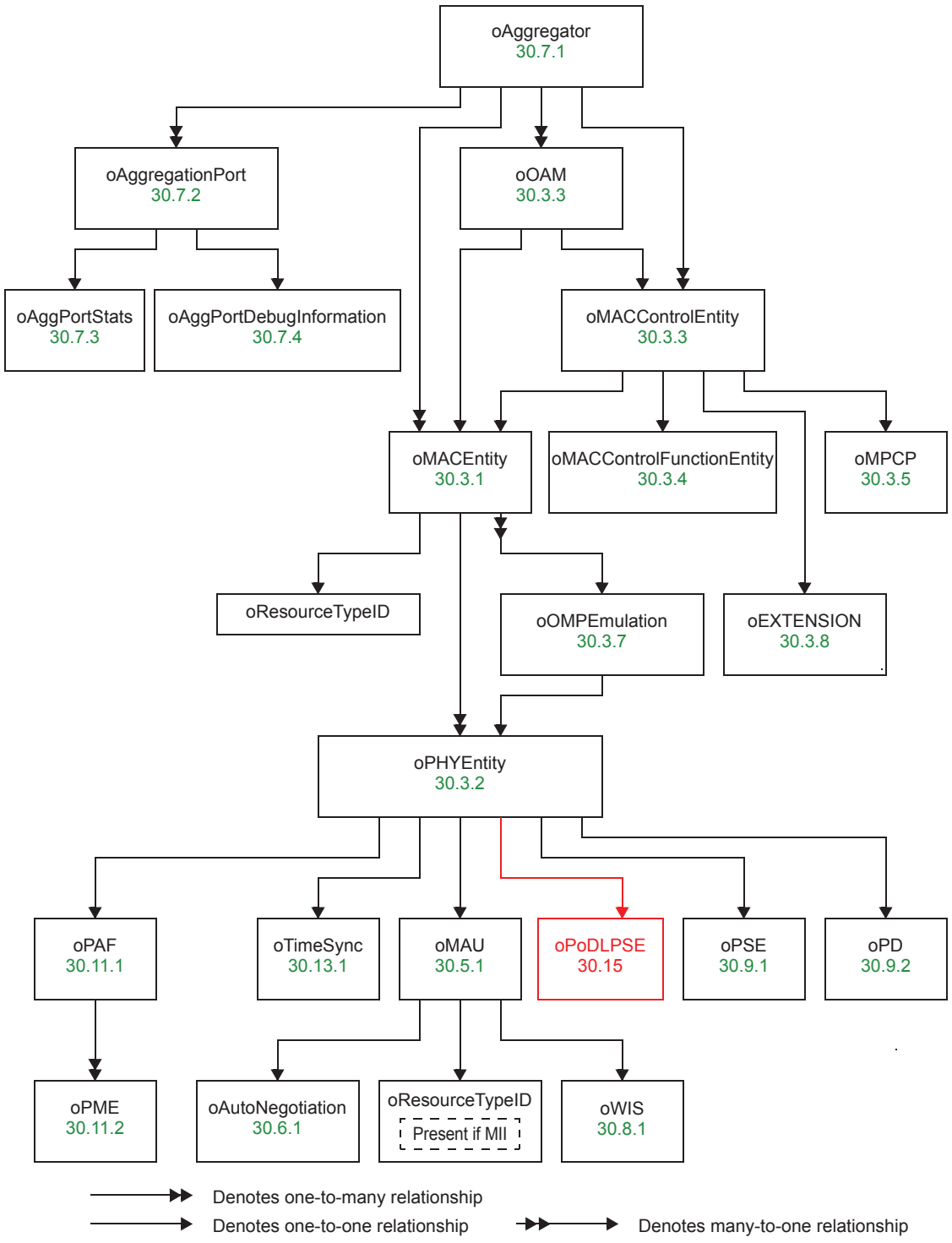
oPoDLPSE — The managed object of that portion of the containment trees shown in Figure 30–3. The attributes, notifications, and actions defined in 30.15 are contained within the PoDLPSE managed object.

30.2.3 Containment

Change the first paragraph of 30.2.3 as shown:

A containment relationship is a structuring relationship for managed objects in which the existence of a managed object is dependent on the existence of a containing managed object. The contained managed object is said to be the subordinate managed object, and the containing managed object the superior managed object. The containment relationship is used for naming managed objects. The local containment relationships among object classes are depicted in the entity relationship diagrams, Figure 30–3 through Figure 30–6. These figures show the names of the object classes and whether a particular containment relationship is one-to-one, one-to-many or many-to-one. For further requirements on this topic, see IEEE Std 802.1F-1993. PSE and PoDL PSE management are ~~is~~ only valid in a system that provides management at the next higher containment level, that is, either a DTE, or in the case of PSE management only, a repeater or Midspan with management.

Change Figure 30-3 by adding oPoDLPSE entity as shown in red below:



Note—The objects oAggregator, oAggregationPort, oAggPortStats and oAggPortDebugInformation are deprecated by IEEE Std 802.1AX-2008.

Figure 30–3— DTE System entity relationship diagram

30.2.5 Capabilities

Change the first paragraph in 30.2.5 and insert Table 30–10

This standard makes use of the concept of packages as defined in ISO/IEC 10165-4:1992 as a means of grouping behaviour, attributes, actions, and notifications within a managed object class definition. Packages may either be mandatory, or be conditional, that is to say, present if a given condition is true. Within this standard capabilities are defined, each of which corresponds to a set of packages, which are components of a number of managed object class definitions and which share the same condition for presence. Implementation of the appropriate Basic and Mandatory packages is the minimum requirement for claiming conformance to IEEE 802.3 Management. Implementation of an entire optional capability is required in order to claim conformance to that capability. The capabilities and packages for IEEE 802.3 Management are specified in Table 30–1a through ~~Table 30-9~~ Table 30–10.

Change the ninth paragraph as follows:

For managed PSEs, the PSE Basic Package is mandatory and the PSE Recommended Package is optional. For managed PoDL PSEs, the PoDLPSE Basic Package is mandatory and the PoDLPSE Recommended Package is optional. For managed PDs, the PD Basic Package is mandatory. For a managed PSE to be conformant to this standard, it shall fully implement the PSE Basic Package. For a managed PoDL PSE to be conformant to this standard, it shall fully implement the PoDLPSE Basic Package. For a managed PD to be conformant to this standard, it shall fully implement the PD Basic Package. For a managed PSE to be conformant to the optional Recommended Package it shall implement that entire package. For a managed PoDL PSE to be conformant to the optional PoDL PSE Recommended Package it shall implement that entire package. PSE, PoDL PSE and PD management is optional with respect to all other CSMA/CD management.

Insert new Table 30-10 as follows:

Table 30–10—PoDL PSE capabilities

				PoDLPSE Basic Package (mandatory)	PoDLPSE Recommended Package (optional)
oResourceTypeID managed object					
	aResourceTypeIDName	ATTRIBUTE	GET	X	
	aResourceInfo	ATTRIBUTE	GET	X	
oPoDLPSE managed object class (30.15)					
	aPoDLPSEID	ATTRIBUTE	GET	X	
	aPoDLPSEAdminState	ATTRIBUTE	GET	X	
	aPoDLPSEPowerDetectionStatus	ATTRIBUTE	GET	X	
	aPoDLPSEType	ATTRIBUTE	GET	X	
	aPoDLPSEDetectedPDType	ATTRIBUTE	GET	X	
	aPoDLPSEDetectedPDPowerClass	ATTRIBUTE	GET	X	
	aPoDLPSEInvalidSignatureCounter	ATTRIBUTE	GET		X
	aPoDLPSEInvalidClassCounter	ATTRIBUTE	GET		X
	aPoDLPSEPowerDeniedCounter	ATTRIBUTE	GET		X
	aPoDLPSEOverLoadCounter	ATTRIBUTE	GET		X
	aPoDLPSEMaintainFullVoltageSignatureAbsentCounter	ATTRIBUTE	GET		X
	aPoDLPSEActualPower	ATTRIBUTE	GET		X
	aPoDLPSEPowerAccuracy	ATTRIBUTE	GET		X
	aPoDLPSECumulativeEnergy	ATTRIBUTE	GET		X
	acPoDLPSEAdminControl	ACTION		X	
Common Attributes Template					
	aCMCounter	ATTRIBUTE	GET		X

Insert new sub-clause 30.15 after 30.14 (as inserted by IEEE Std 802.3br-201x) as follows:

30.15 Layer management for Single-pair Power over Data Lines (PoDL)

30.15.1 PoDL PSE managed object class

This subclause formally defines the behaviours for the oPoDLPSE managed object class attributes and actions.

30.15.1.1 PoDL PSE attributes

30.15.1.1.1 aPoDLPSEID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of aPoDLPSEID is assigned so as to uniquely identify a PoDL PSE among the subordinate managed objects of the containing object.;

30.15.1.1.2 aPoDLPSEAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

enabled	PoDL PSE functions enabled
disabled	PoDL PSE functions disabled

BEHAVIOUR DEFINED AS:

A read-only value that identifies the operational state of the PoDL PSE functions. An interface which can provide the PoDL PSE functions specified in Clause 104 is enabled to do so when this attribute has the enumeration “enabled.” When this attribute has the enumeration “disabled” the interface acts as if it had no PoDL PSE function. The operational state of the PSE function can be changed using the acPoDLPSEAdminControl action.

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the PSE Enable bit specified in 45.2.7b.1.2.

30.15.1.1.3 aPoDLPSEPowerDetectionStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

unknown	initializing, error, or true state unknown
disabled	PoDL PSE disabled
searching	PoDL PSE searching
deliveringPower	PoDL PSE delivering power
sleep	PoDL PSE sleep

BEHAVIOUR DEFINED AS:

A read-only value that indicates the current status of the PoDL PSE.

The enumeration “disabled” indicates that the PoDL PSE State diagram (see Figure 104–4) is in the state DISABLED. The enumeration “deliveringPower” indicates that the PoDL PSE State diagram is in the state POWER_ON or SETTLE_SLEEP. The enumeration “sleep” indicates that the PoDL PSE State diagram is in the state SLEEP. The enumeration “searching” indicates the PoDL PSE State diagram is in either the DETECTION, CLASSIFICATION, CLASSIFICATION_EVAL, or POWER_UP states.

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the PSE Status bits specified in 45.2.7b.2.9.

30.15.1.1.4 aPoDLPSEType

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

unknown	initializing, true state not yet known
typeA	Type A PoDL PSE
typeB	Type B PoDL PSE
typeC	Type C PoDL PSE

BEHAVIOUR DEFINED AS:

A read-only value that identifies the PoDL PSE Type specified in 104.4.1.

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the PSE Type bits specified in 45.2.7b.2.7.

30.15.1.1.5 aPoDLPSEDetectedPDType

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

unknown	initializing, true state not yet known
typeA	Type A PoDL PD
typeB	Type B PoDL PD
typeC	Type C PoDL PD

BEHAVIOUR DEFINED AS:

A read-only value that indicates the Type of the detected PoDL PD as specified in 104.5.1. This value is only valid while a PD is being powered, that is the attribute aPoDLPSEPowerDetectionStatus is reporting the enumeration “deliveringPower”.

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the PD Type bits specified in 45.2.7b.3.1.

30.15.1.1.6 aPoDLPSEDetectedPDPowerClass

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

unknown	initializing, true state not yet known
class0	Class 0 PoDL PD
class1	Class 1 PoDL PD
class2	Class 2 PoDL PD
class3	Class 3 PoDL PD
class4	Class 4 PoDL PD
class5	Class 5 PoDL PD
class6	Class 6 PoDL PD
class7	Class 7 PoDL PD
class8	Class 8 PoDL PD
class9	Class 9 PoDL PD

BEHAVIOUR DEFINED AS:

A read-only value that indicates the Class of the detected PoDL PD as specified in Table 104–1. This value is only valid while a PD is being powered, that is the attribute aPoDLPSEPowerDetectionStatus is reporting the enumeration “deliveringPower”.

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the PD Class bits specified in 45.2.7b.2.8.

30.15.1.1.7 aPoDLPSEInvalidSignatureCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PoDL PSE state diagram (see Figure 104–4) transitions directly from the state DETECTION to the state RESTART.

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the invalid signature bit specified in 45.2.7b.2.3.

30.15.1.1.8 aPoDLPSEInvalidClassCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PoDL PSE state diagram (see Figure 104–4) transitions directly from the state CLASSIFICATION to the state RESTART due to the pi_detecting variable being asserted false and the pi_sleeping variable being asserted true or when PSE state diagram transitions directly from the state CLASSIFICATION_EVAL to the state RESTART due to the valid_class variable being false.

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the class timeout bit specified in 45.2.7b.2.4.

30.15.1.1.9 aPoDLPSEPowerDeniedCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PoDL PSE state diagram (see Figure 104–4) transitions directly from the state CLASSIFICATION_EVAL to the state RESTART due to power_not_available variable being true.

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the power denied bit specified in 45.2.7b.2.1.

30.15.1.1.10 aPoDLPSEOverLoadCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 13 counts per 10 seconds.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PoDL PSE state diagram (see Figure 104–4) enters the OVERLOAD state.

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the overload bit specified in 45.2.7b.2.5.

30.15.1.1.11 aPoDLPSEMaintainFullVoltageSignatureAbsentCounter

see added text on next page

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 33 counts per 10 seconds.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PoDL PSE state diagram (see Figure 104–4) enters the SETTLE_SLEEP state.

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the Maintain Full Voltage Signature Absent bit specified in 45.2.7b.2.6.

30.15.1.2 aPoDLPSEActualPower

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

An integer value indicating present (actual) power being supplied by the PoDL PSE as measured at the MDI in milliwatts. The behaviour is undefined if the state of aPoDLPSE-PowerDetectionStatus is anything other than “deliveringPower”. The sampling frequency and averaging are vendor-defined.

30.15.1.3 aPoDLPSEPowerAccuracy

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A signed integer value indicating the accuracy associated with aPoDLPSEActualPower in milliwatts.

30.15.1.4 aPoDLPSECumulativeEnergy

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. The counter has a maximum increment rate of 100,000 per second.

BEHAVIOUR DEFINED AS:

A count of the cumulative energy supplied by the PoDL PSE, measured at the MDI, and expressed in units of millijoules.

30.15.2 PoDL PSE actions

30.15.2.1 acPoDLPSEAdminControl

ACTION

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

enabled	PoDL PSE functions enabled
disabled	PoDL PSE functions disabled

BEHAVIOUR DEFINED AS:

This action provides a means to alter aPoDLPSEAdminState.;

30.15.1.1.12 aPoDLPSESystemType

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

unknown : initializing, true state not yet known

Plug-And-Play PoDL PSE

Fast-Startup PoDL PSE

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

Insert row to add Power Unit Registers to Table 45-1 as changed by P802.3bn as shown (unchanged rows not shown):

Table 45–1—MDIO Manageable Device addresses

Device address	MMD name
13	Power Unit
14~~13~~ through 28	Reserved

Change reserved row m.5.15:12 and insert row to add Power Unit Registers in Table 45-2 as shown, below reserved for m.5.15:12 and immediately above row for register m.5.11 (unchanged rows not shown):

Table 45–2—Devices in package registers bit definitions

Bit(s)[a]	Name	Description	R/W[b]
m.5.15:~~12~~ 13	Reserved	Value always 0	RO
m.5.12	Power Unit present	1 = Power Unit present in package 0 = Power Unit not present in package	RO

[a]m = address of MMD accessed (see Table 45–1)
[b]RO = Read only

Insert the following subclauses for Power Unit Registers immediately after 45.2.7a.6 (10GPASS-XR receive MER measurement registers) added by P802.3bn.

Editor's Note (to be removed prior to publication) - IEEE P802.3bq, bz, and bn insert Table 45-211d, which these tables are subsequent to in the text of clause 45.

45.2.7b Power Unit Registers

The assignment of registers in the Power Unit MMD is shown in Table 45–211h.

Table 45–211h—Power Unit MMD Registers

Register address	Register name	Subclause
13.0	Single-Pair PSE Control	45.2.7b.1
13.1	Single-Pair PSE Status 1	45.2.7b.2
13.2	Single-Pair PSE Status 2	45.2.7b.3

45.2.7b.1 Single-Pair PSE Control register (Register 13.0)

The assignment of bits in the Single-Pair PSE Control register is shown in Table 45–211i. The default value for each bit of the Single-Pair PSE Control register should be chosen so that the initial state of the PSE upon power up or reset is a normal operational state without management intervention.

Table 45–211i—Single-Pair PSE Control register bit definitions

Bit(s)	Name	Description	R/W[a]
13.0.15:2	Reserved	Value always 0	RO
13.0.1	Enable Power Classification	1 = Power classification enabled 0 = Power classification disabled	R/W
13.0.0	PSE Enable	1= PSE Enabled 0= PSE Disabled	R/W

[a]R/W = Read/Write, RO = Read Only

45.2.7b.1.1 Enable power classification (13.0.2)

The power classification function is enabled by setting bit 13.0.2 to one and disabled by setting bit 13.0.2 to zero. This bit maps to the mr_sccp_enabled variable.

45.2.7b.1.2 PSE Enable (13.0.0)

Setting this bit disables detection and establishes the PSE as a Plug-And-Play System PSE. Clearing this bit enables detection and establishes the PSE as an Fast Startup System PSE.

When bit 13.0.1 is set to zero, the PSE function shall be disabled. When bit 13.0.1 is set to one, the PSE function shall be enabled. This register bit maps to the mr_pse_enable variable.

45.2.7b.2 Single-Pair PSE Status 1 register (Register 13.1)

The assignment of bits in the Single-Pair PSE Status 1 register is shown in Table 45–211j.

Table 45–211j—Single-Pair PSE Status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
13.1.15	Power Removed	1 = Power has been removed due to fault 0 = Power has not been removed	RO/ LH
13.1.14	Valid Signature	1 = Valid PD signature detected 0 = No valid PD signature detected	RO/ LH
13.1.13	Invalid Signature	1 = Invalid PD signature detected 0 = No invalid PD signature detected	RO/ LH
13.1.12	Class Timeout	1 = Classification timeout condition detected 0 = No Classification timeout condition detected	RO/ LH
13.1.11	Overload	1 = Overload condition detected 0 = No overload condition detected	RO/ LH
13.1.10	MFVS Absent	1 = MFVS absent condition detected 0 = No MFVS absent condition detected	RO/ LH
13.1.9:7	PSE Type	1 x x = Reserved 0 1 1 = Reserved 0 1 0 = Type C PSE 0 0 1 = Type B PSE 0 0 0 = Type A PSE	RO
13.1.6:3	PD Class	1 1 x x = Reserved 1 0 1 x = Reserved 1111 = unknown 1 0 0 1 = Class code 9 1 0 0 0 = Class code 8 0 1 1 1 = Class code 7 0 1 1 0 = Class code 6 0 1 0 1 = Class code 5 0 1 0 0 = Class code 4 0 0 1 1 = Class code 3 0 0 1 0 = Class code 2 0 0 0 1 = Class code 1 0 0 0 0 = Class code 0	RO
13.1.2:0	PSE Status	1 1 1 = Unknown 1 1 0 = Reserved 1 0 1 = Reserved 1 0 0 = Error 0 1 1 = Searching 0 1 0 = Delivering power 0 0 1 = Sleeping 0 0 0 = Disabled	RO

[a]RO = Read Only, LH = Latching High

45.2.7b.2.1 Power Removed(13.1.15)

When read as a one, bit 13.1.15 indicates that voltage at the PI has been removed. This bit shall be set to one when the PSE state diagram (see Figure 104–4) enters the state OVERLOAD. The Power Removed bit shall be implemented with latching high behavior as defined in 45.2.

45.2.7b.2.2 Valid Signature (13.1.14)

When read as a one, bit 13.1.14 indicates that a valid signature has been detected. This bit shall be set to one when mr_valid_signature transitions from FALSE to TRUE. The Valid Signature bit shall be implemented with latching high behavior as defined in 45.2.

45.2.7b.2.3 Invalid Signature (13.1.13)

When read as a one, bit 13.1.13 indicates that an invalid signature has been detected. This bit shall be set to one when the PSE detection state diagram (see Figure 104–5) enters the state IDLE_DETECT. The Invalid Signature bit shall be implemented with latching high behavior as defined in 45.2.

45.2.7b.2.4 Class Timeout(13.1.12)

When read as a one, bit 13.1.12 indicates that a Classification timeout condition has been detected. The Class Timeout bit shall be set to one when the PSE state diagram (see Figure 104–4) transitions directly from the state CLASSIFICATION_EVAL to RESTART due to the pi_detecting variable being asserted false and the pi_sleeping variable being asserted true. The Class Timeout bit shall be implemented with latching high behavior as defined in 45.2.

45.2.7b.2.5 Overload (13.1.11)

When read as a one, bit 13.1.11 indicates that an overload condition has been detected. This bit shall be set to one when the PSE state diagram (see Figure 104–4) enters the state OVERLOAD. The Overload bit shall be implemented with latching high behavior as defined in 45.2.

45.2.7b.2.6 MFVS Absent (13.1.10)

When read as a one, bit 13.1.10 indicates that an MFVS Absent condition has been detected. The MFVS Absent bit shall be set to one when the PSE state diagram (see Figure 104–4) transitions directly from the state POWER_ON to SETTLE_SLEEP due to tmfvdo_timer_done being asserted. The MFVS Absent bit shall be implemented with latching high behavior as defined in 45.2.

45.2.7b.2.7 PSE Type (13.1.9:7)

Bits 13.1.9:7 report the PSE Type of the PSE as specified in 104.4.1. When read as '000', bits 13.1.9:7 indicate a Type A PSE, when read as '001' a Type B PSE is indicated, and when read as '010' a Type C PSE is indicated.

45.2.7b.2.8 PD Class (13.1.6:3)

insert "1111, ie: "unknown" until the classification function has successfully completed." below

Bits 13.1.6:3 report the PD Class of a detected PD as specified in 104.5.2. The value in this register is ~~valid while a PD is connected, i.e., while the PSE Status (13.1.2:0) bits are reporting "delivering power".~~ When read as '0000' bits 13.1.2:0 a Class 0 PD is indicated, when read as a '0001' a Class 1 PD is indicated, when read as a '0010' a Class 2 PD is indicated, when read as a '0011' a Class 3 PD is indicated, when read as a '0100' a Class 4 PD is indicated, when read as a '0101' a Class 5 PD is indicated, when read as a '0110' a Class 6 PD is indicated, when read as a '0111' a Class 7 PD is indicated, when read as '1000' a Class 8 PD is indicated, and when read as a '1001' a Class 9 PD is indicated.

45.2.7b.2.9 PSE Status (13.1.2:0)

Bits 13.1.2:0 report the current status of the PSE. When read as '000', bits 13.1.2:0 indicate that the PSE state diagram (see Figure 104–4) is in the state DISABLED. When read as '010', bits 13.1.2:0 indicate that the PSE state diagram is in the state POWER_ON. When read as '011', bits 13.1.2:0 indicate that the PSE

state diagram is in any of the following states: DETECTION, CLASSIFICATION, CLASSIFICATION_EVAL, or POWER_UP. When read as '100', bits 13.1.2:0 indicate that the PSE state diagram is in the state OVERLOAD. When read as '101', bits 13.1.2:0 indicate that the PSE state diagram is in the state IDLE due to the variable overload_detected = true. When read as '001', bits 13.1.2:0 indicate that the PSE state diagram is in a state other than those listed above.

45.2.7b.3 Single-Pair PSE Status 2 register (Register 13.2)

The Single-Pair PSE Status 2 register is an extension of the Single-Pair PSE Status 1 register. Assignment of bits in the Single-Pair PSE Status 2 register is shown in Table 45–211k.

Table 45–211k—Single-Pair PSE Status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
13.2.15:3	Reserved	Value always 0	RO
13.2.2:0	PD Type	1 x x = Reserved 0 1 1 = Reserved 0 1 0 = Type C PD 0 0 1 = Type B PD 0 0 0 = Type A PD 111 = unknown	RO

[a]RO = Read Only, LH = Latching High

45.2.7b.3.1 PD Type (13.2.2:0)

Bits 13.2.2:0 report the PD Type of a detected PD as specified in 104.5.1. When read as '000', bits 13.2.2:0 indicate a Type A PD, when read as '001' a Type B PD is indicated, and when read as '010' a Type C PD is indicated.The value in this register is ~~valid while a PD is connected, i.e., while the PSE Status (13.1.2:0) bits are reporting "delivering power".~~ Insert "111 ie; "unknown" until a successful classification and identification of the PD type has completed and the PSE Status (13.1.2:0) bits are reporting "delivering power"

45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, MDIO interface

45.5.3 Major capabilities/options

Insert the following row at the bottom of the Major capabilities/options table

Item	Feature	Subclause	Value/Comment	Status	Support
*PODL	Implementation of Single-Pair Power over Data Lines	45.2.7b		O	Yes [ ] No [ ] N/A[ ]

45.5.3.13b Single-Pair Power over Data Line management functions

Insert 45.5.3.13b after 45.5.3.13b as shown below