200 Gb/s over 30 m OM4 Objective: BER Floor Optimization and Baseline Link Update

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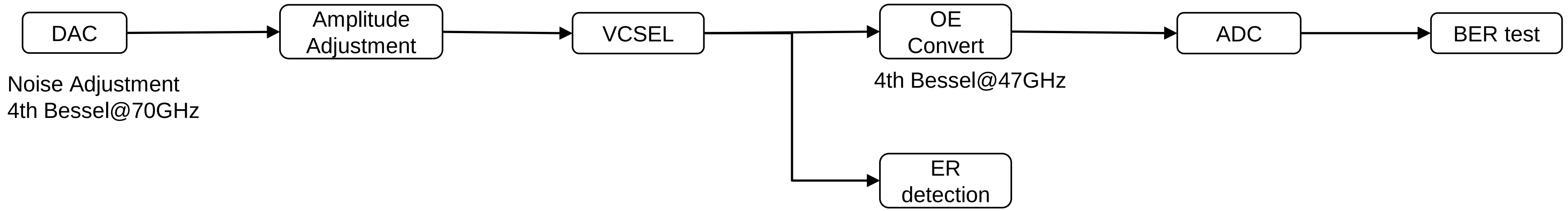
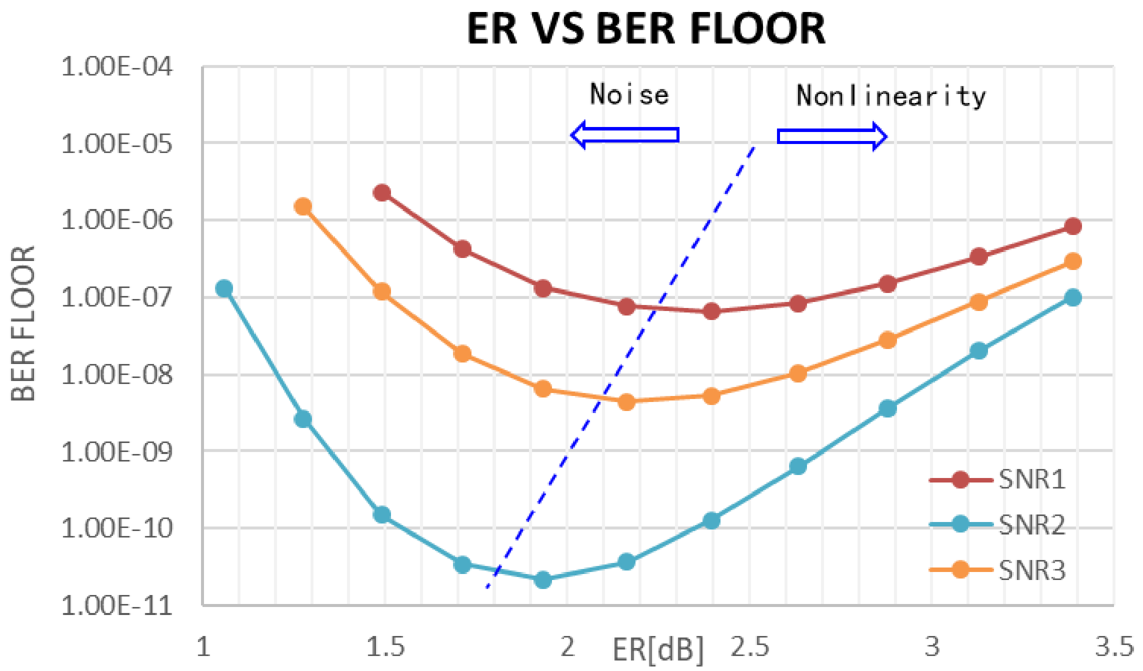
The Importance of BER Floor minimization

- The Bit Error Floor is an important metric to optimize.
- Hyperscalers are supportive of any efforts to improve performance margins of future PMDs.
- Hyperscalers already impose additional minimum error floor and FEC bins beyond what's required in current IEEE specs. It is necessary to ensure robust performance on AI backend networks.
- Some transceiver technologies have more margin that others. Typical error floors for SiP or EML-based DR transceivers are orders of magnitude better than those of VCSEL-based.
- It is critical for a future VCSEL based solution to optimize toward a lower error floor.

ER VS BER Floor





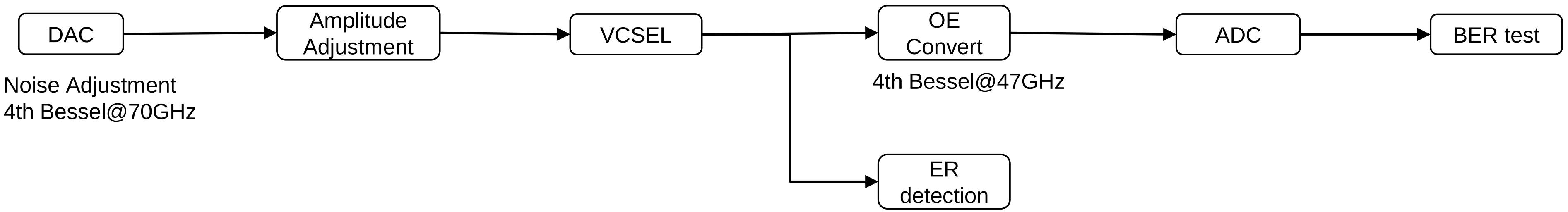
Simulation Process

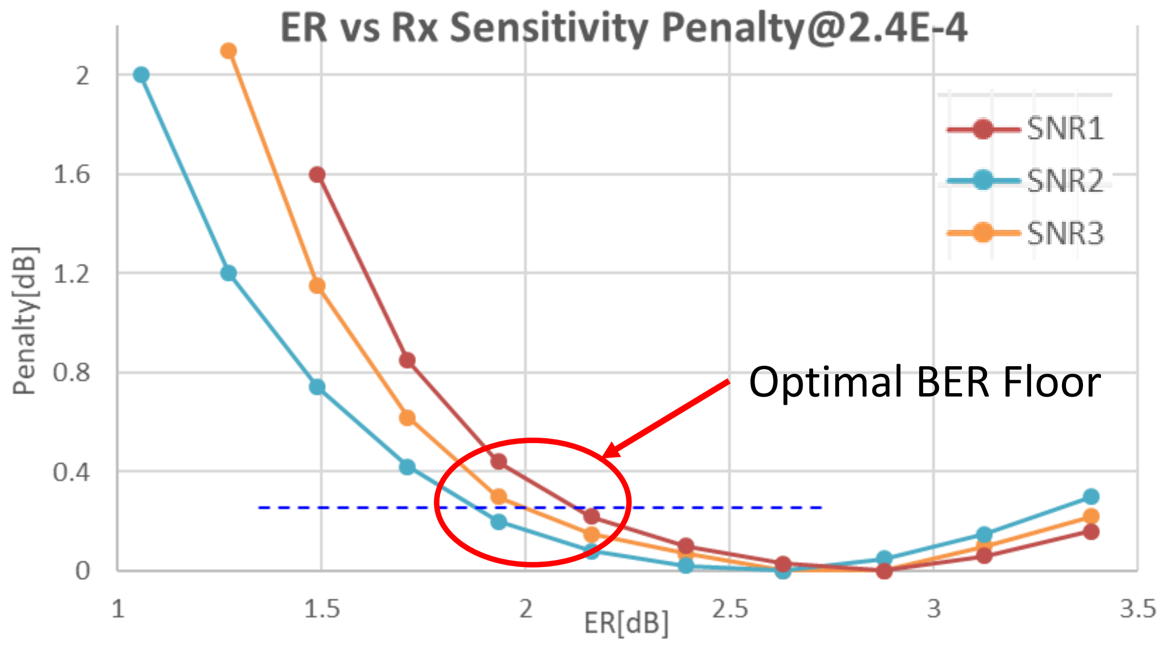
- VCSEL characteristics extracted from real devices
- Noise is adjusted through electrical SNR
- ER is adjusted thought DAC output amplitude
- Ber floor is measured and plotted for different SNR and ER

Observation

- As SNR decreases, the degradation of the BER floor is more driven by nonlinearity
- For BER optimization ER decreases from 2.5 dB to 2 dB.

ER VS Rx Sensitivity Penalty and Impact on Error Floor





Simulation

- VCSEL characteristics extracted from real devices
- Noise is adjusted through electrical SNR
- ER is adjusted thought DAC output amplitude
- For each SNR scenarios, the ER penalty is plotted

Observation

- The optimal ER and SNR are intentionally detuned from the ER that is optimal for a given SNR level to minimize the BER floor, resulting in a 0.2 dB sensitivity penalty when the ER changes from 2 dB to 2.5 dB.

ERROR FLOOR OPTIMIZATION RESULTS IN AN ADDITIONAL LINK PENALITY

ER Optimization at 200 Gb/s MMF

We observe a tendency for ER to decrease with higher performance devices

- As the bandwidth of VCSEL chips increases, the ER will gradually decrease.
- 200G bit/s system tend to employ larger pre-emphasis, which reduces the ER.

Benefits from lower ER

- Reduce DSP output amplitude to lower power consumption.
- ER can be intentionally detuned to minimize the Error floor

Re-evaluation of optimal ER is required for 200 Gb/s MMF links

- Propose to reduce the ER from 2.5 dB to 2 dB for 200 Gb/s MMF.

Illustrative Link budgets

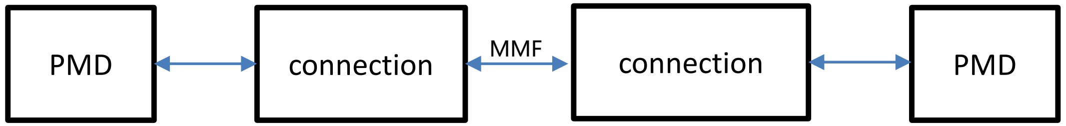
Description	200GBASE-xx1 400GBASE-xx2 800GBASE-xx4 1.6TBASE-xx8	Unit
	OM4	
Effective modal bandwidth at 850 nm	4700	MHz.km
Power budget (for max TDECQ)	TBD	dB
Operating distance	0.5 To 30/50	m
Channel insertion loss	1.6	dB
Maximum discrete reflectance	-35	dB
Allocation for penalties (for max TDECQ)	TBD	dB
Additional insertion loss allowed	0.1	dB

ISO-IEC 14763-3 / 11801

For installations tested in accordance with ISO/IEC specifications, the following maximum limits apply to the various cable plant components.

Item	Specification
Connector loss	0.75 dB
Splice loss	0.3 dB
850 nm	3.5 dB/km
1300 nm	1.5 dB/km

Table 2, ISO-IEC cable plant specification



The channel Insertion loss=0.1(fiber)+1.5(connector)=1.6dB

The channel insertion loss is calculated using maximum distance 30m and optical fiber attenuation of 3.5dB/km at 850nm plus an allocation for connection and splice loss

Proposing to maintain 1.6dB channel insertion loss and 0.1dB additional insertion loss, the same as 100G MMF VR1

Summary

- For 200G MMF, ER will reduce due to the limited VCSEL bandwidth and more pre-emphasis compensation.
- By analyzing ER vs Ber floor and RX sensitivity, Propose to reduce the ER from 2.5 dB to 2 dB for 200G MMF.
- Propose maintain 1.6dB channel insertion loss and 0.1dB additional insertion loss.

Illustrative Baseline Preview

Illustrative Transmitter Specifications

Description	200GBASE-xx1 400GBASE-xx2 800GBASE-xx4 1.6TBASE-xx8	Unit
Signaling rate, each lane (range)	TBD	GBd
Modulation Format	PAM4	
Lane wavelengths (range)	844~863	nm
RMS spectral width	TBD	nm
Average launch power, each lane (max)	TBD	dBm
Average launch power, each lane (min)	TBD	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane(max)	TBD	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane(min) for TDECQ < 1.8 dB for 1.8 dB ≤ TDECQ ≤ TDECQ (max)	TBD TBD TBD	 dBm dBm
Transmitter and dispersion eye closure (TDECQ), each lane (max)	TBD	dB
TECQ (max)	TBD	dB
Average launch power of OFF transmitter, each lane (max)	-30	dBm
Transmitter power excursion, each lane (max)	TBD	dB
Extinction ratio, each lane, (min)	TBD	dB
Transmitter transition time (max)	8	ps
Transmitter over/under-shoot (max)	TBD	%
RIN_xOMA (max)	TBD	dB/Hz
Optical return loss tolerance (max)	TBD	dB
Encircled flux	≥86% at 19 um ≤30% at 4.5 um	dB

Illustrative Receiver Specifications

Description	200GBASE-xx1 400GBASE-xx2 800GBASE-xx4 1.6TBASE-xx8	Unit
Signaling rate, each lane (range)	TBD	GBd
Modulation Format	PAM4	
Lane wavelengths (range)	844~863	nm
Damage threshold, each lane	TBD	dBm
Average receive power, each lane (max)	TBD	dBm
Average receive power, each lane (min)	TBD	dBm
Receive power, each lane (OMA_{outer}) (max)	TBD	dBm
Receiver reflectance (max)	TBD	dB
Receiver sensitivity (OMA_{outer}), each lane (max) for TECQ < 1.8dB for 1.8 dB ≤ TECQ ≤ SECQ	 TBD TBD	 dBm dBm
Stressed receiver sensitivity (OMA_{outer}), each lane (max)	TBD	dBm
Conditions of stressed receiver sensitivity test:		
SECQ	4.4	dB
OMA_{outer} of each aggressor lane[c]	3.5	dBm

Illustrative Link Budget

Description	200GBASE-xx1 400GBASE-xx2 800GBASE-xx4 1.6TBASE-xx8	Unit
	OM4	
Effective modal bandwidth at 850 nm	4700	MHz.km
Power budget (for max TDECQ)	TBD	dB
Operating distance	0.5 To 30	m
Channel insertion loss	TBD	dB
Maximum discrete reflectance	-35	dB
Allocation for penalties (for max TDECQ)	TBD	dB
Additional insertion loss allowed	TBD	dB