FEC/ Architecture/ Extender Sublayer

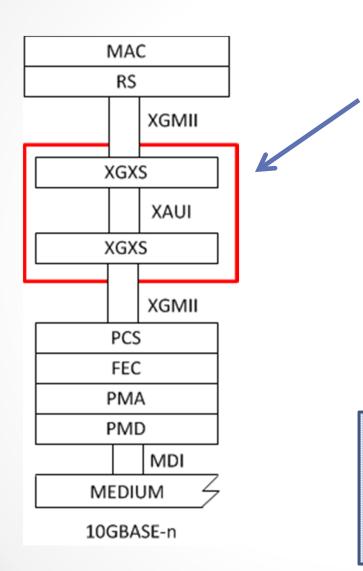
John D'Ambrosia, Dell

IEEE 802.3 400 Gb/s Ethernet Study Group
Logic Ad Hoc
August 20, 2013

Introduction

- Presentation is based on continuing discussions of my prior presentation to the Study Group in July.
 - o http://www.ieee802.org/3/400GSG/public/13_07/dambrosia_400_02_0713_.pdf

10 GbE Architecture



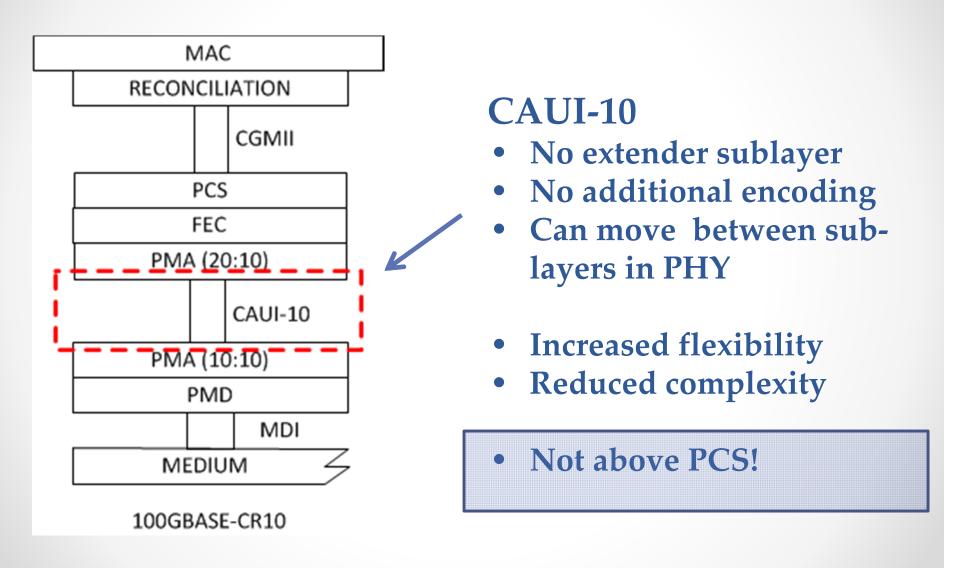
XGXS Sub-layer

- XGMII Extender contains XAUI
- 8B / 10B encoding / decoding
- Clock / data recovery in XGXS
- XGXS encoding does not match 10 GBASE-R (64b/66b) PCS
- Added complexity
- Limited flexibility

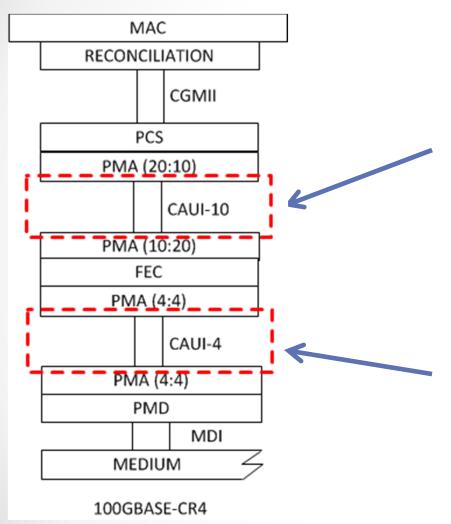
Multiple PCS's possible

• Clauses 48 (8B/10B), 49 (64B/66B), 55 (twisted pair PCS)

802.3ba 40 / 100 GbE Architecture



100GBASE-CR4 Architecture



CAUI-10

- No extender sublayer
- No additional encoding
- Can only be between PCS and top FEC

FEC

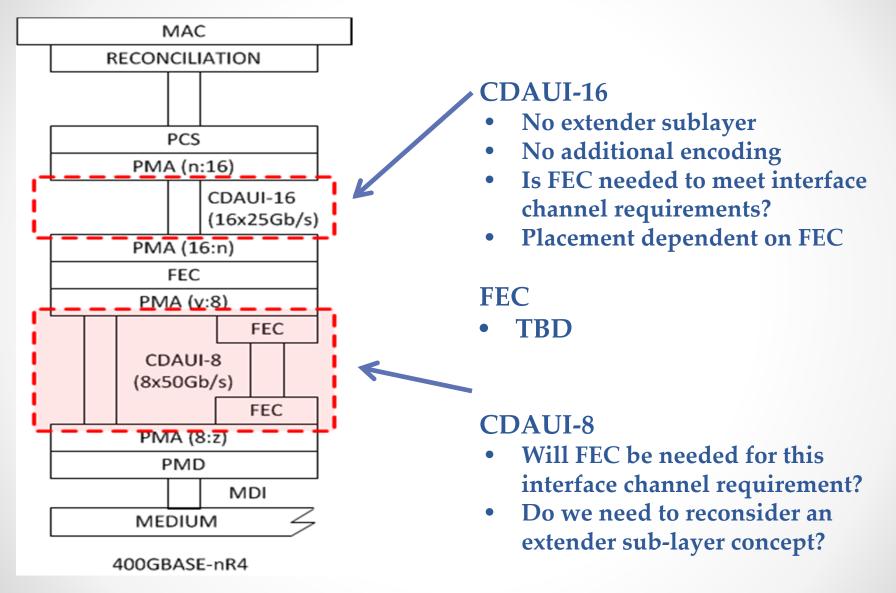
- Transcoding
- FEC encoding
- 4 lanes

CAUI-4

- No extender sublayer
- No additional encoding
- Can be between any sub-layers in PHY
- Added complexity / rules

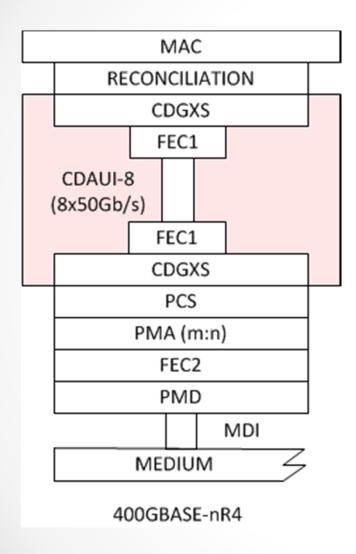
 IEEE 802.3 400 Gb/s Ethernet Study Group – Logic Adhoc Logic Ad Hoc, 20-Aug-2013

For Discussion



 IEEE 802.3 400 Gb/s Ethernet Study Group – Logic Adhoc Logic Ad Hoc, 20-Aug-2013

For Discussion Now



- Will we need multiple PCS?
 - WHO KNOWS?
- Assume CDGXS would include
 - Encoding
 - FEC
 - CDAUI-n electrical specifications
 - Alignment markers?
- Would the FEC in CDGXS be the same FEC for the PMD?
 - Can we assume this?
 - Do we need independence?
- While part of the physical layer specification (not PHY), we haven't defined an optional physical instantiation above the PCS since XGMII / XAUI. Suggest specific objective.

Summary

- Reminder: This presentation is focused on highlighting questions to be asked, not providing answers!
- FEC discussion is extending into "Extender SubLayer"
- If we recognize that we may want an interface above the PCS – recognize an objective regarding the CDGXS.
 - Specify an optional CDGXS (400 Gigabit Extender Sublayer)