

FORWARD ERROR CORRECTION FOR 400G: INITIAL THOUGHTS

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100G FEC AS IT STANDS TODAY

Currently two FEC layers are currently proposed for 100G Ethernet operation. Both are in draft form in Clause 91 of the 802.3bj revisions to the standard.

- A Reed-Solomon($N=528, K=514, m=10, T=7$) code that was designed for NRZ ~25Gb/s over backplane and co-ax channels but which will also be deployed in 100G optics.
- A Reed-Solomon($N=544, K=514, m=10, T=15$) code that was designed for PAM-4 ~25Gb/s over backplane channels but which may also be deployed in 100G optics.

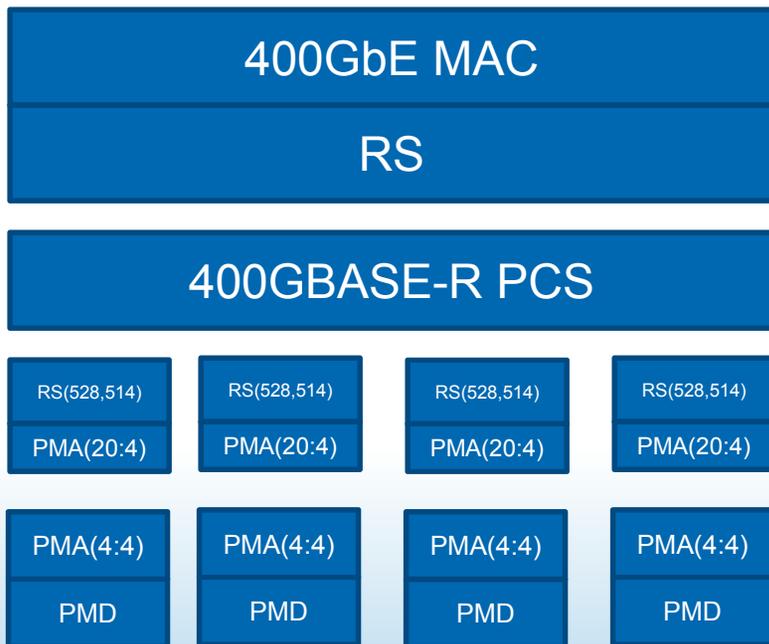
People will be building encoder and decoder solutions for these codes so it makes sense to leverage these codes if possible.

400G

- Initially a 400G link will probably consist of 16 lanes of ~25Gb/s¹.
- The aggregation of 4x100G links would also seem to be a likely use case.
- In these cases it is not unreasonable to assume that the PMD technologies and the channels are very similar to those used in 100G. Therefore the same FEC used in 100G seems like a reasonable starting point for analysis.

¹ See http://www.ieee802.org/3/400GSG/public/13_05/gustlin_400_01b_0513.pdf

400G: EXAMPLE A¹

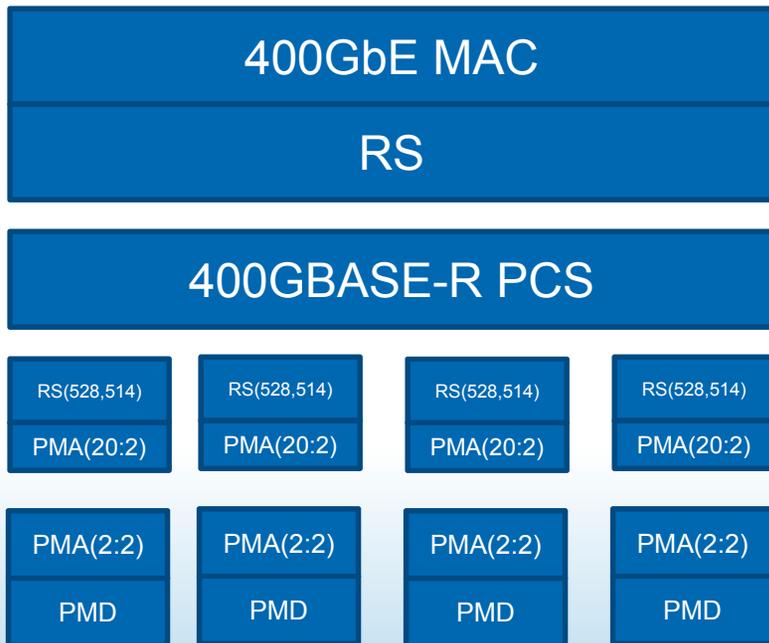


16 Lanes @ 25Gb/s per Lane

- Allows for re-use of the RS(528,514) FEC.
- Lane alignment across the 4 100G channels would have to be done in the 400GBASE-R PCS.
- This would not pull the FEC into the 400G PCS. Is that something we want or not?
- Latency and coding gain would be identical to the 100G use case. Makes sense for 25Gb/s PMD lanes.

¹ This architecture is based on the diagram to the left on page 9 of http://www.ieee802.org/3/400GSG/public/13_05/ghiasi_400_01a_0513.pdf

400G: EXAMPLE B



8 Lanes @ 50Gb/s per Lane

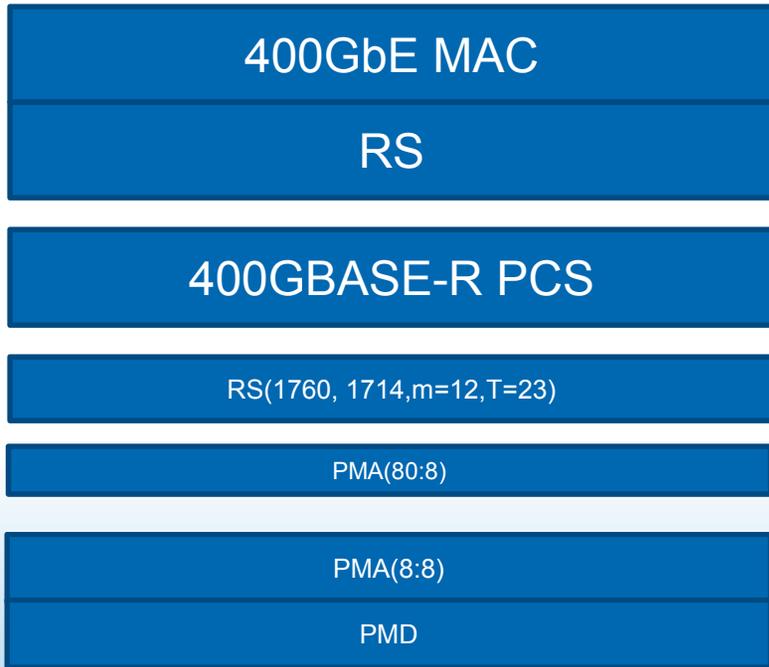
- Allows for re-use of the RS(528,514) FEC.
- Lane alignment across the 4 100G channels would have to be done in the 400GBASE-R PCS.
- This would not pull the FEC into the 400G PCS. Is that something we want or not?
- Latency and coding gain would be identical to the 100G use case. **This might not make sense for 50Gb/s PMD Lanes.**

LATENCY AND CODING GAIN

- As we migrate from ~25Gb/s PMD lanes to higher speeds (~50Gb/s??) we *might* want more coding gain.
- As we move to 400G is the 100ns FEC decode latency an acceptable number?
- We have some options here but there are some rules we must follow for the ECC to work. For an RS(N,K,m,T) we must ensure:
 - $\text{Log}_2(N) \leq m$.
 - $T \leq \text{floor}((N-K)/2)$.
- But even with these rules we can do some interesting things...

¹ See http://www.ieee802.org/3/400GSG/public/13_05/gustlin_400_01b_0513.pdf

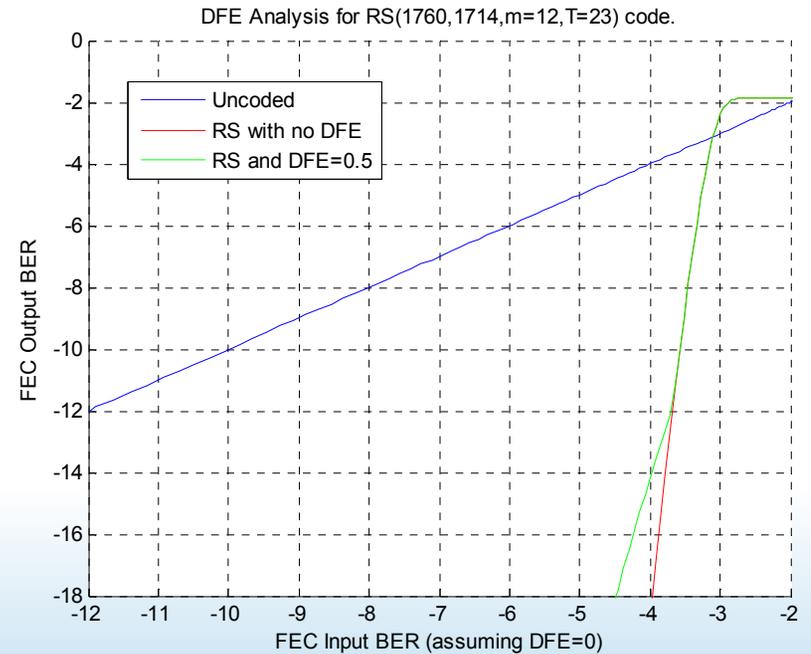
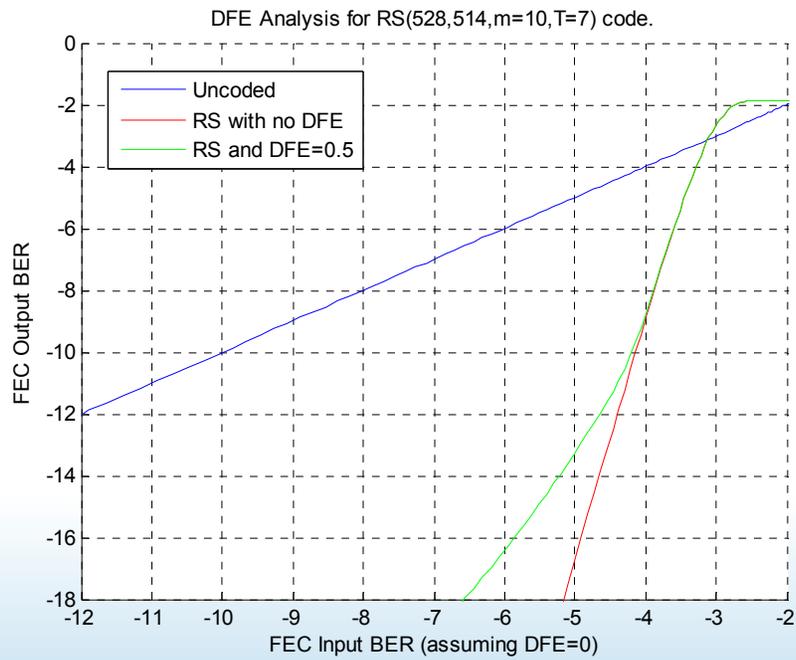
400G: EXAMPLE C: MORE GAIN



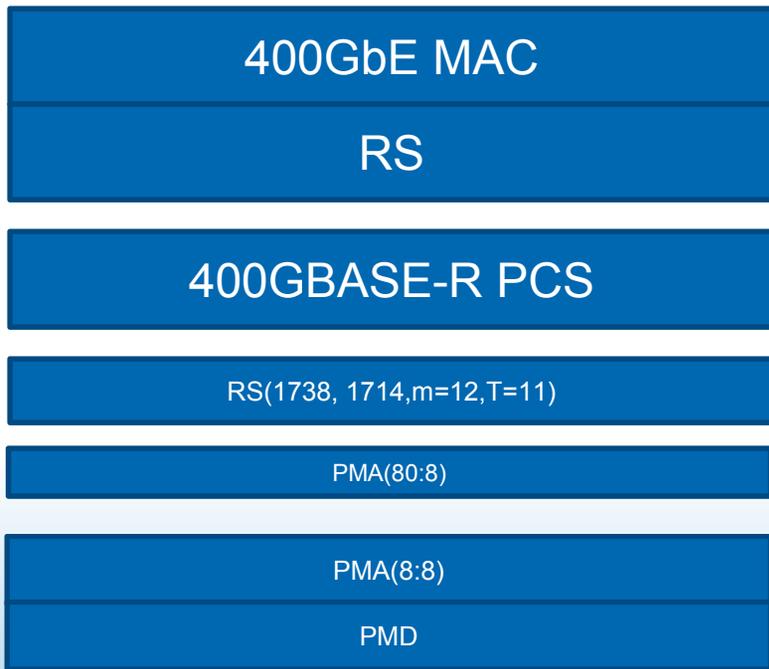
8 Lanes @ 50Gb/s per Lane

- Run a single FEC over all 400G.
- Modify N, K and m to ensure:
 - User payload fits.
 - Parity overhead the same.
- However this is a much more complex decoder (m is 12 not 10, block size is bigger and T is a lot bigger).
- Probably makes sense to reduce T which would allow us to drop baud rate.
- This example allow us to increase input BER from $\sim 3e-5$ to $\sim 2e-4$!

RS(1760,1714,M=12,T=23)



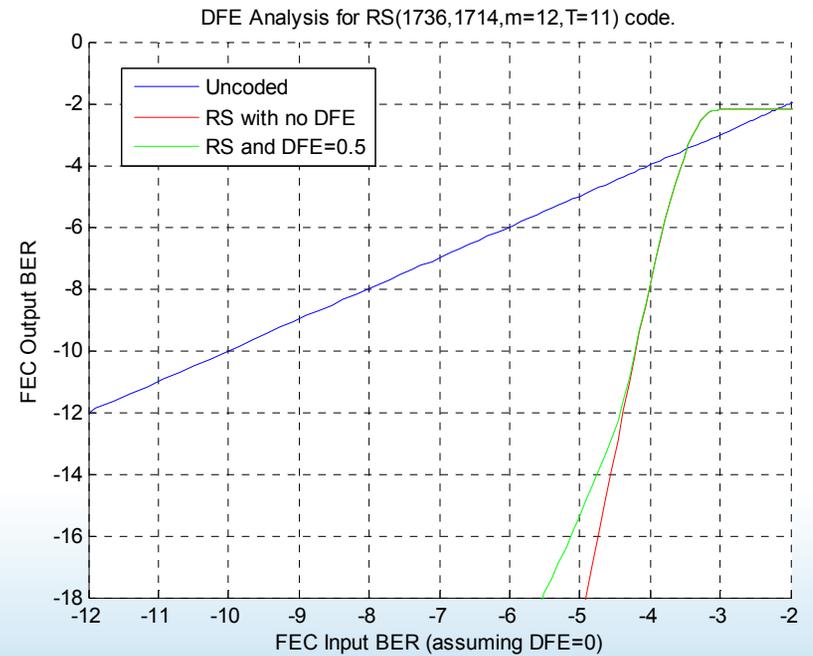
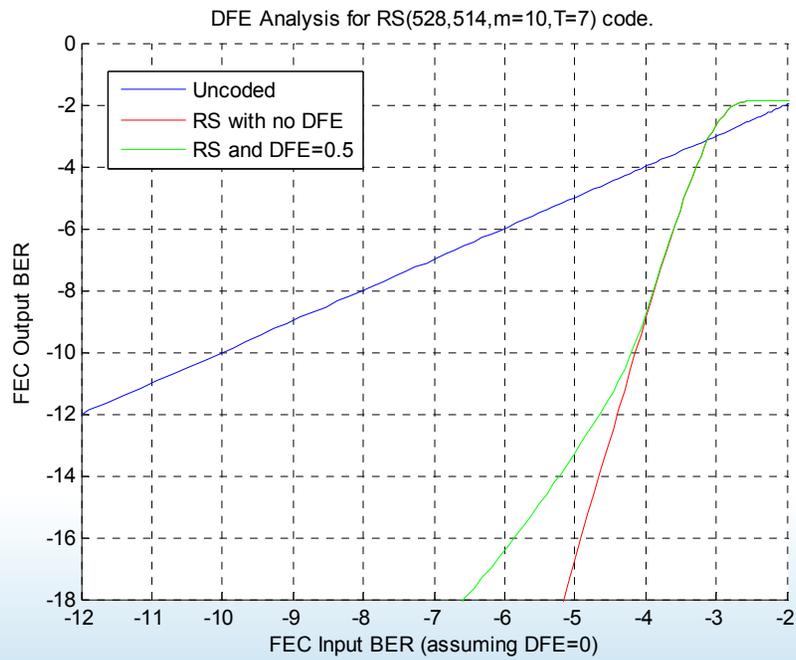
400G: EXAMPLE C: SAME GAIN AND LATENCY AS RS(528,514)



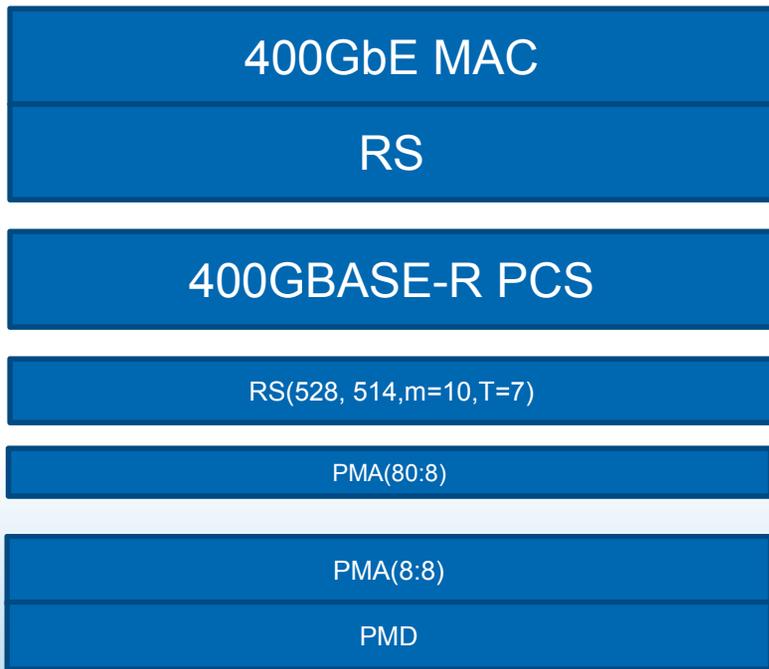
8 Lanes @ 50Gb/s per Lane

- Run a single FEC over all 400G.
- Modify N, K and m to ensure:
 - User payload fits.
 - ECC performance about the same.
- This is a more complex decoder (m is 12 not 10, block size is bigger and T is bigger).
- Note baud rate on the line is less which provides SNR gain in band-limited channels.
- This example allow us to reduce latency from 100ns to ~98 ns.

RS(1738,1714,M=12,T=11)



400G: EXAMPLE D: USE RS(528,514) OVER ALL LANES



8 Lanes @ 50Gb/s per Lane

- Run a single FEC over all 400G.
- Now need to determine how to map all 80 PCS lanes into FEC.
- This is a more complex decoder since its throughput is 400G/s not 100G/s.
- This example allow us to reduce latency from 100ns to 25 ns.

WE NEED TO COMPLETE THIS TABLE

Code	Relative Complexity	Input Ber @ 1e-12 output BER	Latency
4 x RS(528,514,10,7)	1	3e-5	100ns
RS(1760,1712,12,23)	??	2e-4	100ns
RS(1738,1712,12,11)	??	3e-5	98ns
RS(528,514,10,7)	1	3e-5	25ns
Others??			

CONCLUSIONS

- Lots of options exist and we can leverage off the Clause 91 FEC(s).
- Important to determine if:
 - Latency can stay at 100ns.
 - BER can stay at $\leq 1e-12$.

POTENTIAL STRAW POLL QUESTIONS FOR GENEVA

1. Do you wish to reuse the FEC in Clause 91 as much as possible for 400G?
Y. N. Don't Care.
2. Would you like to see the FEC integrated into the 400GBASE-R PCS?
Y. N. Don't Care.
3. Do you think the BER objective of at least $1e-12$ is sufficient for 400G?
Y. N. Don't Care.
4. Do you think the latency of the 400G FEC be reduced from the 100ns value of 100G FEC?
Y. N. Don't Care.