Commnent (#161, #191, #192, #193, #404, #405):

The following needs some updates: 79.3.2.6a, 79.3.2.6b, 79.3.2.6c.2, 79.3.2.6c.3, 79.3.2.6d.
The content of some of the items above are for a dual-signature but it doesn't say it.
The following concept was evaluated in order to decide how to fill in the following TLVs field for single and dual-signature PDs:

#	PSE Type	Operating over	Connected to a PD	TLV field		
				Y	A	B
				pd_requested_power pse_allocated_power	pd_req_power_mode(A) pse_allocated_power_Alt(A)	pd_req_power_mode(B) pse_allocated_power_Alt(B)
1	3/4	4-pairs	SS	1-999	0	0
2	3/4	2-pairs	SS	1-999	0	0
3	3/4	4-pairs	DS	1-999	1-499	1-499
	3/4	4-pairs with time delay until the 2nd mode is active too	DS	1-999	1-499	1-499
4	3/4	2-pairs	DS	1-499	1-499 if this mode/Alt is active. If not set to value 0.	1-499 if this mode/Alt is active. If not set to value 0.
	1/2	2-pairs	DS	1-499	1-499 if this mode/Alt is active. If not set to value 0.	1-499 if this mode/Alt is active. If not set to value 0.

Case #3: The value of column Y=A+B.
Case #4: The value of Y=A or Y=B pending the active pairs.

So rules are:

PD:

- single-signature => use single-sig fields

- dual-signature connected to a PSE operating over 2-pairs => use single-sig fields and the active mode/Alt(X)

- dual-signature connected to Type 3/4 PSEs operating over 4-pairs => use dual-sig fields and the sum value of them in the single-signature field.

PSE

- PSE connected to single-sig => use single-sig fields

- PSE that did not do connection check (2-pair PSE) => use single-sig fields and will be equal to the value of the active mode/Alt(X). The other non-active mode will set to value 0.

- PSE connected to dual-sig => use dual-sig fields and the single-signature field will be equal to A+B.

Suggested Remedy:

Make the following changes:

79.3.2.5 PD requested power value

For Type 3 and Type 4 single-signature PDs and Type 1 and Type 2 PDs, the PD requested power value field shall contain the PD's requested power value defined in Table 79–5. The fields for PD requested power value Mode A and PD requested power value Mode B in Table 79-6a shall be set to value 0.

For Type 3 and Type 4 dual-signature PDs connected to PSEs operating over 2-pairs mode, the PD requested power value field in Table 79–5 shall be set to be equal to field value of the active PD requested power value Mode (X) in Table 79–6a while the other non-active mode field shall be set value 0.

~~The PD requested power value field shall contain the PD's requested power value defined in Table 79–5. For Type 3 and Type 4 devices, the value should be (PD requested power value Mode A + PD requested power value Mode B).~~

"PD requested power value" is the maximum input average power (see 33.3.8.2 and 145.3.8.2) the PD wants to draw. "PD requested power value" is the power value at the input to the PD's PI.

Table 79–5—PD requested power value field

Bit	Function	Value/meaning
15:0	PD requested power value	~~Power = 0.1 × (decimal value of bits) Watts.~~ Power expressed in units of 0.1 W. Valid values for these bits are decimal 1 through ~~255~~999.

79.3.2.6 PSE allocated power value

For PSEs when supporting single-signature PDs and Type 1 and Type 2 PDs, the PSE allocated power value field shall contain the PSE's allocated power value defined in Table 79-6. The fields for PSE allocated power value Alternative A and PSE allocated power value Alternative B in Table 79-6b shall be set to value 0.

For PSEs operating over 2-pairs mode when supporting dual-signature PDs, the PSE allocated power value field in Table 79–6 shall be set to be equal to the field value of the active PSE allocated power value Alternative (X) in Table 79–6b while the other non-active Alternative field shall be set value 0.

~~The PSE allocated power value field shall contain the PSE's allocated power value defined in Table 79–6. For Type 3 and Type 4 devices, the value should be (PSE allocated power value Alternative A + PSE allocated power value Alternative B).~~

"PSE allocated power value" is the maximum input average power (see 33.3.8.2 and 145.3.8.2) the PSE expects the PD to draw. "PSE allocated power value" is the power at the input to the PD's PI. The PSE uses this value to compute PClass defined in 33.2.7 and 145.2.7.

Table 79–6—PSE allocated power value field

Bit	Function	Value/meaning
15:0	PSE allocated power value	~~Power = 0.1 × (decimal value of bits) Watts.~~ Power expressed in units of 0.1 W. Valid values for these bits are decimal 1 through ~~255~~999.

79.3.2.6a Dual-signature PD requested power value Mode A and Mode B

For dual-signature PDs operating over 4-pairs, the PD requested power value field shall contain the PD's requested power value defined in Table 79–6a over mode A and over mode B.
The fields for PD requested power value in Table 79-5 shall be set to the sum value of PD requested power value Mode A and PD requested power value Mode B in Table 79-6A.

If mode (X) became non-active while the other mode is active, prior to return to IDLE state, the PD requested power value Mode (X) field value shall be set to 0.

~~The PD requested power value field shall contain the PD's requested power value defined in Table 79–6a. For Type 3 and Type 4, the value should be (PD requested power value Mode A + PD requested power value Mode B). For Type 3 and Type 4, the PD requested power field defined in Table 79.3.2.5 is the sum of the PD requested power values defined in Table 79–6a.~~

Table 79–6a—PD requested power value field for Mode A and Mode B

Bit	Function	Value/meaning
15:0	PD requested power value Mode A	Power expressed in units of 0.1 W. Valid values for these bits are decimal 1 through 499.
15:0	PD requested power value Mode B	Power expressed in units of 0.1 W. Valid values for these bits are decimal 1 through 499.

~~The value for the Mode A field should be (PD requested power value – PD requested power value Mode B). The value for the Mode B field should be (PD requested power value – PD requested power value Mode A).~~

"PD requested power value Mode A" and "PD requested power value Mode B" are the maximum input average power levels (see 145.3.8.2) the PD wants to draw for the respective pairset. "PD requested power value Mode A" and "PD requested power value Mode B" are the power values at the input to the PD's PI.

79.3.2.6b PSE allocated power value Alternative A and Alternative B

For Type 3 and Type 4 PSE operating over 4-pairs when supporting dual-signature PD, the PSE allocated power value Alternative A field and the PSE allocated power value Alternative B field shall contain the values in Table 79-6b. The sum value of PSE allocated power value Alternative A field and the PSE allocated power value Alternative B field shall be set in PSE allocated power value field in Table 79–6.

~~The PSE allocated power value field Alternative A and the PSE allocated power value field Alternative A shall contain the PSE's allocated power value for Alternative A and Alternative B respectively, defined in Table 79–6b. For Type 3 and Type 4, the PSE allocated power value field defined in Table 79.3.2.5 is the sum of the PSE allocated power values defined in Table 79–6b.~~

~~The value for the Alternative A field should be (PSE allocated power value – PSE allocated power value Alternative B). The value for the Alternative B field should be (PSE allocated power value – PSE allocated power value Alternative A).~~

"PSE allocated power value Alternative A" and "PSE allocated power value Alternative B" are the maxi-mum input average power levels (see 145.3.8.2) the PSE expects the PD to draw on the respective Alterna- tives. "PSE allocated power value Alternative A" and "PSE allocated power value Alternative B" are the power levels at the input to the PD's PI. The PSE uses this value to compute $P_{Class\text{-}2P}$ defined in 145.2.7.

Table 79–6b—PSE allocated power value field for Alternative A and Alternative B

Bit	Function	Value/meaning
15:0	PSE allocated power value Alternative A	Power expressed in units of 0.1 W. Valid values for these bits are decimal 1 through 499.
15:0	PSE allocated power value Alternative B	Power expressed in units of 0.1 W. Valid values for these bits are decimal 1 through 499.

79.3.2.6c Power status

-Make the following changes.
-To renumber the subclause numbers and the related Table numbers per the YELLOW marke and make the correct links.
-Replace Table 79-6a with Table 79-6X1 in the following sections and Tables:

Table 79–6a—Power status field
79.3.2.6c Power status

The power status field shall contain the PSE's bit-map of the PSE power pair and PSE or PD power class, defined in ~~Table 79–6a~~ **Table 79-6X1**, and is reported for the device generating the TLV.

79.3.2.6c.1 PSE power pairsx
The PSE power pairsx field shall contain an integer value for PSE power pairs defined by 145.2.4. A TLV generated by a PD shall set the field to 00.

79.3.2.6c.2 Power Classx Mode A
When the power ~~type~~ typex is PD this field shall be set to the requested Class of the dual-signature PD for Mode A during Physical Layer Classification as defined in 145.3.6. When the power type is PSE this field shall be set to the PSEs assigned Class for Alternative A as defined in 145.2.7. PSEs connected to a single-signature PD and single-signature PDs set this field to value 0.

79.3.2.6c.3 Power Classx Mode B
When the power ~~type~~ typex is PD this field shall be set to the requested Class of the dual-signature PD for Mode B during Physical Layer Classification as defined in 145.3.6. When the power type is PSE this field shall be set to the PSEs assigned Class for Alternative B as defined in 145.2.7. PSEs connected to a single-signature PD and single-signature PDs set this field to value 0.

79.3.2.6c.4 Power Classx
When the power ~~type~~ typex is a single-signature PD or Type 1 and Type 2 PD, this field shall be set to the requested Class of the PD during Physical Layer Classification as defined in 145.3.6. When the power type is PSE this field shall be set to the PSEs assigned Class as defined in 145.2.7. PSEs connected to a dual-signature PD and dual-signature PDs set this field to ~~value 15~~value 0.

79.3.2.6d System setup
The System setup field shall contain the device bit-map of the Power ~~type~~typex, PD 4PID, and PD Load defined in **Table 79-6X2** ~~Table 79–6b~~ and is reported for the device generating the TLV. The value of the System setup field transmitted by a PSE is undefined.

79.3.2.6d.1 Power typex
This field shall be set according to **Table 79-6X2** ~~Table 79–6b~~.

Replace Table 79-6b with Table 79-6X2 in the following sections and Tables and make the correct links:

79.3.2.6d.2 PD 4PID
79.3.2.6d.3 PD Load
Table 79–6b—System setup field

Table 79-6X1 ~~Table 79–6a~~—Power status field

Bit	Function	Value/meaning
15:13	Reserved	Transmit as zero. Ignore on receive.
12:11	PSE power pairsx	6 5 1 1 = Both Alternatives 1 0 = Alternative B 0 1 = Alternative A 0 0 = Reserved/Ignore
10	Reserved	Transmit as zero. Ignore on receive.
9:7	Power Classx Mode A	9 8 7 1 1 1 = Reserved/Ignore 1 1 0 = Reserved/Ignore 1 0 1 = Class 5 1 0 0 = Class 4 0 1 1 = Class 3 0 1 0 = Class 2 0 0 1 = Class 1 0 0 0 = Single-signature PD
6:4	Power Classx Mode B	6 5 4 1 1 1 = Reserved/Ignore 1 1 0 = Reserved/Ignore 1 0 1 = Class 5 1 0 0 = Class 4 0 1 1 = Class 3 0 1 0 = Class 2 0 0 1 = Class 1 0 0 0 = Single-signature PD
3:0	Power Classx	3 2 1 0 1 1 1 1 = Dual-signature PD 1 1 1 0 = Reserved/Ignore 1 1 0 1 = Reserved/Ignore 1 1 0 0 = Reserved/Ignore 1 0 1 1 = Reserved/Ignore 1 0 1 0 = Reserved/Ignore 1 0 0 1 = Reserved/Ignore 1 0 0 0 = Class 8 0 1 1 1 = Class 7 0 1 1 0 = Class 6 0 1 0 1 = Class 5 0 1 0 0 = Class 4 0 0 1 1 = Class 3 0 0 1 0 = Class 2 0 0 0 1 = Class 1 0 0 0 0 = Class 0

Table 79-6X2 ~~Table 79–6b~~—System setup field

Table 79–6b—System setup field

Bit	Function	Value/meaning
7:4	Power typex	7 6 5 4 1 1 1 1 = Type 4 dual-signature PD 1 1 1 0 = Reserved/Ignore 1 1 0 1 = Type 3 dual-signature PD 1 1 0 0 = Reserved/Ignore 1 0 1 1 = Reserved/Ignore 1 0 1 0 = Reserved/Ignore 1 0 0 1 = Type 4 single-signature PD 1 0 0 0 = Type 4 PSE 0 1 1 1 = Type 3 single-signature PD 0 1 1 0 = Type 3 PSE 0 1 0 1 = Type 2 PD 0 1 0 0 = Type 2 PSE 0 0 1 1 = Type 1 PD 0 0 1 0 = Type 1 PSE 0 0 0 1 = Reserved/Ignore 0 0 0 0 = Reserved/Ignore
3	PD 4PID	1 = PD supports powering of both Modes 0 = PD does not support powering of both Modes
2	Reserved	Transmit as zero. Ignore on receive.
1	PD Load	1 = PD is dual-signature and power demand on Mode A and Mode B are electrically isolated. 0 = PD is single-signature or dual-signature and power demand on Mode A and Mode B are not electrically isolated.
0	Reserved	Transmit as zero. Ignore on receive.

END OF BASE LINE