P802.3bt D3.0 – Clearing ‘shalls’ from 145.1 v100

145.1.1 Compatibility considerations

~~All implementations of PD and PSE systems shall be compatible at their respective Power Interfaces (PIs) when used in accordance with the restrictions of Clause 145 where appropriate.~~ The requirements in this Clause are designed such that PSEs and PDs that meet these requirements are compatible at their respective Power Interfaces (PIs). Designers are free to implement circuitry within the PD and PSE in an application-dependent manner provided that the respective PI specifications are satisfied.

Elevate subclause 145.1.3.1 to 145.1.4.

~~145.1.3.1~~ 145.1.4 Cabling requirements

Type 3 and Type 4 operation requires Class D, or better, cabling as specified in ISO/IEC 11801:1995 with the additional requirement that the channel DC loop resistance ~~shall be~~ is 25 Ω or less. These requirements are also met by Class D or better cabling as specified by ISO/IEC 11801:2002, Category 5e or better cable and components as specified in ANSI/TIA-568-C.2, or Category 5 cable and components as specified in ANSI/TIA/EIA-568-A-1995.

Move the content of 145.1.3.2 into 145.1.4 (append at the end) and change as follows:

145.1.3.2 Link section requirements

Within Clause 145 and its annexes, the term link section refers to the point-to-point medium connection between two and only two active Power Interfaces (PIs).

Type 3 and Type 4 operation requires link sections to ~~Link sections for all Types shall~~ comply with the intra-pair resistance unbalance requirements for twisted- pair cabling as specified in ISO/IEC 11801:2002 and ANSI/TIA-568-C.2. Refer to Annex 145A for more information including the requirements for pair-to-pair resistance unbalance when operating over 4 pairs.