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# Technical Feasibility – PHYs beyond 10G

IEEE 802.3 Greater than 10 Gbps Automotive Electrical  
Ethernet Study Group

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# Technical Feasibility vs. Baseline Proposals

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- Study Group does Technical Feasibility
  - Theory, analysis, simulations showing reasons to believe we CAN get to a solution
  - Often done with Shannon Capacity, Measurements, and Architecture discussions
- Task Force does Baseline Proposals
  - Specific proposals for modulation, coding, bandwidths, IL
  - NOT until we get to Task Force
- **THE FOLLOWING IS FOR TECHNICAL FEASIBILITY AND NOT A PROPOSAL**

# Capacity

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- Shannon capacity arguments are often used for technical feasibility
- Shannon capacity arguments are **HIGHLY SENSITIVE** to assumptions
  - How much signal can be transmitted over how much bandwidth
  - What additive impairments can be cancelled
  - What is the “noise” which is left over?
  - How do we treat implementation limits
- Nonstationary noise (e.g., EMI) isn't treated by Shannon-Hartley law (AWGN) theory

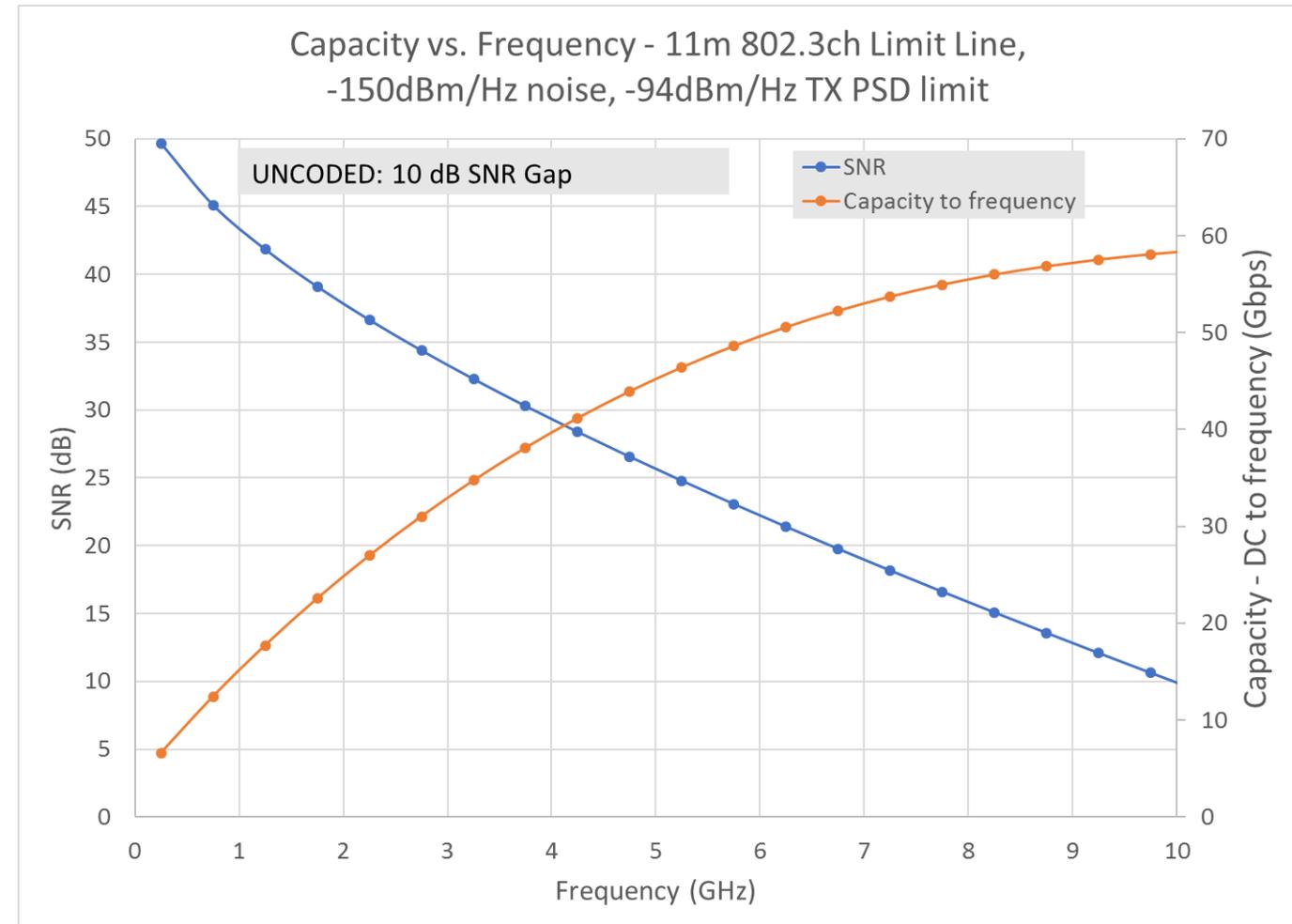
# What are the noise sources?

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- Fixed levels: (AGN noise sources)
  - Circuit board noise
  - Receiver noise floor (thermal)
- Relative levels (vary with Tx signal level) - Alien Crosstalk
- Environment-dependent: (NOT Shannon-Hartley law)
  - Impulsive EMI
  - Rate of variation of echo & impulse response (minor effect)
- Implementation complexity dependent: (NOT Shannon-law)
  - Residual echo levels
  - Residual ISI levels

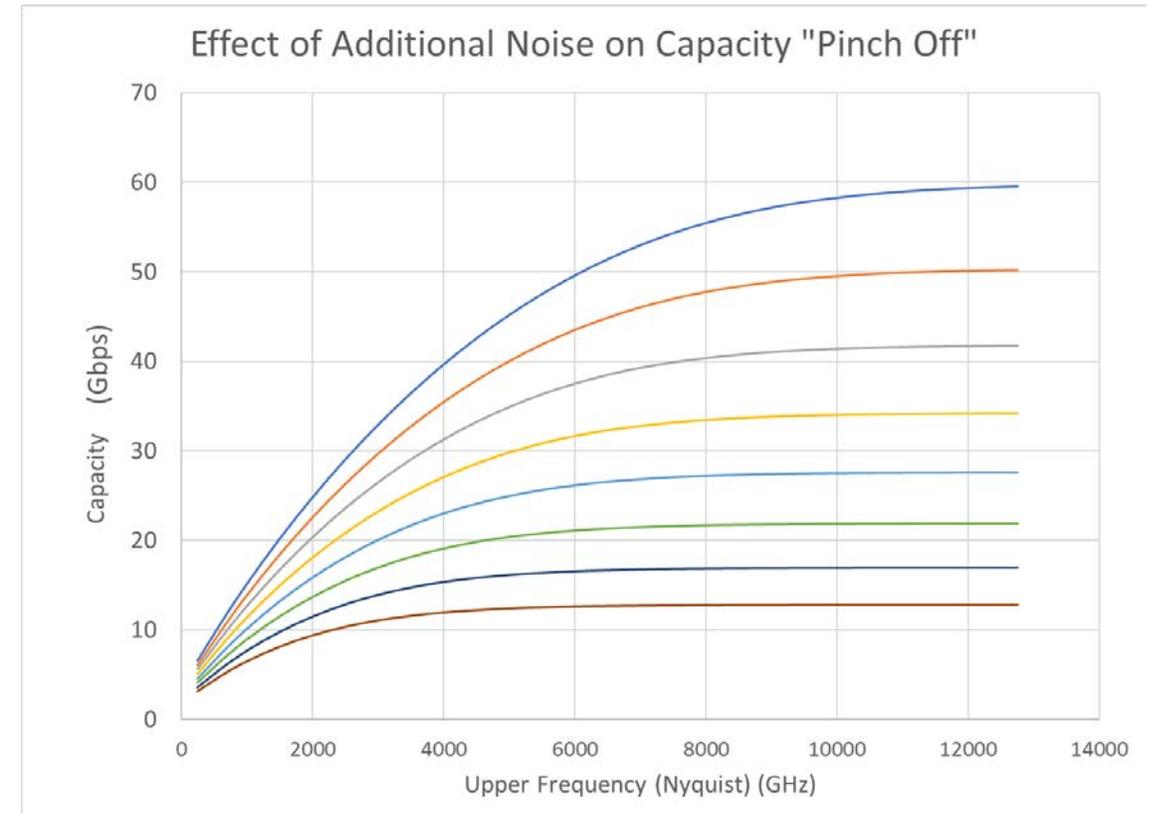
# Plenty of Capacity in 802.3ch model cable at 11m

- 802.3ch IL length-scaled to 11m
- 802.3ch Tx PSD scaled to 25 Gbps, -150 dBm/Hz AWGN board noise model, Uncoded transmission
- Capacity continues to grow with bandwidth until 10 GHz
- Real limits will happen with higher frequency noise
  - Causes “pinch off”



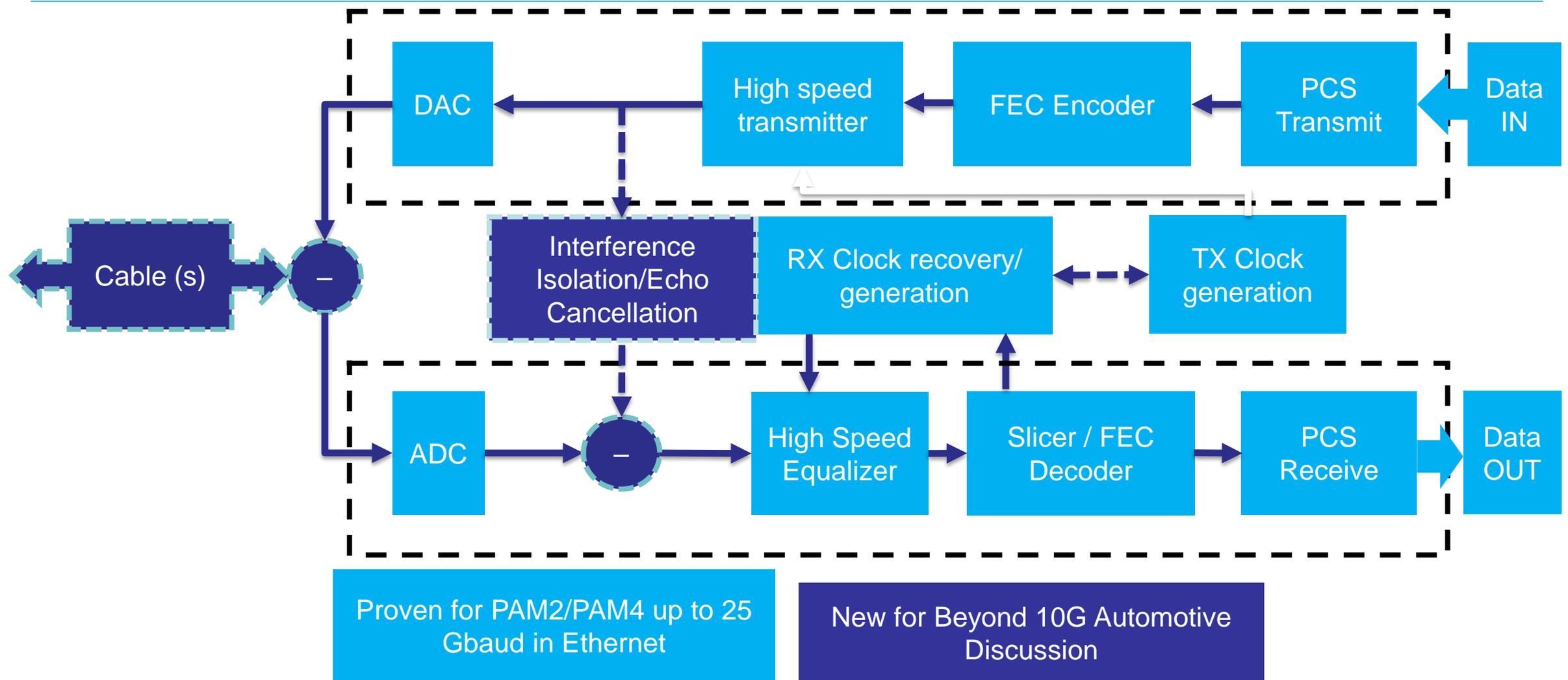
# High-frequency noise causes capacity Pinch Off

- Usable bandwidth:
  - Decreases in the presence of high frequency noise
  - Increases with use of coding gain
- 802.3ch-specified cable still has > 25 Gbps with uncoded transmission and 22 dB margin to capacity
- Bandwidth < 6 GHz
- All feasible for 25 Gbps



<b>Margin to capacity (dB)</b>	10	13	16	19	22	25	28	31
<b>90% capacity Freq. (GHz)</b>	6.5	6	5.5	5	4.5	4	3.5	3
<b>Capacity (Gbps)</b>	60	50	42	34	28	22	17	13

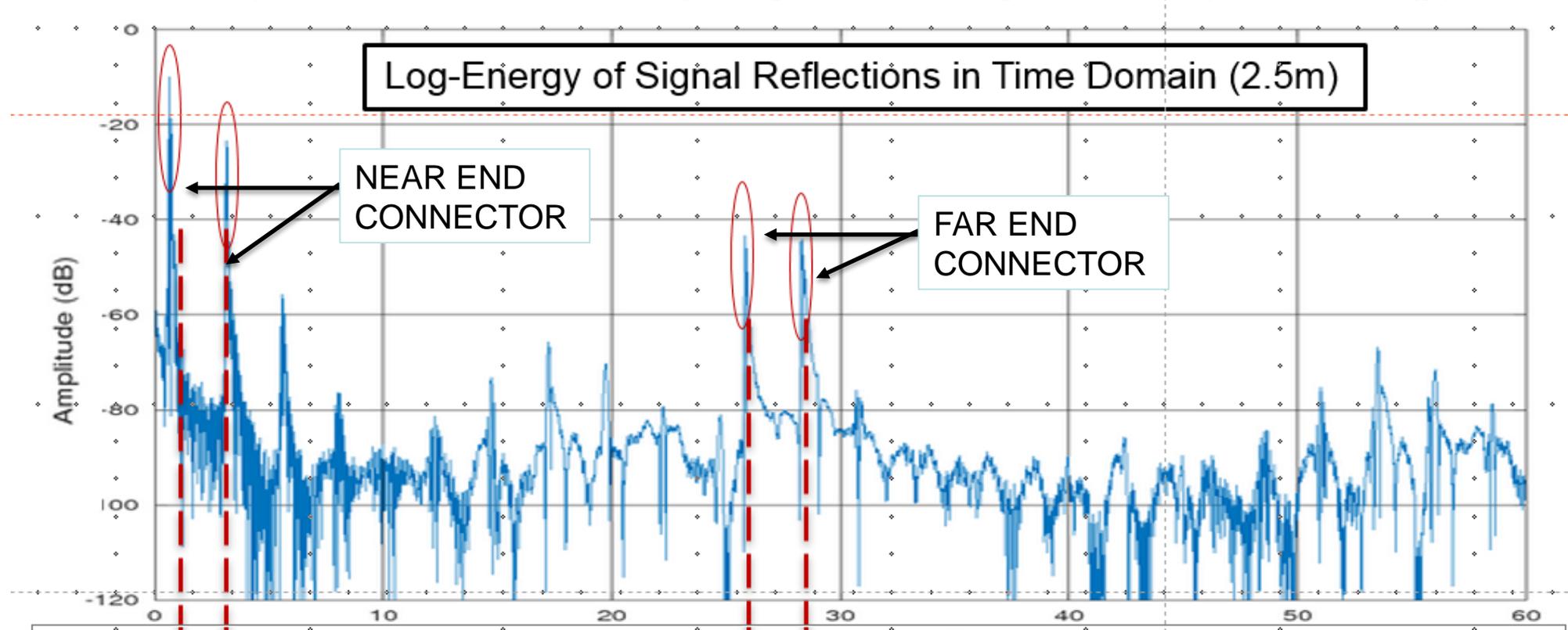
# High Speed PHY block diagram – Proven parts



# Feasibility Focus – Echo Cancellation at high speeds

- Echo from discontinuities (connectors/segments/bends) dominates over micro-reflections from cable roughness

Note – Echo response becomes lower frequency as time delay increases (NOT causing pinch off)



# Restrictions

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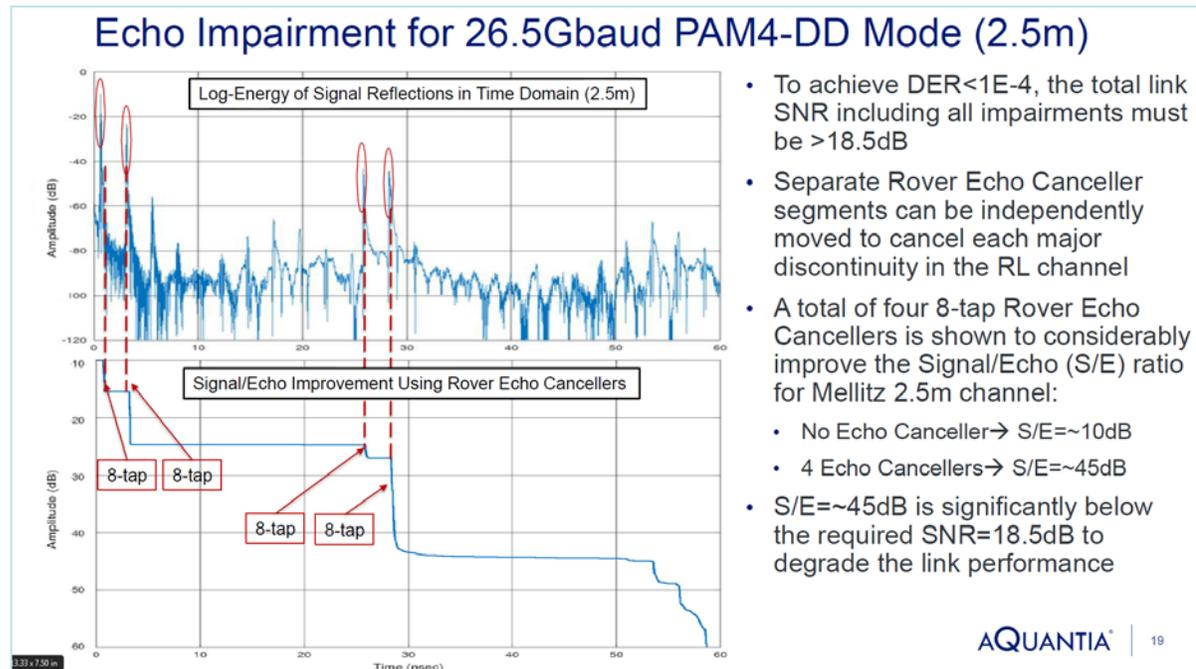
- Need to limit the number of connectors & bends
- Need to specify micro-reflection (TDR) levels
- Unlikely to extend much beyond PAM-4 SNR levels
  - Simulations/demonstrations show micro-reflections limit signal to echo ratio limiting the PAM levels

# Roving taps & Sparse Echo Cancellation

- Time domain structure of return loss is important
- Leads to significant power & feasibility trades

[http://www.ieee802.org/3/ck/public/18\\_09/farjadrad\\_3ck\\_01b\\_0918.pdf](http://www.ieee802.org/3/ck/public/18_09/farjadrad_3ck_01b_0918.pdf)

[http://www.ieee802.org/3/bq/public/jan14/langner\\_3bq\\_01\\_0114.pdf](http://www.ieee802.org/3/bq/public/jan14/langner_3bq_01_0114.pdf)



## Restricted Echo Cancellation

- Opportunity for improvement:
  - “Restricted” or “Sparse” Echo
  - Cancel echoes only from a subset of taps
- Moving to “restricted” echo cancellation could potentially cut echo-canceller power by 75%
  - Assumption is that since we are in a two connector datacenter model, we may be able to utilize the fact that there are limited points of reflection to simplify the equalization
  - Still requires fast response to areas of bending on cable
- This would give a 40GBASE-T filter power increase of 1.44x

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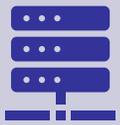
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## 802.3 has pushed the speed/implementation limits before

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- High speed ethernet is usually on the ‘bleeding edge’
  - Usually ‘optical’ projects, but all have electrical interfaces
    - Examples: 802.3ae (10G), 802.3ba (40G/100G), 802.3cd (50G/100G)
  - Various levels of parallelism are visited over the life of the standard (e.g., 10-lane -> 4-lane -> single lane solutions)
- Methodology is to prove out technical feasibility with a high level of parallelism, but the market evolves with much less parallelism.
- We can borrow from best practices
  - 802.3ba created an architecture to do this, later standards built on and refined it

# Well-trodden Technical Feasibility Path for Optical Ethernet



Optical Ethernet often starts with architecture rather than PHY



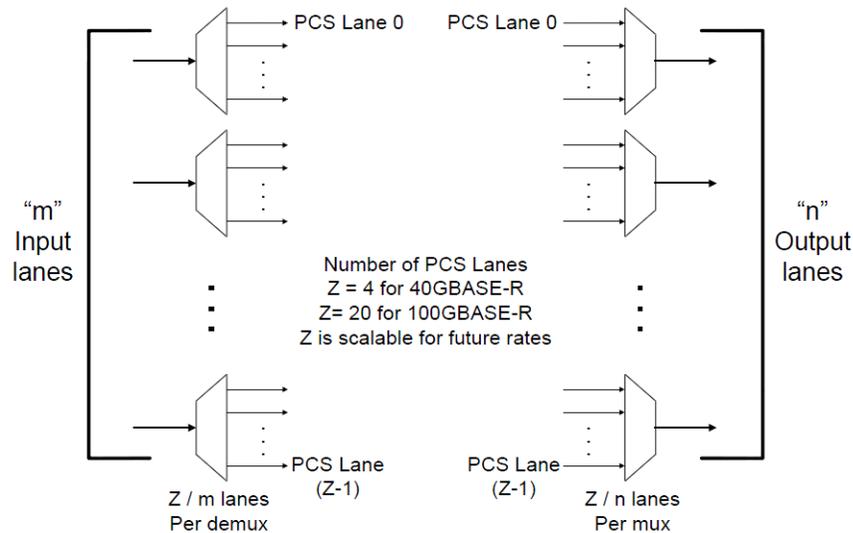
Define PHYs to match applications



Parallelize as needed for technological maturity

[http://www.ieee802.org/3/time\\_adhoc/public/apr09/dambrosia\\_03\\_0509.pdf](http://www.ieee802.org/3/time_adhoc/public/apr09/dambrosia_03_0509.pdf)

## PMA Demux / Mux Functionality



- Enables changing of lane number and rate per lane for multiple physical layer specifications
- For example 100GbE:
  - 10 x 10 Gb/s
  - 5 x 20 Gb/s
  - 4 x 25 Gb/s
  - 2 x 50 Gb/s
  - 1 x 100 Gb/s

Shows PMA demux / mux functionality in one direction only

# 802.3cd 50 Gbps Ethernet builds further

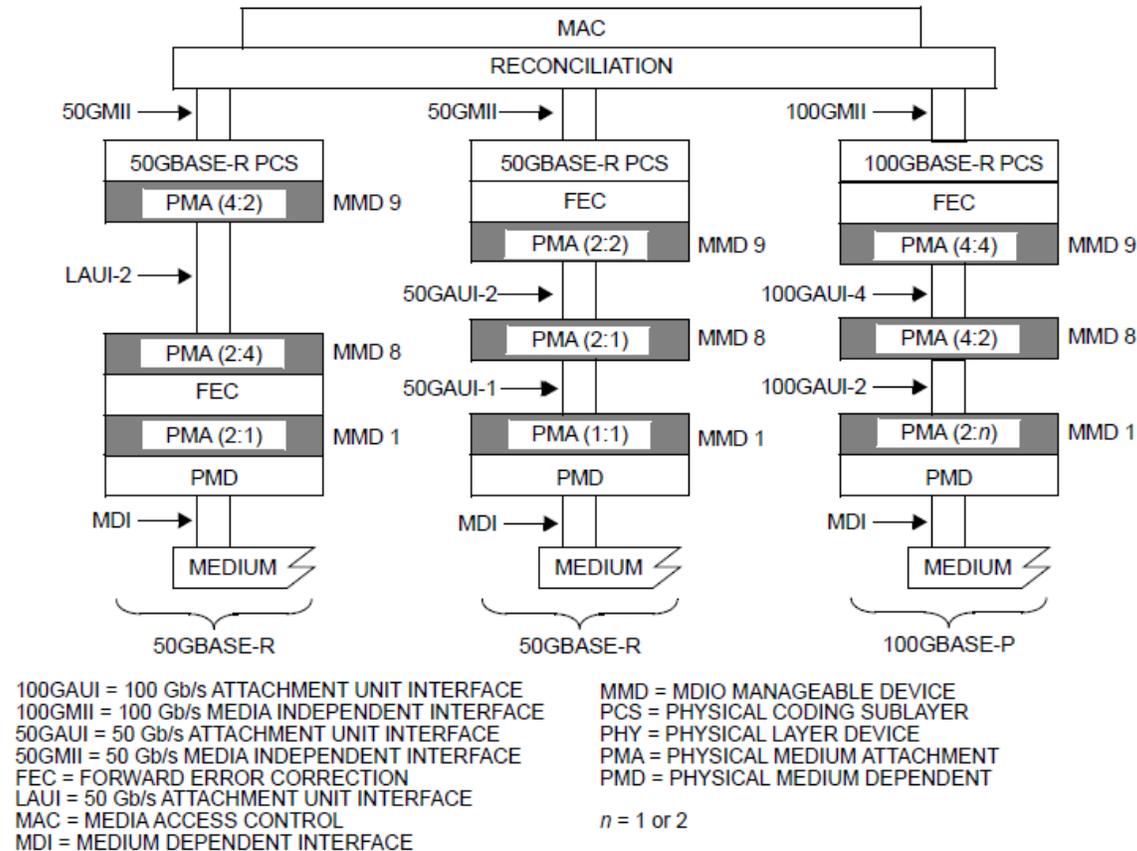


Figure 135-2—Example 50GBASE-R and 100GBASE-P PMA layering

Source: IEEE Std 802.3cd-2018

# 802.3ca provides a mechanism for bonding PHY lanes

- Clause 143 bonds multiple physical layers in to a higher rate lane
- Provides a framework for extensibility to higher rates with the best PHYs available at the time given technology
- Assures a path to technical feasibility

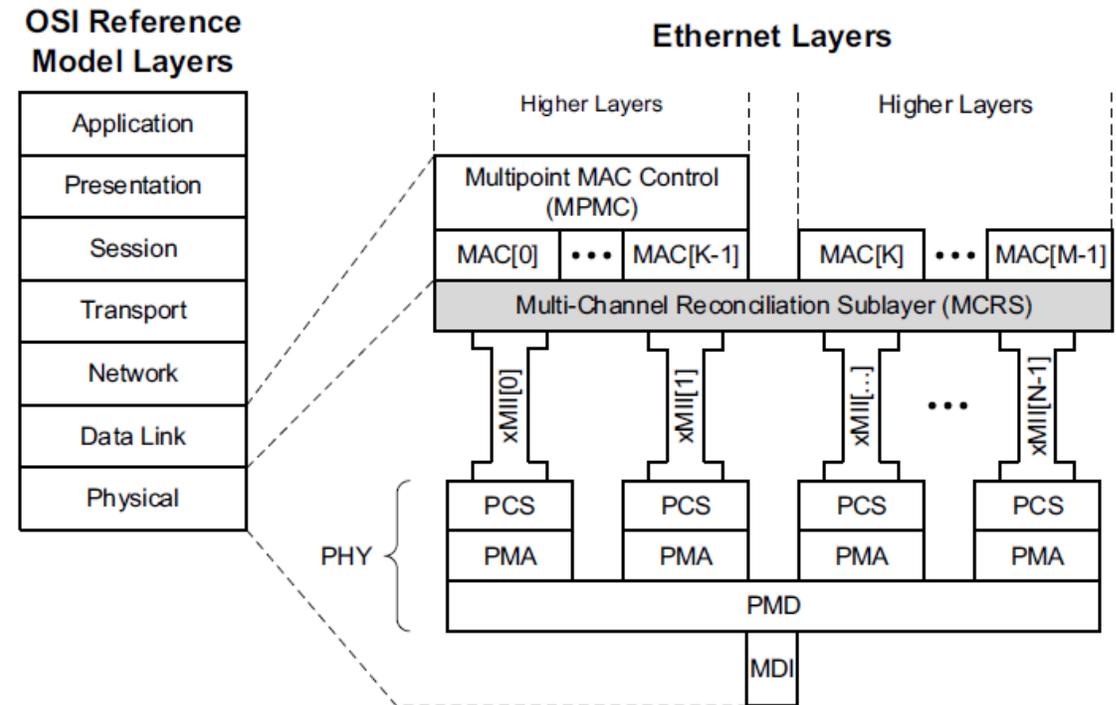


Figure 143-1—Relationship of MCRS to the OSI Reference Model

Source: IEEE P802.3ca D2.2

# Possible extensions to 50 Gbps on 2 cables

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## 2x25 GBd PAM-4 Single-duplex

- Reuse of 50 Gbps optical serdes
- 2X signaling rate in PHY vs dual-duplex
  - 2X speed DFE ~ 4X length
  - 2X speed FFE ~ 4X length
- Channel loss budget at 12.5 GHz
  - Connectors/Cabling specified, no suckouts to 12.5 GHz
- Balance of complexity shifts toward cabling, connectors, & boards circuits/cost balance
- Lower expectations from system
  - Shorter trace lengths, overall less margin

## 2x12.5 GBd PAM-4 Dual-duplex

- Reuse of single lane silicon from 25G
- Echo canceller
  - PAM-4 -> multiply-free structure
  - Sparse structure at higher speeds
- Robust, known system expectations
  - Shared risk with 25GBASE-T1
- Loss budgeted at 6.25 GHz
  - Existing cabling & components
- Better balance of complexity

# Summary

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- REMINDER: THESE ARE NOT BASELINE PROPOSALS
- Technical feasibility for 25 Gbps echo cancelled transmission based on extensions of 802.3ch technology
  - Natural extension of echo cancellation speed
  - Natural extension of cable bandwidth within limits already shown
- Technical feasibility path for 50 Gbps (and 100 Gbps) based on (at least) proven path for parallelization used in 802.3 high speed technologies
  - Fallback for 25 Gbps is parallelization of slight rate increase to 802.3ch technology

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# THANK YOU!

Consensus  
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