PMA lane versus PCS frame FEC and the resulting impact on guaranteeing performance at transceiver module / host PCB interface

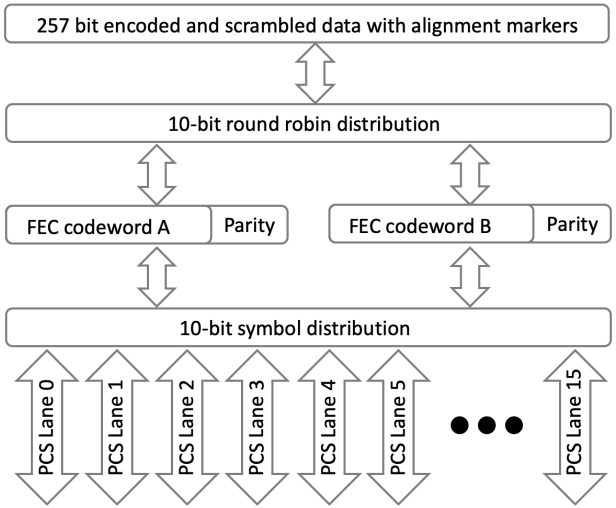
Jim Theodoras

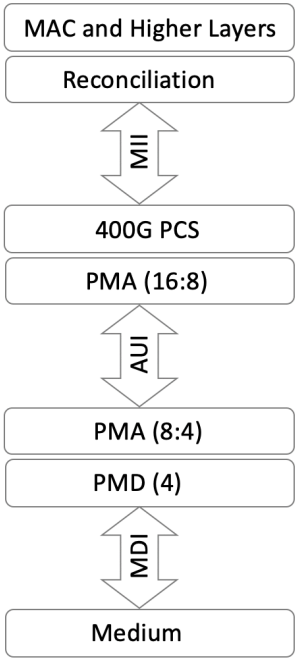
Employed by and affiliated with HG Genuine

400GAUI-8 FEC

HGGenuine

- FEC is at PCS layer, striped across lanes
- FEC uses Round Robin distribution across PCS lanes
- FEC uses lane markers, hence can begin and stop anywhere





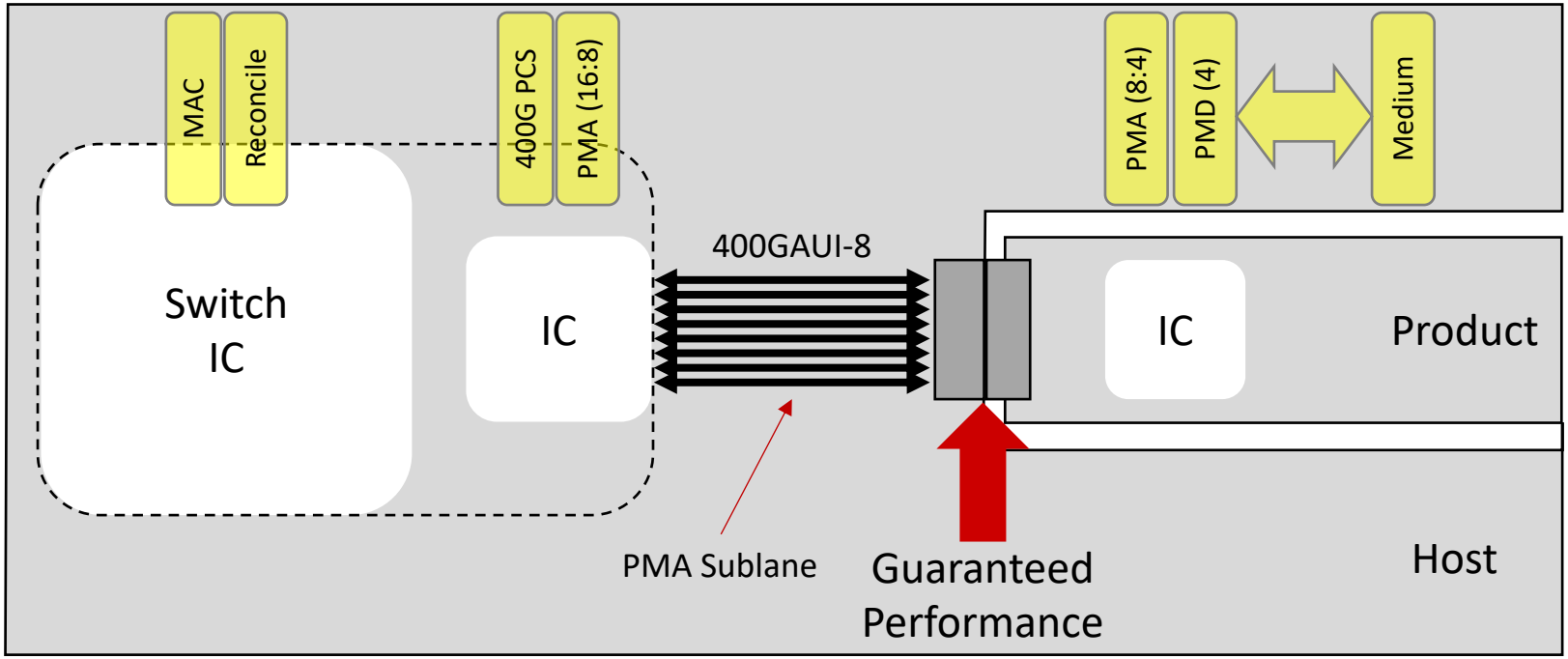
For a great tutorial, please see:

Mark Gustlin, “A Deep Dive into the 802.3bs 200GBASE-R and 400GBASE-R PCS/PMA”, in Ethernet Alliance Blog, Mar 28, 2018.

Product / Host Interface

HGGenuine

- The physical boundary could be anywhere in stack
- Let's consider QSFP-DD as product and switch as host



Monitoring Performance

HGGenuine

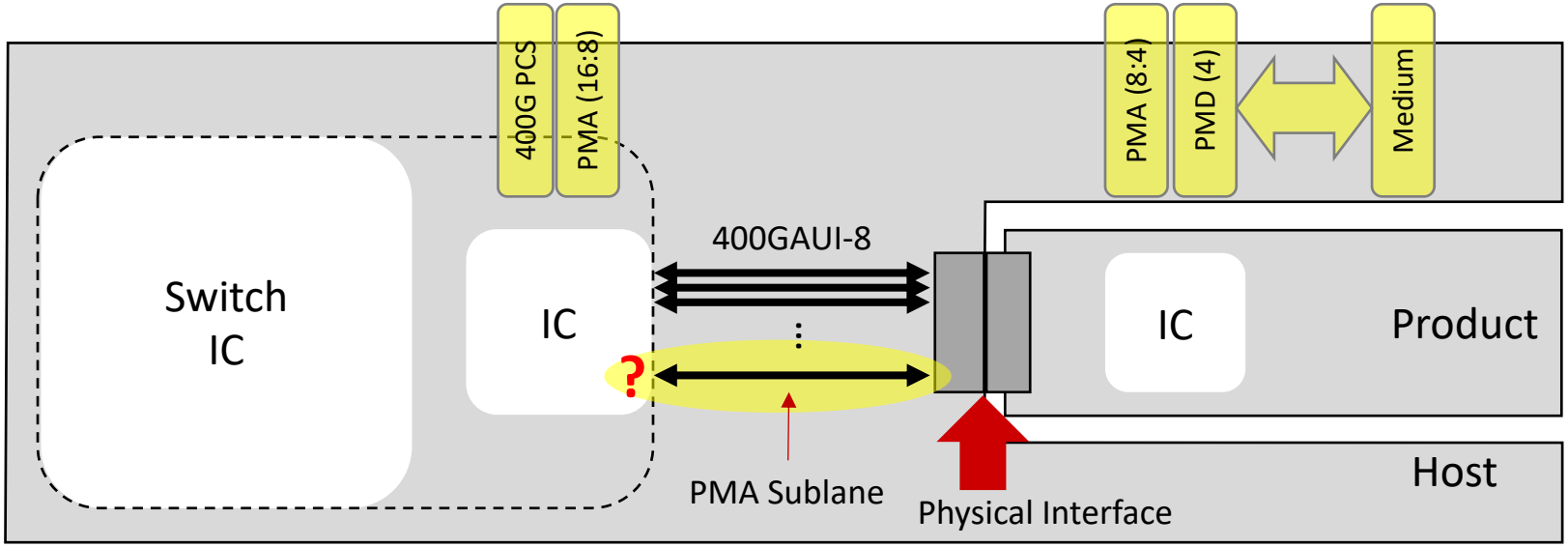
- What tools do I have available at end user level (IOS, JunOS, EOS)?

>PCS Framed up: OK
>PCS Error Blocks: 0
>PCS BER: 1E-12
>
>FEC number of corrected codewords: [big number]
>FEC number of uncorrected codewords: 0 [hopefully]
>FEC lane corrected symbols
>Lane 0 [number]
⋮
>Lane 15 [number]
>Number of PMA lanes: 8 [for this example]
>FEC lane mapping
>FEC lane: 00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15
>PMA lane: 01 01 00 00 03 03 02 02 05 05 04 04 07 07 06 06

Performance at Physical Interface

HGGenuine

- My customers are asking me for performance metrics per each individual PMA sublane
- My customers do not consider the PCS metrics close enough to PMA lane
- Ideally, it would be preferable to have pre and post FEC BER for each PMA sublane, as each is an individually equalized high speed transmission line.



Proposal

HGGenuine

Wherever a potential physical boundary between a product and host exists, there should be a well-defined way of quantifying performance on a per lane basis.