Technical feasibility of 200G per lane CR/KR electrical links

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Background

- The comprehensive analysis on PAM signaling schemes indicates that 200G per lane electrical interfaces are feasible, including the AUIs of C2M and C2C as well as the PHYs of CR and KR. (lu_b400g_01_210322)
- Objectives and criteria for 200G/lane electrical interfaces should be set properly to facilitate technical discussions. (lu_b400g_01_210517)
  - Objectives for 200G/lane electrical interfaces
    - N*200G/lane based AUIs (C2M and C2C, adopted)
    - N*200G/lane based PHYs (CR and KR, under discussion)
  - Requirements and Criteria for 200G/lane electrical.
    - **Commonality**: Common signaling with application-specific performance.
    - **Compatibility**: Support interoperability with legacy 100G/lane link transceiver.
    - **Competitiveness**: Lower power ("pJ/bit") and lower cost ("cost/bit").

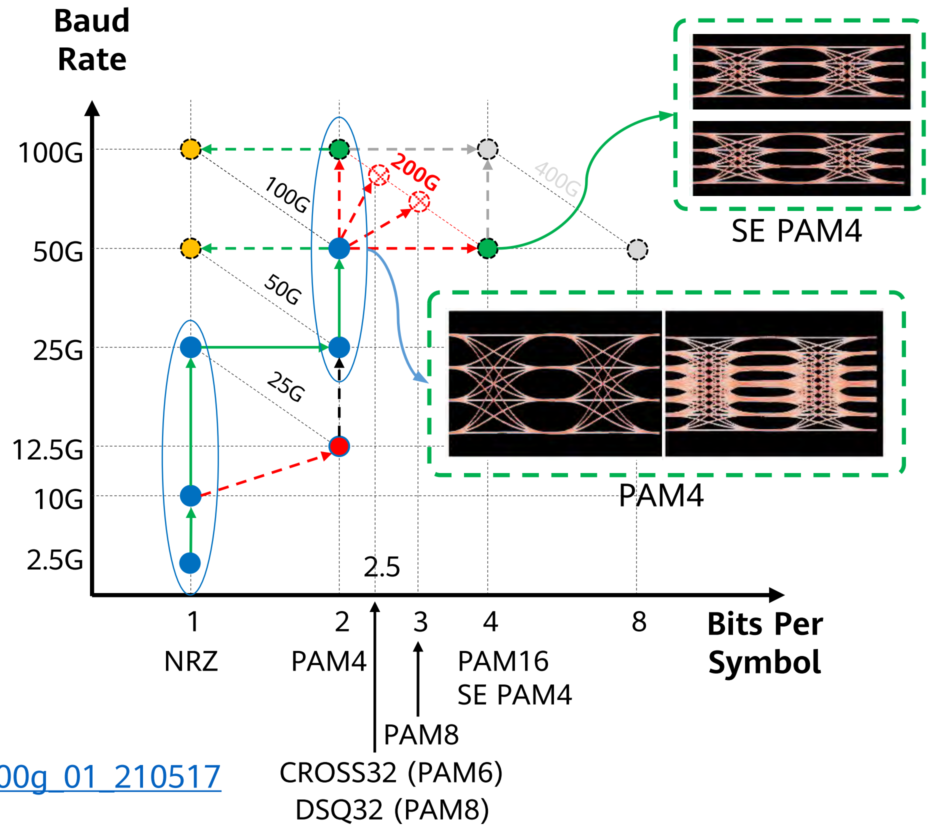
"3 **Com** Criteria"

Candidates for 200G per lane signaling

Commonality
Common signaling with application-specific performance.

Compatibility
Interoperability with legacy 100G/lane link transceiver.

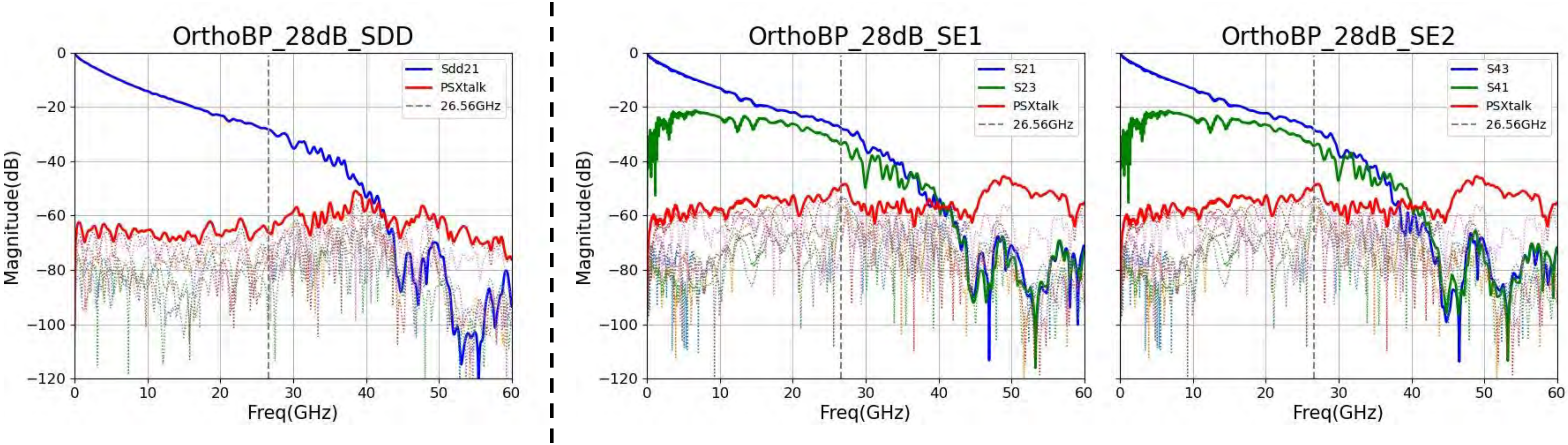
Competitiveness
Lower power ("pJ/bit") and lower cost ("cost/bit").



lu_b400g_01_210517

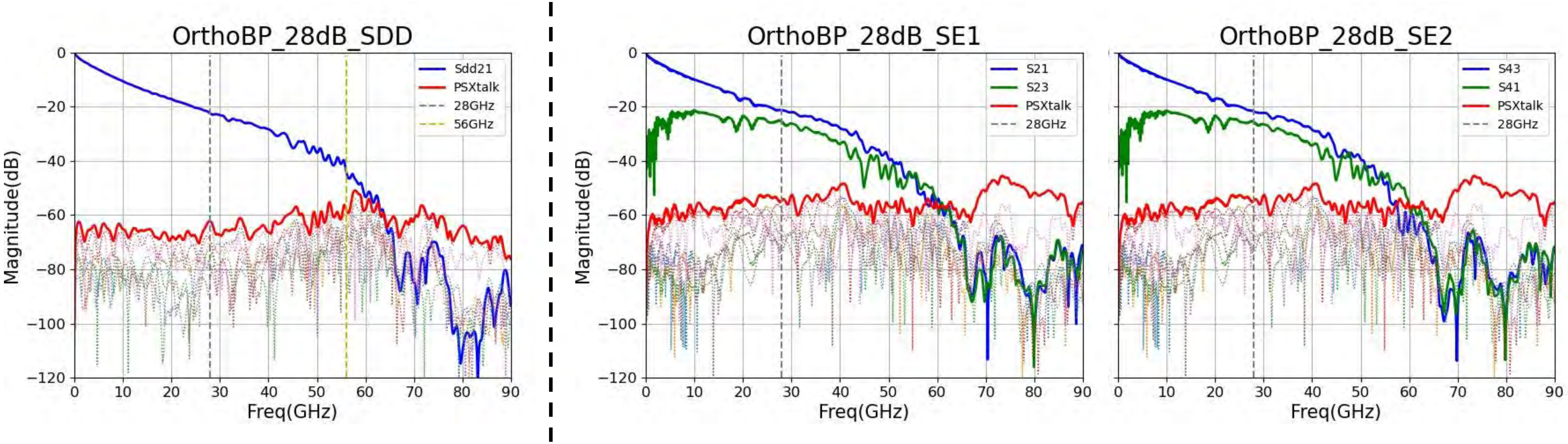
- **CR and KR dominate the feasibility of electrical links** in order to meet the criteria of "commonality", "compatibility" and "competitiveness".
- **C2M and C2C AUIs are usually covered by CR and KR transceivers** in large ASIC and on-board CDR.
  - Module CDR may use a dedicated C2M transceiver. it may also be implement by dynamically limiting the equalization capabilities of CR&KR transceiver.
- Three aspects should be considered in sequence
  - **Channel and signaling**
  - Advanced DSP algorithm
  - Stronger FEC
- With IEEE 802.3ck 112G PAM4 channels, PAM4 and SE PAM4 are investigated to explore the feasibility of 200G per lane electrical links.

Channel description (IEEE 802.3ck channel)



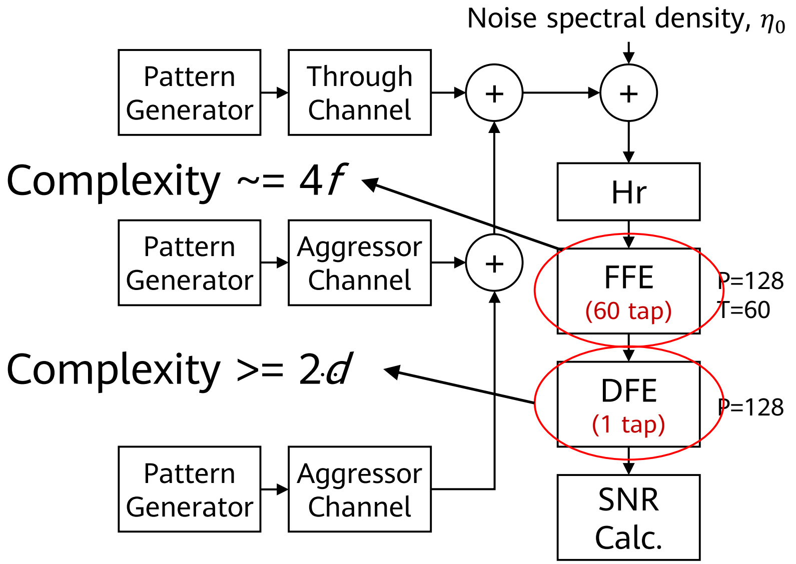
- IEEE 802.3ck orthogonal backplane channels are considered, only 28dB channel is shown.
  - ~24dB @ 26.56GHz, 20 inch orthogonal backplane (Low).
  - ~28dB @ 26.56GHz, 24 inch orthogonal backplane (Medium).
  - ~32dB @ 26.56GHz, 28 inch orthogonal backplane (High).
  - From tracy_3ck_01b_0119 .
- The package is not considered, i.e. the loss is “bump-to-bump”.

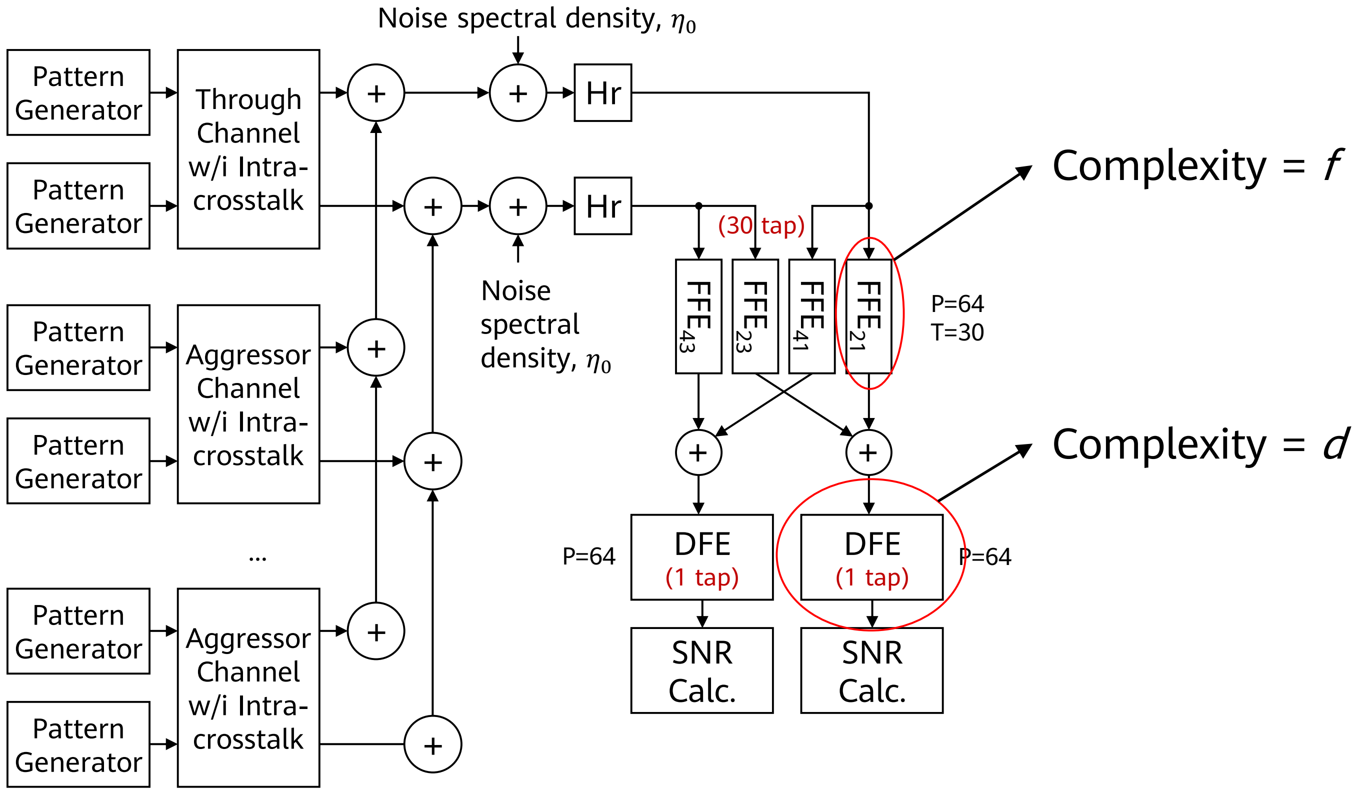
Channel description (Bandwidth scaled up by 1.5x)



- IEEE 802.3ck orthogonal backplane channels are considered, only 28dB channel (before scaling) is shown.
  - ~18dB @ 26.56GHz, ~35dB @ 53GHz, ~19dB @ 28GHz, ~39dB @ 56GHz (Low).
  - ~21dB @ 26.56GHz, ~41dB @ 53GHz, ~23dB @ 28GHz, ~44dB @ 56GHz (Medium).
  - ~24dB @ 26.56GHz, ~46dB @ 53GHz, ~26dB @ 28GHz, ~49dB @ 56GHz (High).
  - Scaled from tracy_3ck_01b_0119 .
- The package is not considered, i.e. the loss is “bump-to-bump”.

System model for PAM signaling investigation





- T-tap, P-parallel FFE needs P*T multipliers and P*(T-1) adders
- 1-tap PAM-M unrolled P-parallel DFE, needs M(M-1)*P comparators.

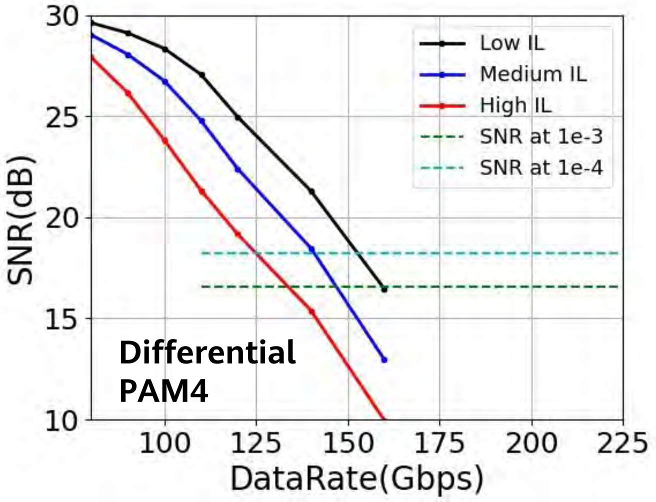
	FFE config.	DFE config.	Complexity of FFE	Complexity of DFE
Differential PAM4	1*2T taps	1 tap	~ $4f$	>= $2d$**
Single-Ended PAM4	4*T taps	1 tap	< $4f$*	$2d$

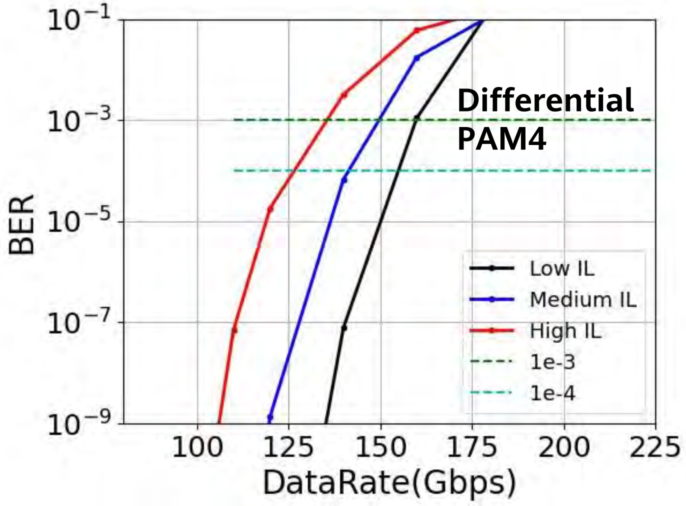
* The cross FFE does not need T taps.
** the mux array is simpler for singled-ended PAM4 DFE.

Complexity is "normalized". Dominant impairments are considered.

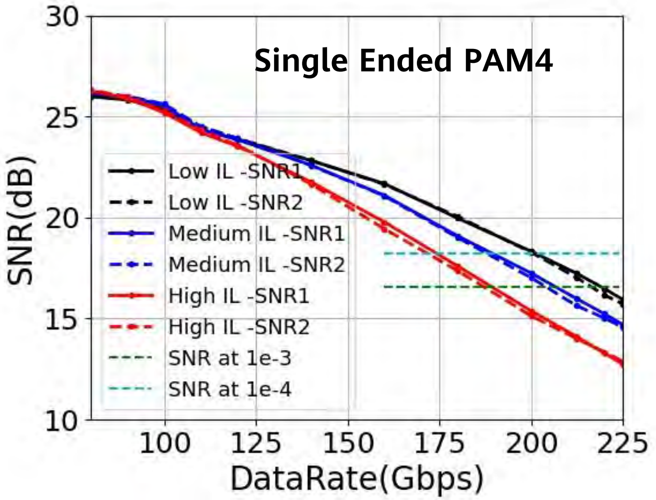
- PAM4: ISI/Loss
- SE PAM4: Crosstalk

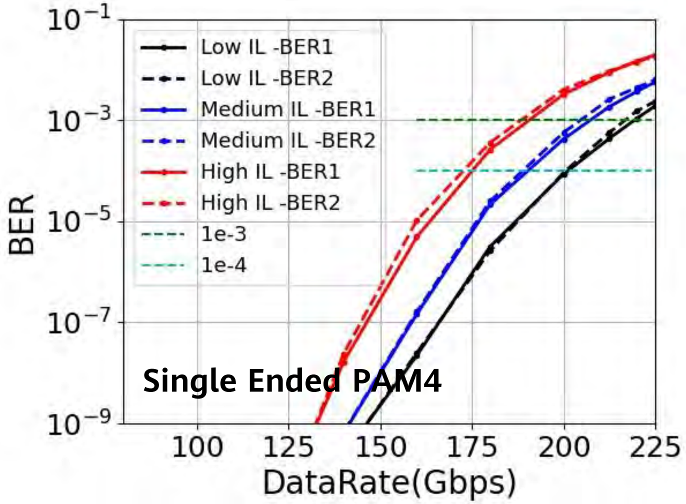
Simulation results (Original channel)





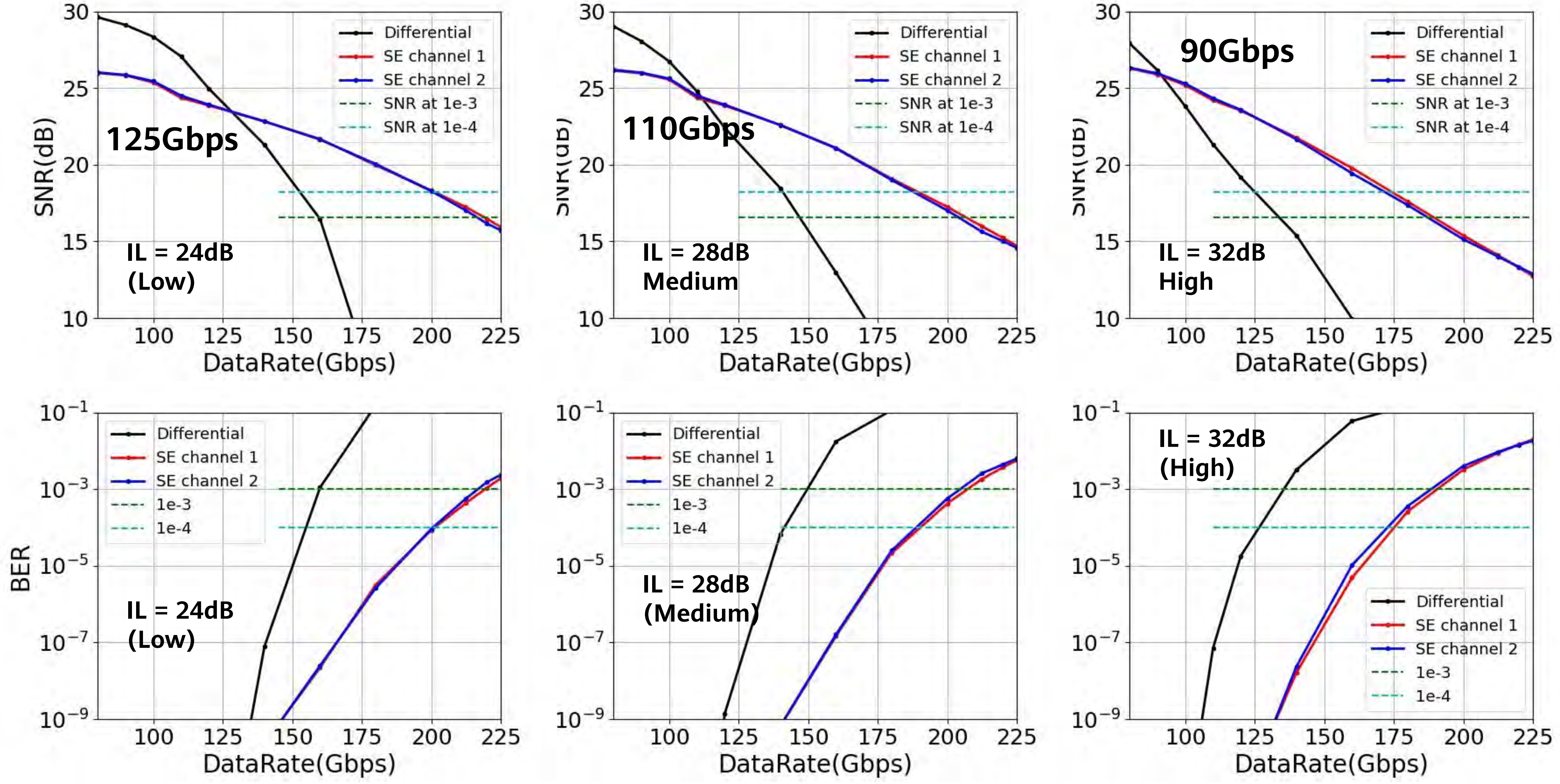
FEC limit = 1e-4 / RS(544, 514)		
Channel IL(dB)	Differential	Single-Ended
24 (Low)	155Gbps	200Gbps
28 (Medium)	140Gbps	190Gbps
32 (High)	125Gbps	170Gbps



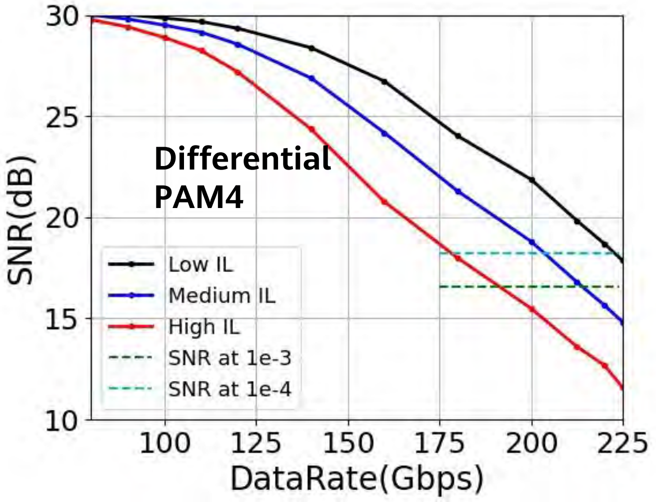


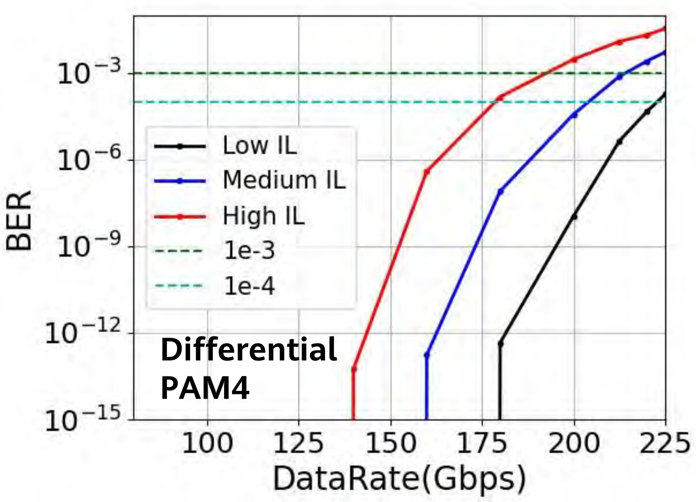
FEC limit = 1e-3 / Stronger FEC		
Channel IL(dB)	Differential	Single-Ended
24 (Low)	160Gbps	220Gbps
28 (Medium)	150Gbps	210Gbps
32 (High)	135Gbps	190Gbps

Simulation results (Original channel)

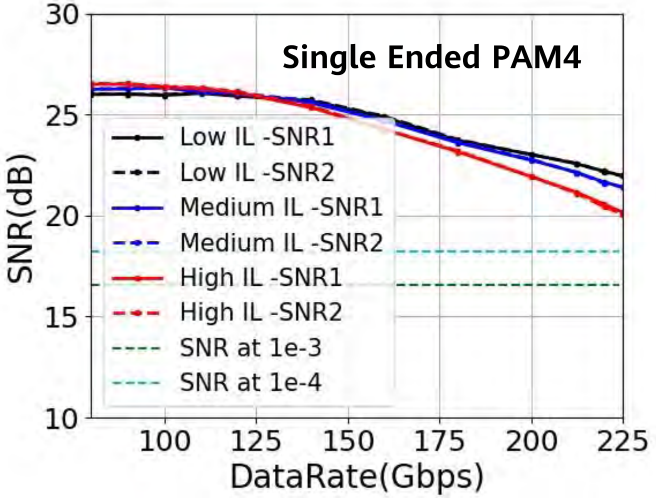


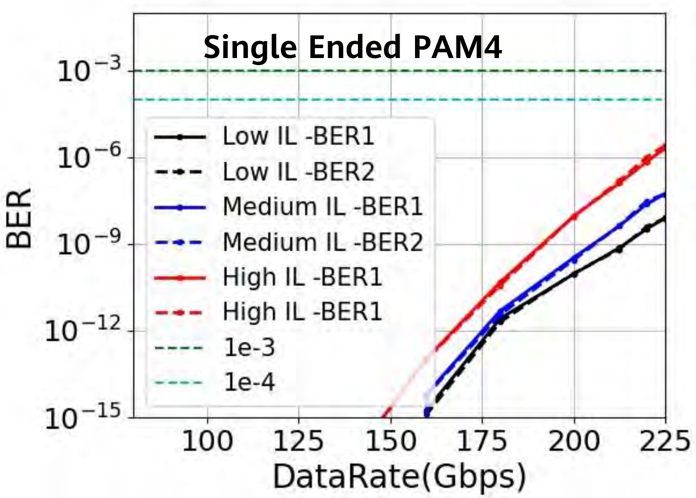
Simulation results (Bandwidth scaled up by 1.5x)





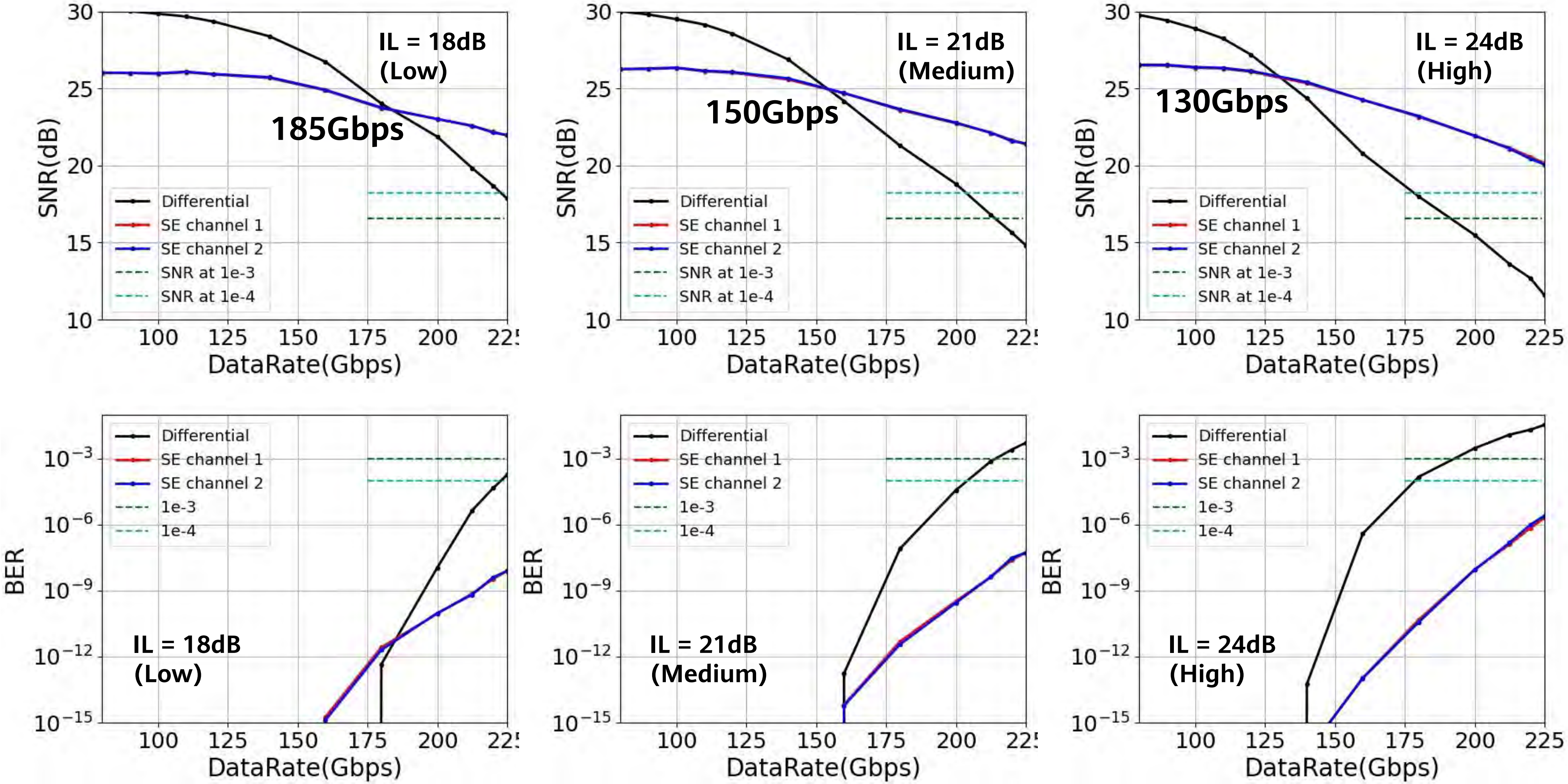
FEC limit = 1e-4 / RS(544, 514)		
Channel IL(dB)	Differential	Single-Ended
18/35 (Low)	220Gbps	>>225Gbps
21/41 (Medium)	205Gbps	>>225Gbps
24/46 (High)	180Gbps	>>225Gbps



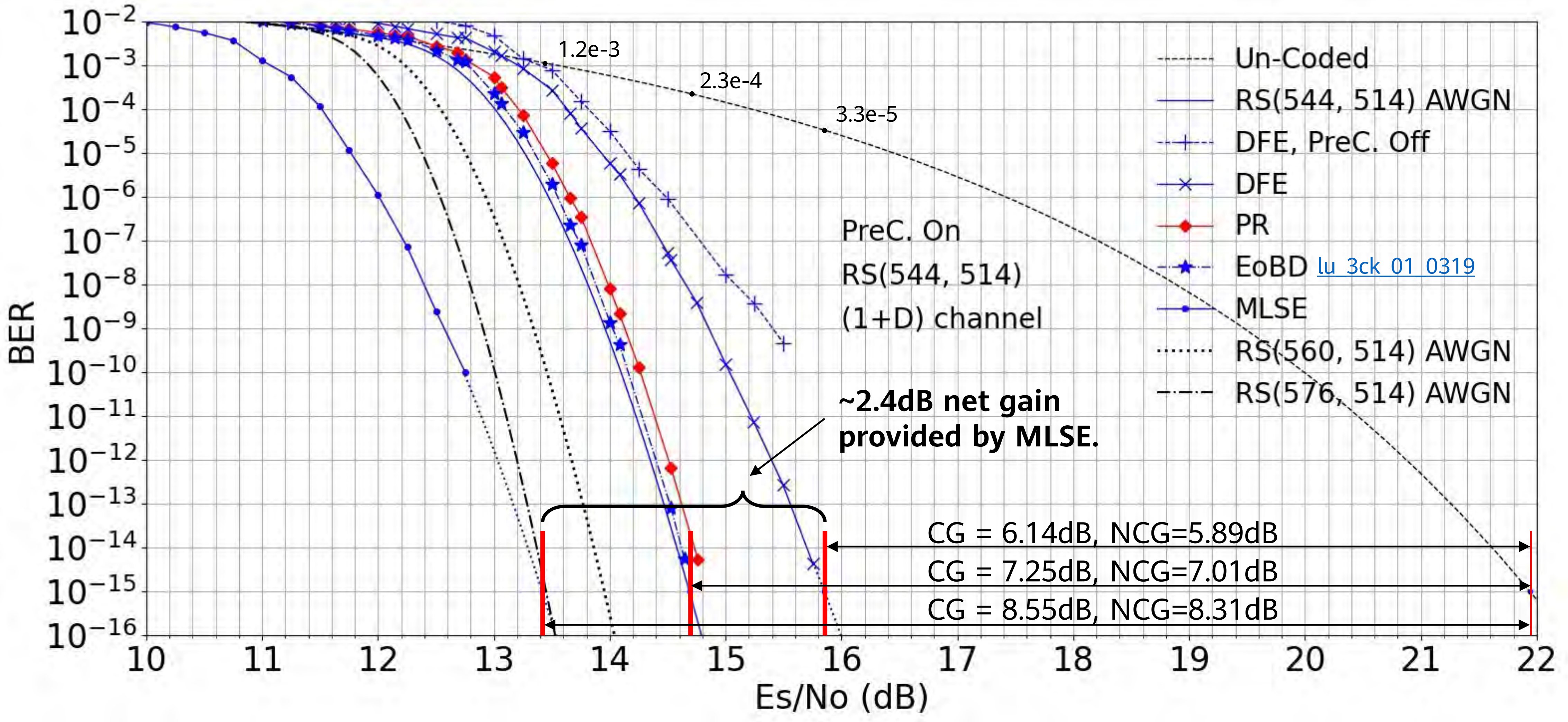


FEC limit = 1e-3 / Stronger FEC		
Channel IL(dB)	Differential	Single-Ended
19/39 (Low)	>225Gbps	>>225Gbps
23/44 (Medium)	215Gbps	>>225Gbps
26/49 (High)	190Gbps	>>225Gbps

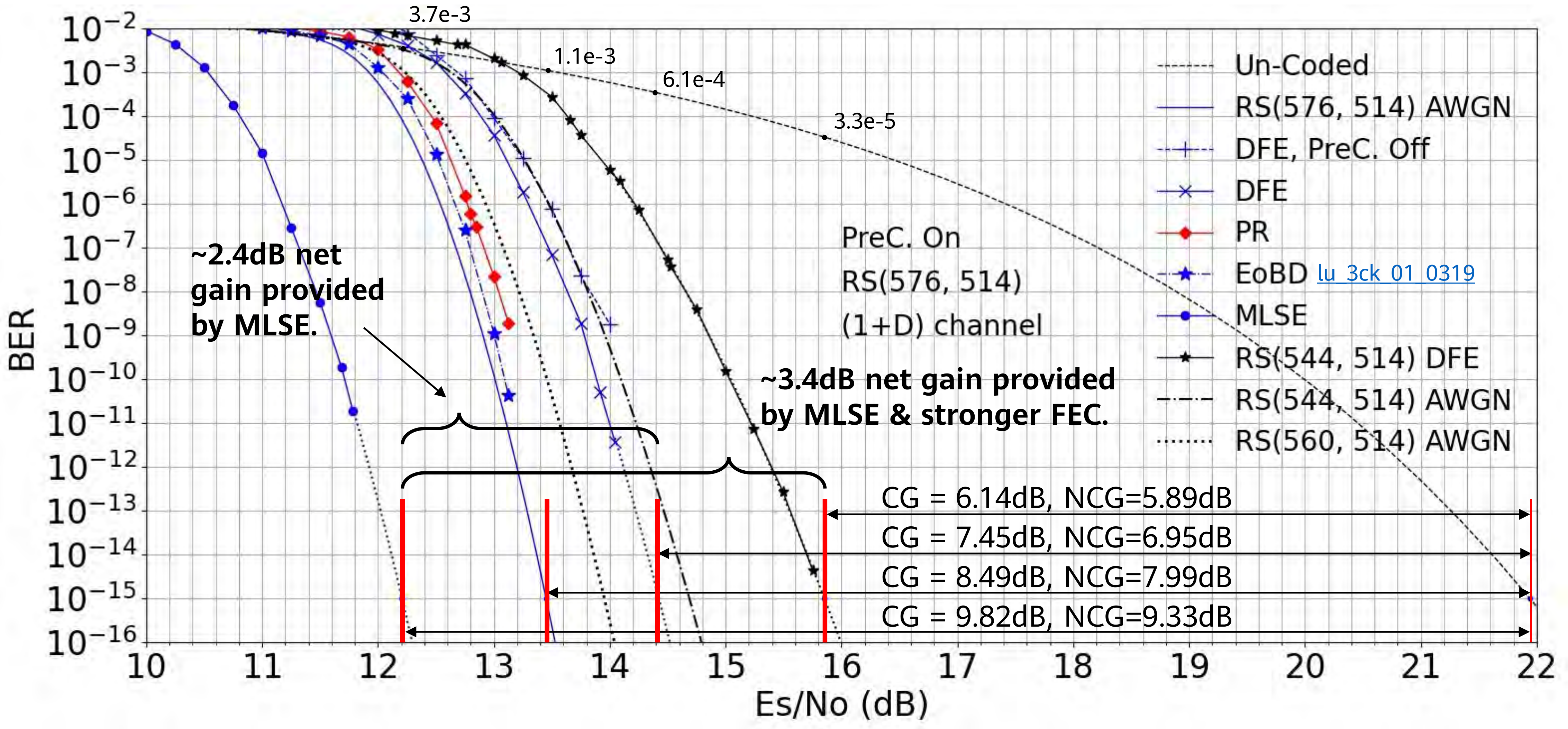
Simulation results (Bandwidth scaled up by 1.5x)



Reference for 200G FEC: 6% OH, RS(544, 514)



Reference for 200G FEC: 12% OH, RS(576, 514)



Summary, discussion and recommendation

- Insertion loss target of CR & KR channels for PAM4 and SE PAM4.
  - Assume the improved package loss is ~6dB @ 26.56GHz & ~12dB @ 53GHz.
    - Optimistic compared with noujeim_b400g_01_210517 .
  - PAM4:
    - Bump-to-Bump, ~18dB @ 26.56GHz & ~35dB @ 53GHz
    - Ball-to-Ball, ~**12dB** @ 26.56GHz & ~23dB @ 53GHz
    - “112G PAM4 XSR channel” extend bandwidth beyond 50GHz.
  - SE PAM4:
    - Bump-to-Bump, ~28dB @ 26.56GHz
    - Ball-to-Ball, ~**22dB** @ 26.56GHz
    - “112G PAM4 MR channel” with single-ended signaling optimization.
- Crosstalk optimization of CR & KR channels for PAM4 and SE PAM4.
  - PAM4: High frequency cross talk suppression beyond 50GHz.
  - SE PAM4: Single-ended signaling optimization within 50GHz.

Summary, discussion and recommendation

- **MLSE** can provide **~2.4dB** net gain over RS(544, 514) or stronger FEC.
- **Stronger FEC** can provide **~1.0dB** net coding gain.
- **MLSE and stronger FEC** can provide **~3.4dB** net gain.
  - Net coding gain ~= **9.33dB**
  - Pre-FEC random BER ~= **3.7e-3**.
- **Call for actions:** analysis/reference design of 200G channels.
- **N*200G (N=4, 2, 1), PHYs (CR & KR) are proposed as objectives.**

Thanks!
Q&A