



# Clarifying misinterpretation of ACT

Contribution to 802.3dm Task Force

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# Introduction

- This presentation attempts to correct some of misunderstanding about ACT that was present in the New Orleans presentation  
[https://www.ieee802.org/3/dm/public/0525/Chini\\_3dm\\_02a\\_0525.pdf](https://www.ieee802.org/3/dm/public/0525/Chini_3dm_02a_0525.pdf)
- There were number of misunderstandings in the [Chini\\_3dm\\_02a\\_0525](#) presentation that are direct misreading of presentations that have been made by me, Ragnar Jonsson
- This presentation will attempt to point out and correct misunderstanding in the [Chini\\_3dm\\_02a\\_0525](#) presentation that can be traced directly to my earlier presentations
- Pointing out misunderstanding in the work of others can sometimes be perceived as being hostile or condescending. I hope that this presentation does not come across that way, and I will try my best to only focus on correcting misunderstanding that I may have caused.

# Key Misunderstandings

What was misunderstood	Clarification
On page 4 of <a href="#">Chini 3dm 02a 0525</a> it is misstated that the simulation uses 1-tap FFE and 1-tap DFE	No equalization is needed for the upstream ACT receiver
On page 9 of <a href="#">Chini 3dm 02a 0525</a> it is misstated that for the upstream direction ACT will need an ADC, full DME, and FFE.	No equalization is needed for the upstream ACT receiver, and no digital processing is needed
On page 10 of <a href="#">Chini 3dm 02a 0525</a> it is misstated that ACT only uses 10-bit RS (360,326) FEC	The upstream ACT receiver uses much simpler RS-FEC than what is used in TDD
On page 9 of <a href="#">Chini 3dm 02a 0525</a> there is comparison of the complexity of high-performance simulation implementation and low-performance analog implementation	The simulation is a conceptual simplification and is not intended as a “suggested” design
On page 9 of <a href="#">Chini 3dm 02a 0525</a> there are incorrect performance numbers quoted for ACT, based on the performance of the “good” and “bad” cables from <a href="#">jonsson 3dm 02 09 15 24</a>	The “bad” cable should not be used to evaluate PHY performance, but the 16dB+ SNR performance of the simulated ACT PHY is very good
On page 9 of <a href="#">Chini 3dm 02a 0525</a> there is comparison of the performance of ACT PHY vs TDD PHY, which quotes TDD performance for “easy” cables and ACT performance for “bad” cables, and incorrectly states that ACT performance is significantly worse than TDD	The reference TDD analogue based PHY will not work on the “bad” cable, where the simulated ACT PHY works with 16dB+ SNR
On page 5 of <a href="#">Chini 3dm 02a 0525</a> it is stated that for the “bad” cable the main challenge is the low frequency echo	The abnormally high low frequency echo does degrade the ACT performance in this simulation, but the primary challenge is the secondary reflections

# Misunderstanding #1

## What was misunderstood:

On page 4 of [Chini 3dm 02a 0525](#) it is misstated that the simulation uses 1-tap FFE and 1-tap DFE

## What was actually stated:

The [jonsson 3dm 02 03 10 25](#) presentation showed the output of AFE without any equalization being performed. This had been explicitly stated in previous presentation [jonsson 3dm 01b 01 20 25](#)

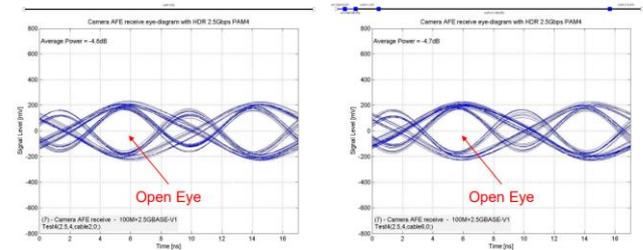
## Clarification:

No equalization is needed for the upstream ACT receiver

- ACT-simDM, uses **30 taps of fractional FFE** and **10 taps of DFE** for downstream receiver and **1-tap FFE** with **1-tap DFE** for upstream receiver. The **ADC** digitization effect is not modeled (i.e. assumed negligible).

From page 4 of [Chini 3dm 02a 0525](#)

## LDR Eye for Low and High Echo Cables



From page 6 of [jonsson 3dm 02 03 10 25](#)

## Simulation of Equalizer and Echo Cancellation

- **No echo cancellation** is used for either high or low data rate signals
- **No equalization** is used for the 100Mbps DME signal
- T/2-spaced equalizers are used for the high data rate signals, to minimize ambiguity due to sampling phase at the ADC
- The equalizer has 30 FFR taps and 10 DFE taps
- Equalizer coefficients for high data rate signals are calculated using line probing signals and closed form minimum mean square equalizer algorithm from [1]
  - The noise estimate is set to zero, so this becomes zero-forcing equalizer solution

[1] R. H. Jonsson, "DSL Channel Equalization" in *Fundamentals of DSL Technology* P. Golden, H. Dedieu, and K. S. Jacobsen, Eds. CRC Press, 2005, pp. 299-350.

From page 5 of [jonsson 3dm 01b 01 20 25](#)

# Misunderstanding #2

## What was misunderstood:

On page 9 of [Chini 3dm 02a 0525](#) it is misstated that for the upstream direction ACT will need an ADC, full DME, and FFE.

## What was actually stated:

The [jonsson 3dm 02 03 10 25](#) presentation showed that no equalization is needed for the ACT upstream receiver and there is no need for ADC.

It is clearly stated [jonsson 3dm 01b 01 20 25](#) that NO equalization is used for the 100Mbps!

## Clarification:

No equalization is needed for the upstream ACT receiver, and no digital processing is needed

- For upstream direction, a high performance receiver for TDD uses a DFE with total of 6 add/subtract taps where as ACT needs an ADC, full size DME and FFE (multipliers not adders). The calculated SNR for ACT is 20dB while for TDD, it is 26.7dB to 32dB depending on return loss effect on the secondary reflections<sup>1,2</sup>. TDD processes 1680bits in 9.6us (175MSPs) where as ACT processes 234MSPs continuously.

- [https://www.ieee802.org/3/dm/public/0325/Chini\\_3dm\\_02b\\_0325.pdf](https://www.ieee802.org/3/dm/public/0325/Chini_3dm_02b_0325.pdf)
- [https://www.ieee802.org/3/dm/public/0325/zimmerman\\_ILD\\_3dm\\_01\\_03052025.pdf](https://www.ieee802.org/3/dm/public/0325/zimmerman_ILD_3dm_01_03052025.pdf)

From page 9 of [Chini 3dm 02a 0525](#)

## Simulation of Equalizer and Echo Cancelation

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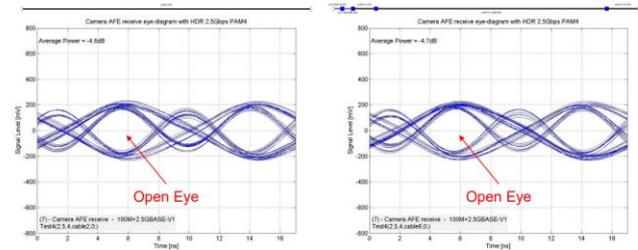
[1] R. H. Jonsson, "DSL Channel Equalization" in *Fundamentals of DSL Technology* P. Golden, H. Dedieu, and K. S. Jacobsen, Eds. CRC Press, 2005, pp. 299-350.

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## LDR Eye for Low and High Echo Cables



From page 6 of [jonsson 3dm 02 03 10 25](#)

# Misunderstanding #3

- TDD uses an 8-bit RS (130, 122) code while ACT uses a 10-bit RS (360, 326) code as in 802.3ch.

From page 10 of [Chini\\_3dm\\_02a\\_0525](#)

## What was misunderstood:

On page 10 of [Chini\\_3dm\\_02a\\_0525](#) it is misstated that ACT only uses 10-bit RS (360,326) FEC

## What was actually stated:

The [jonsson\\_sedarat\\_lo\\_3dm\\_01a\\_11\\_11\\_24](#) presentation, and multiple presentations since then, clearly state that upstream ACT uses 6-bit RS(50,46)

## Clarification:

The upstream ACT receiver uses much simpler RS-FEC than what is used in TDD

## Closer Look at RS(50,46,6)

- Latency
  - The RS(50,46,6) FEC will introduce about 2.5-3us latency when FEC decoding is active, which in some applications is higher than desired
  - If the FEC decoding is not active this latency reduces to about 0.4us
- Burst correction
  - The RS(50,46,6) FEC with line rate of 117.1875Mb/s can correct over 50ns error bursts
- Flexibility
  - The text proposal assumes MII with 16B/17B blocks, but the same FEC code could also support XGMII with 64B/65B blocks, if Task Force selects XGMII over MII for low rate
- Complexity
  - The complexity of the FEC decoder is higher than for some of the alternative ACT candidates, but is still a very small portion of the overall PHY complexity

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# Misunderstanding #4

## What was misunderstood:

On page 9 of [Chini 3dm 02a 0525](#) there is comparison of the complexity of high-performance **simulation** implementation and low-performance analog implementation

## What was actually stated:

The [jonsson 3dm 01b 01 20 25](#) presentation explains the simulation environment and explains how it is defined to avoid simulation problems. To avoid “implementation specific” artifacts in the simulation the simulation is more complex than it must be.

## Clarification:

The simulation is a conceptual simplification and is not intended as a “suggested” design

- The receiver design for optimized performance includes a CTLE, HPF and a DFE<sup>1</sup> with analog implementation. The same equalizer design may be used on both sides of a link for 2.5Gbps/100Mbps.
- Such an equalizer is several times less complex than the one suggested for ACT downstream receiver (see pages 4 and 5 of this presentation). The big portion of savings is in the elimination of ADC, but also in eliminating FFE and reduced DFE.

From page 9 of [Chini 3dm 02a 0525](#)

## Simulation of Equalizer and Echo Cancellation

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From page 5 of [jonsson 3dm 01b 01 20 25](#)

# Misunderstanding #5

## What was misunderstood:

On page 9 of [Chini 3dm 02a 0525](#) there are incorrect performance numbers quoted for ACT, based on the performance of the “good” and “bad” cables from [jonsson 3dm 02 09 15 24](#)

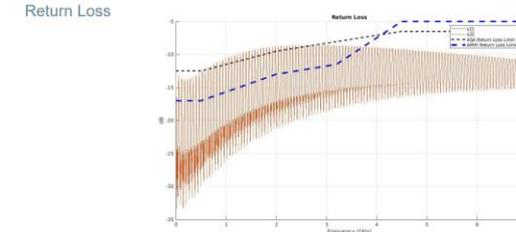
## What was actually stated:

The “bad” cable from [jonsson 3dm 02 09 15 24](#) was never intended to evaluate PHY performance. The cable was artificially constructed to demonstrate that secondary reflections are a potential problem. As was pointed out in the [ahuja 8023dm 01e 11112024 poorreturnloss equalization](#) presentation, this cable violates all RL limits and is worse than what is expected of real cables.

- The other obvious difference is in the performance, when dp-SNR is compared. For TDD, dp-SNR is 32dB with a typical<sup>1</sup> cable but dp-SNR may drop to 26.7dB due to secondary reflections<sup>2</sup> for cables with marginal RL. For ACT, dp-SNR is 16dB to 28.5dB depending on the channel return loss (see page 5 of this presentation).

From page 9 of [Chini 3dm 02a 0525](#)

### “Bad Connector” Channel Characteristics



- Return Loss for the channel breaches the RL limits for both ASA and A-PHY.
- Note that A-PHY is FDD/Full-Duplex.

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From page 9 of

[ahuja 8023dm 01e 11112024 poorreturnloss equalization](#)

## Clarification:

The “bad” cable should not be used to evaluate PHY performance, but the 16dB+ SNR performance of the **simulated** ACT PHY is very good

# Misunderstanding #6

## What was misunderstood:

On page 9 of [Chini 3dm 02a 0525](#) there is comparison of the performance of ACT PHY vs TDD PHY, which quotes TDD performance for “easy” cables and ACT performance for “bad” cables, and incorrectly states that ACT performance is significantly worse than TDD

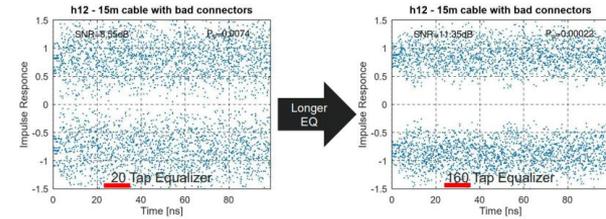
## What was actually stated:

The “bad” cable used in the Chini presentations comes from [jonsson 3dm 02 09 15 24](#), where it was demonstrated that TDD systems needed long equalizers to work on that cable. While the simulated ACT PHY works on the “bad” cable the TDD PHY with “eliminating FFE and reduced DFE” will simply not work on this cable.

- The other obvious difference is in the performance, when dp-SNR is compared. For TDD, dp-SNR is 32dB with a typical<sup>1</sup> cable but dp-SNR may drop to 26.7dB due to secondary reflections<sup>2</sup> for cables with marginal RL. For ACT, dp-SNR is 16dB to 28.5dB depending on the channel return loss (see page 5 of this presentation).

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## Good vs Bad Connectors – Longer Equalizer



Longer EQ can help mitigate the problem, somewhat

This drives up the relative cost and the power consumption of the PHY

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From page 6 of [jonsson 3dm 02 09 15 24](#)

## Clarification:

The reference TDD analogue based PHY will not work on the “bad” cable, where the simulated ACT PHY works with 16dB+ SNR

# Misunderstanding #7

## What was misunderstood:

On page 5 of [Chini 3dm 02a 0525](#) it is stated that for the “bad” cable the main challenge is the low frequency echo

## What was actually stated:

The “bad” cable used in the Chini presentations comes from [jonsson 3dm 02 09 15 24](#), where it was demonstrated that TDD systems needed long equalizers to work (and it violates all RL limits)

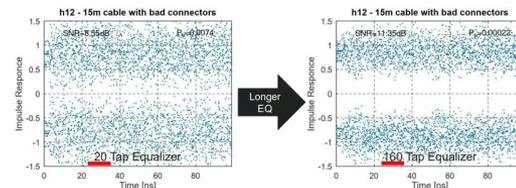
## Clarification:

The abnormally high low frequency echo does degrade the ACT performance in this simulation, but the primary challenge is the secondary reflections

For the “bad” channel, when echo path is forced to zero, SNR seen to be 21dB. Therefore, an SNR of 16dB is dominated by low frequency echo.

From page 5 of [Chini 3dm 02a 0525](#)

## Good vs Bad Connectors – Longer Equalizer



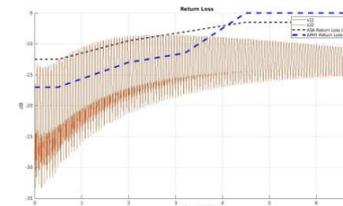
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From page 6 of [jonsson 3dm 02 09 15 24](#)

## “Bad Connector” Channel Characteristics

Return Loss



- Return Loss for the channel breaches the RL limits for both ASA and A-PHY.
- Note that A-PHY is FDD/Full-Duplex.

# Why this matters?

- The misunderstandings in the [Chini\\_3dm\\_02a\\_0525](#) presentation result in completely wrong conclusions
- Opposite to what is stated in the [Chini\\_3dm\\_02a\\_0525](#) presentation the following is true:
  - The 100Mbps ACT camera receiver is much smaller than the 3Gbps TDD camera receiver (this should not be a surprise for anyone)
  - The Multi-Gig ACT receiver is similar complexity as the TDD receiver
  - The simulated 2.5Gbps ACT receiver used in the presentation is so robust that it can operate over the “bad” cable, where the suggested analog based TDD receiver would fail completely

# Summary

- The [Chini 3dm 02a 0525](#) presentation has many misunderstandings about ACT and the conclusions are incorrect
- I encourage all participants to review the misunderstandings of ACT to form an accurate opinion based on the correct understanding of ACT
- Any presentation that claims that 100Mbps receiver is more complex than a 3Gbps receiver should be met with at least some minimal level of skepticism: In the [Chini 3dm 02a 0525](#) presentation this conclusion was based on unusually many misunderstandings

Multiple misunderstandings in [Chini 3dm 02a 0525](#) leads to **wrong conclusions**



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