delay. The transmit path data delay is expressed in units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in Register 1.1 (see 45.2.1.2.4).

Table 45–5—TimeSync WIS transmit path data delay register

Bit(s)	Name	Description	R/W[a]
2.1801.15:0	Maximum WIS transmit path data delay, lower	WIS_delay_TX_max [15:0]	RO, MW
2.1802.15:0	Maximum WIS transmit path data delay, upper	WIS_delay_TX_max [31:16]	RO, MW
2.1803.15:0	Minimum WIS transmit path data delay, lower	WIS_delay_TX_min [15:0]	RO, MW
2.1804.15:0	Minimum WIS transmit path data delay, upper	WIS_delay_TX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.2.22 TimeSync WIS receive path data delay (Registers 2.1805, 2.1806, 2.1807, 2.1808)

The TimeSync WIS receive path data delay register contains the maximum (Registers 2.1805, 2.1806, see Table 45–6) and minimum (Registers 2.1807, 2.1808, see Table 45–6) values of the receive path data delay. The receive path data delay is expressed in units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in Register 1.1 (see 45.2.1.2.4).

Table 45–6—TimeSync WIS receive path data delay register

Bit(s)	Name	Description	R/W[a]
2.1805.15:0	Maximum WIS receive path data delay, lower	WIS_delay_RX_max [15:0]	RO, MW
2.1806.15:0	Maximum WIS receive path data delay, upper	WIS_delay_RX_max [31:16]	RO, MW
2.1807.15:0	Minimum WIS receive path data delay, lower	WIS_delay_RX_min [15:0]	RO, MW
2.1808.15:0	Minimum WIS receive path data delay, upper	WIS_delay_RX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.3.66 TimeSync PCS capability (Register 3.1800)

The TimeSync PCS capability register (see Table 45–235) indicates the capability of the PCS to report the transmit data delay (in ns-resolution registers 3.1801 through 3.1804 and, separately, in sub-ns-resolution registers 3.1809 and 3.1810) and receive data delay (in ns-resolution registers 3.1805 through 3.1808 and, separately, in sub-ns-resolution registers 3.1811 and 3.1812).

Table 45–235—TimeSync PCS capability

Bit(s)	Name	Description	R/W[a]
3.1800.15:4	Reserved	Value always 0	RO
3.1800.3	TimeSync fine resolution transmit path data delay	1 = PCS provides information on transmit path data delay with sub-ns-resolution in registers 3.1809 and 3.1810 0 = PCS does not provide information on transmit path data delay with sub-ns-resolution	RO

Table 45–235—TimeSync PCS capability *(continued)*

Bit(s)	Name	Description	R/W[a]
3.1800.2	TimeSync fine resolution receive path data delay	1 = PCS provides information on receive path data delay with sub-ns-resolution in registers 3.1811 and 3.1812 0 = PCS does not provide information on receive path data delay with sub-ns-resolution	RO
3.1800.1	TimeSync transmit path data delay	1 = PCS provides information on transmit path data delay with ns-resolution in registers 3.1801 through 3.1804 0 = PCS does not provide information on transmit path data delay with ns-resolution	RO
3.1800.0	TimeSync receive path data delay	1 = PCS provides information on receive path data delay with ns-resolution in registers 3.1805 through 3.1808 0 = PCS does not provide information on receive path data delay with ns-resolution	RO

[a]RO = Read only

Furthermore, The TimeSync PCS capability register indicates the support for IEEE Std 802.3bf (register 3.1800.15) and IEEE Std 802.3cx (register 3.1800.14) TimeSync. Note that for backward compatibility reasons, the values in register 3.1800.15 are inverted, i.e., the value of 0 indicates the support for IEEE Std 802.3bf TimeSync.

Table 45–235—TimeSync PCS capability

Bit(s)	Name	Description	R/W[a]
3.1800.15	IEEE Std 802.3bf support	0 = PCS supports IEEE Std 802.3bf TimeSync 1 = PCS does not support IEEE Std 802.3bf TimeSync	RO
3.1800.14	IEEE Std 802.3cx support	0 = PCS does not support IEEE Std 802.3cx TimeSync 1 = PCS supports IEEE Std 802.3cx TimeSync	RO
3.1800.13:4	Reserved	Value always 0	RO
3.1800.3	TimeSync fine resolution transmit path data delay	1 = PCS provides information on transmit path data delay with sub-ns-resolution in registers 3.1809 and 3.1810 0 = PCS does not provide information on transmit path data delay with sub-ns-resolution	RO
3.1800.2	TimeSync fine resolution receive path data delay	1 = PCS provides information on receive path data delay with sub-ns-resolution in registers 3.1811 and 3.1812 0 = PCS does not provide information on receive path data delay with sub-ns-resolution	RO
3.1800.1	TimeSync transmit path data delay	1 = PCS provides information on transmit path data delay with ns-resolution in registers 3.1801 through 3.1804 0 = PCS does not provide information on transmit path data delay with ns-resolution	RO
3.1800.0	TimeSync receive path data delay	1 = PCS provides information on receive path data delay with ns-resolution in registers 3.1805 through 3.1808 0 = PCS does not provide information on receive path data delay with ns-resolution	RO

[a]RO = Read only