Some questions proposed for 802.3cx

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Background

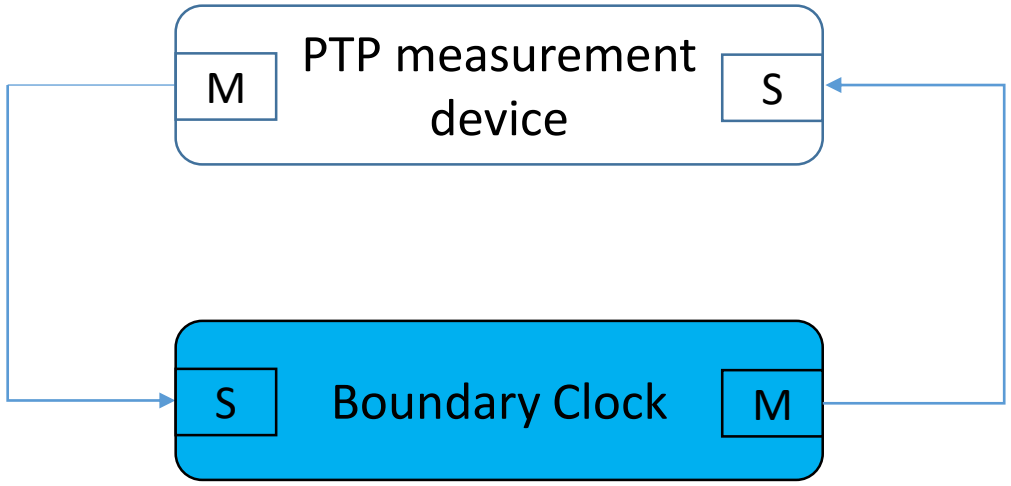
- Based on the requirement of ITU-T G.8273.2, the time error of the enhanced PTP clock is between +/- 5ns ~ +/- 30ns.

- The G.8273.2 has included some Ethernet interfaces, e.g., 1GE, 10GE, 25GE, 40GE and 100GE. Newer interfaces (50GE, 200GE, etc.) will be added in the future.

- Improving PTP timestamp accuracy is required to meet the enhanced clock requirement.

PTP clock test verification

- The figure below is the test platform to verify the Boundary Clock (BC).
  - The Slave port of BC gets four timestamps (T1/T2/T3/T4), and the BC uses four timestamps to calculate its time error and adjust its time. The message rate of both Sync and Delay_Req/Delay_Resp messages are 16hz.
  - The Slave port of PTP measurement device also gets four timestamps (T1/T2/T3/T4), and calculates the time error (TE). Finally, the PTP measurement device verifies whether TE meets the specs.



- **Therefore, the test results are actually affected by 4 Ethernet ports (2 ports of measurement device and 2 ports of BC).**

Factors affecting timestamp accuracy of BC

- Generally, the PTP accuracy of BC equipment is affected by several factors:
  - PTP filtering clock in the system card;
  - The synchronization time error between the system card and line cards;
  - **The accuracy of timestamps generated at the MAC layer of line card.**

- Based on the class C and D specs in ITU-T G.8273.2, the clock accuracy of the whole system is about +/- 5ns ~ +/- 30ns.

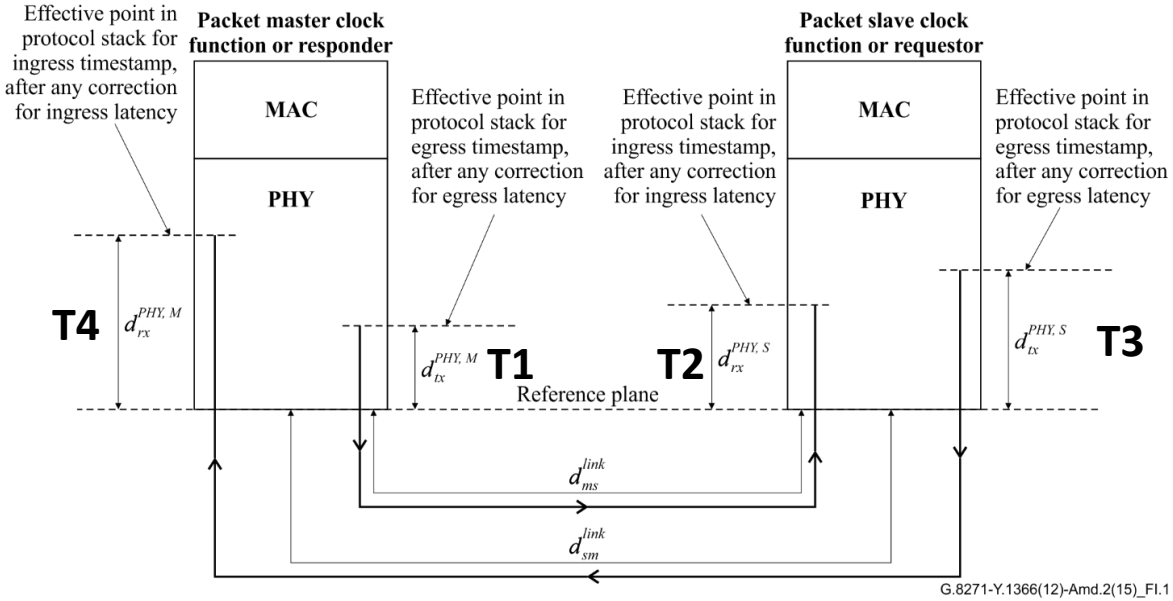
- Assuming 20% error budget caused by one PHY port, the accuracy of timestamps at the MAC layer is about +/-1ns ~ +/-6ns.

Timestamp accuracy caused by MAC/PHY

- The figure I.1 of ITU-T G.8271 also explains the timestamp accuracy caused by MAC or PHY layer,

$$e_{phy}^{M} = \frac{d_{tx}^{PHY,M} - d_{rx}^{PHY,M}}{2} \qquad e_{phy}^{S} = \frac{d_{tx}^{PHY,S} - d_{rx}^{PHY,S}}{2}$$

$$D_{asym} = e_{phy}^{M} + e_{link-asym} - e_{phy}^{S}$$



- If the delay of TX and RX for one port is symmetrical (with or without compensation), the time error of PTP clock is not affected.
  - The equations above can be revised as,

$$D_{asym} = e_{phy}^{M} + e_{link-asym} - e_{phy}^{S} = \frac{d_{tx}^{PHY,M} + d_{rx}^{PHY,S}}{2} - \frac{d_{tx}^{PHY,S} + d_{rx}^{PHY,M}}{2} + e_{link-asym}$$

(T1, T2, T3, T4)

This new equation shows, if the sum of TX and RX for one direction equals to the other direction, the time error of PTP clock is also not affected**.**

PHY Delay measurement in Clause 90 of IEEE 802.3

- Clause 90 of IEEE 802.3 defines a PHY delay measurement function, and registers to report these delays.
- The delay of each PHY sub-layer is reported separately, PMA/PMD, WIS, PCS, etc.
- The resolution of reported delay in each PHY sub-layer is 1ns, and this is mentioned in Clause 45.2.

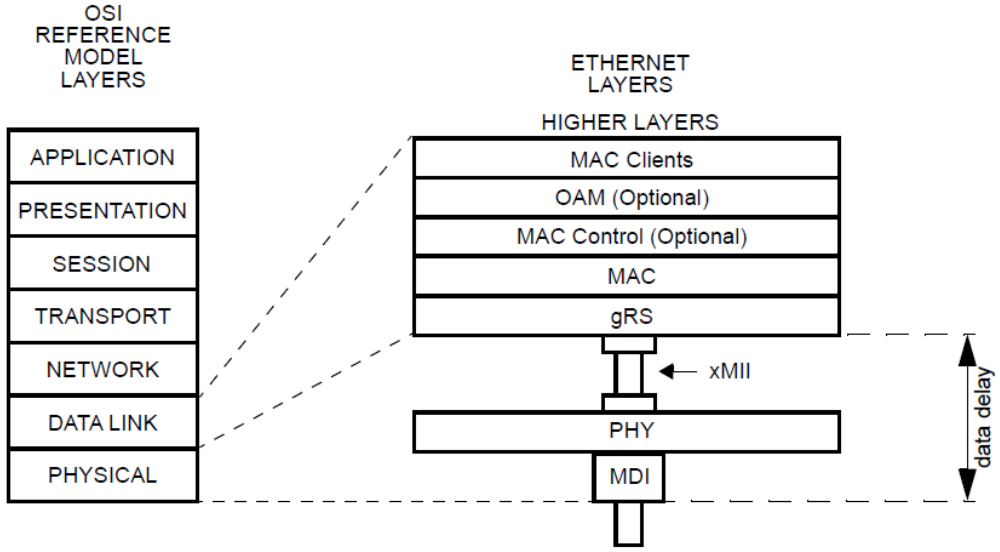


Figure 90–3—Data delay measurement

Table 90–1—Summary of TimeSync features in Clause 45

Register	Name	Reference
1.1800	TimeSync PMA/PMD capability register	45.2.1.146
1.1801 through 1.1804	TimeSync PMA/PMD transmit path data delay	45.2.1.147
1.1805 through 1.1808	TimeSync PMA/PMD receive path data delay	45.2.1.148
2.1800	TimeSync WIS capability register	45.2.2.20
2.1801 through 2.1804	TimeSync WIS transmit path data delay	45.2.2.21
2.1805 through 2.1808	TimeSync WIS receive path data delay	45.2.2.22
3.1800	TimeSync PCS capability register	45.2.3.66
3.1801 through 3.1804	TimeSync PCS transmit path data delay	45.2.3.67
3.1805 through 3.1808	TimeSync PCS receive path data delay	45.2.3.68
4.1800	TimeSync PHY XS capability register	45.2.4.28
4.1801 through 4.1804	TimeSync PHY XS transmit path data delay	45.2.4.29
4.1805 through 4.1808	TimeSync PHY XS receive path data delay	45.2.4.30
5.1800	TimeSync DTE XS capability register	45.2.5.28
5.1801 through 5.1804	TimeSync DTE XS transmit path data delay	45.2.5.29
5.1805 through 5.1808	TimeSync DTE XS receive path data delay	45.2.5.30
6.1800	TimeSync TC capability register	45.2.6.14
6.1801 through 6.1804	TimeSync TC transmit path data delay	45.2.6.15
6.1805 through 6.1808	TimeSync TC receive path data delay	45.2.6.16

Proposals for PHY delay measurement

- This presentation recommends some improvements to be considered by the task force.

① The PHY layer shall be allowed to report a total delay of all sub-layers, which could improve the accuracy of reported delay.
  - For example, for the case of PHY including PMA/PMD, WIS and PCS, if the delay of each sub-layer is reported separately, the accuracy of the total delay is 3ns, because the accuracy of each sub-layer is 1ns;
  - if the delay of all sub-layers can be reported as a total number, the accuracy could be 1ns.

② Improve the resolution of the reported delay from the current 1ns to a lower value, e.g., 0.1ns

Delay measurement in optical module

- Another question is the delay of optical module, the PHY layer of some interfaces are composed of chip and optical module.

  - For example, the PMA layer is required at both chip side and module side for 200GE/400GE .
  - The TX/RX delays of the optical module are suggested to be reported if they are **asymmetrical**.
  - Because the chip also includes a part of PMA function, the registers for the delay of both PMA layers should be defined.

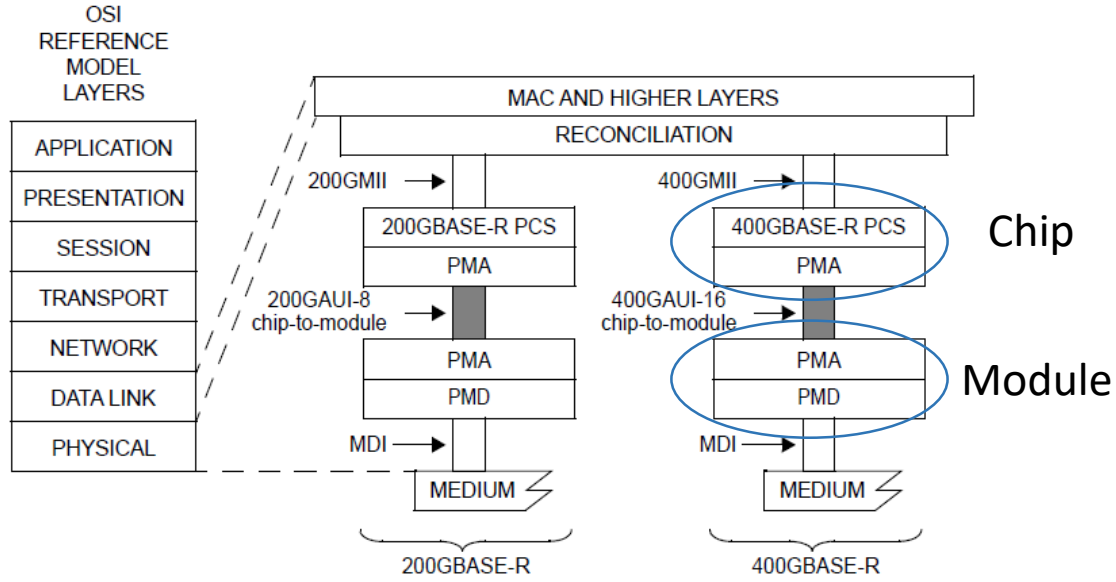


Figure 120C–1—Example 200GAUI-8 and 400GAUI-16 chip-to-module relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

Summary

- This presentation introduces the requirement of PTP clocks.

- Some recommendations are proposed to be considered by IEEE 802.3cx.
  ① The total delay of all sub-layers in the PHY layer should be reported as one.
  ② The resolution of delay can be improved, e.g., to 0.1ns.
  ③ The delay of optical module is recommended to be reported.

Thank you