Contribution to 802.3cx

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Open Questions

- Three question was put forward by Gorshe gorshe_1_0119.pdf and later suggested further updates by Nicholl nicholl_nea_01_190416.pdf.

- This presentation add further responses for the below three questions as outlined by Gorshe and Nicholl
  - Clarify Tx and Rx Path Data Delay
  - Clearly specify how AM and Idle insertion/deletion affect PTP timestamps
  - Clarify how to account for the lane distribution impact on the latency difference between the MII and the PHY of each lane

Proposed Text to Clarify Tx and Rx Path Data Delay (1 of 3)

- Redefinition of Time stamp point as proposed by Gorshe and Nicholl with proposed update of Clause 90.7 first paragraph is problematic.
  - In Nicholl Clause 90.7 proposed text:
    - The transmit path data delay is measured from the beginning of the first symbol after the SFD at the xMII input to the beginning of the first symbol after the SFD at the MDI output. The receive path data delay is measured from the beginning of the first symbol after the SFD at the MDI input to the beginning of the first symbol after the SFD at the xMII output.

Proposed Text to Clarify Tx and Rx Path Data Delay (2 of 3)

- In Nicholl Clause 90.7 proposed text:
  - For a PHY that includes an FEC function, the transmit and receive path data delays may show significant variation depending upon the position of the beginning of the first symbol after the SFD within the FEC block. However, since the variation due to this effect in the transmit path is expected to be compensated by the inverse variation in the receive path, it is recommended that the transmit and receive path data delays be reported as if the beginning of the first symbol after the SFD is at the start of the FEC block.

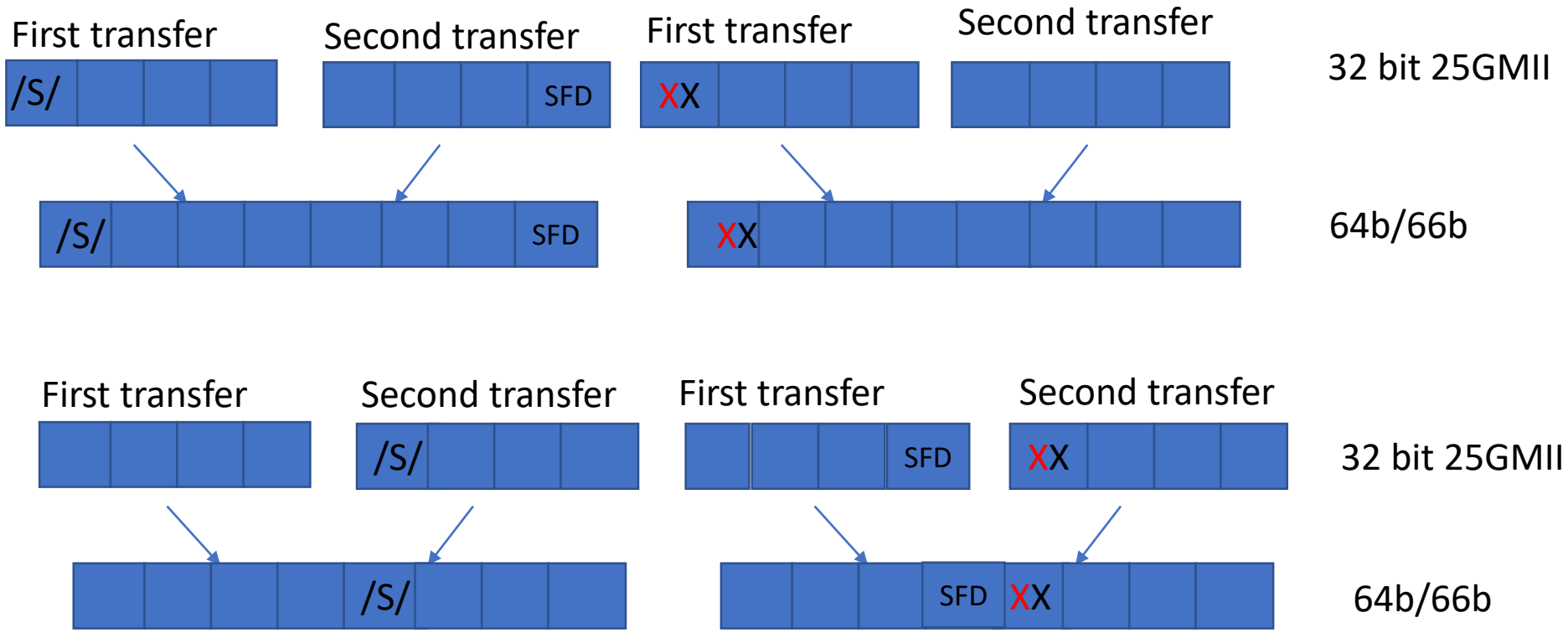
Proposed Text to Clarify Tx and Rx Path Data Delay (2 of 3) – Problem

- The proposed update to Clause 90 would pose a interoperability concern regarding 25Gbps with RS-FEC enabled if implemented with a Clause 106 RS interface with 32 bit wide 25GMII.

- As Clause 106 with 32 bit wide 25GMII allows /S/ on first octet, depending on the alignment of the /S/ in First transfer or Second transfer the SFD and first symbol after SFD might be encoded in different 64B/66B blocks. By this its possible that SFD and first symbol after SFD are encoded into different 256B/257B blocks and subsequently encoded into different RS-FEC blocks.

- With the proposed update a timestamp taken with a implementation according to current Clause 90 could differ by one RS-FEC frame length of 5280UI. Degrading timestamp performance on implementations aligned to current definition.

Exemplification of Clause 107 32 bit 25GMII to 64b/66b bit mapping



- Exemplification of Clause 107 potential of separating SFD and proposed new timestamp point indicated in RED

Proposed Text to Clarify Tx and Rx Path Data Delay (3 of 3)

- Agree with Nicholl for proposed update of Clause 90.7 third paragraph.

- In Nicholl Clause 90.7 proposed text:
  - The receiver of a multi-lane PHY is expected to include a buffer to compensate for skew between the lanes. This buffer selectively delays each lane such that the lanes are aligned at the buffer output. The earliest arriving lane experiences the most delay through the buffer and the latest arriving lane experiences the least delay through the buffer. The receive path data delay for a multi-lane PHY is reported as if the beginning of the first symbol after the SFD arrived at the MDI input on the lane with the smallest buffer delay.

AM Insert/Delete and Rate Adaptation

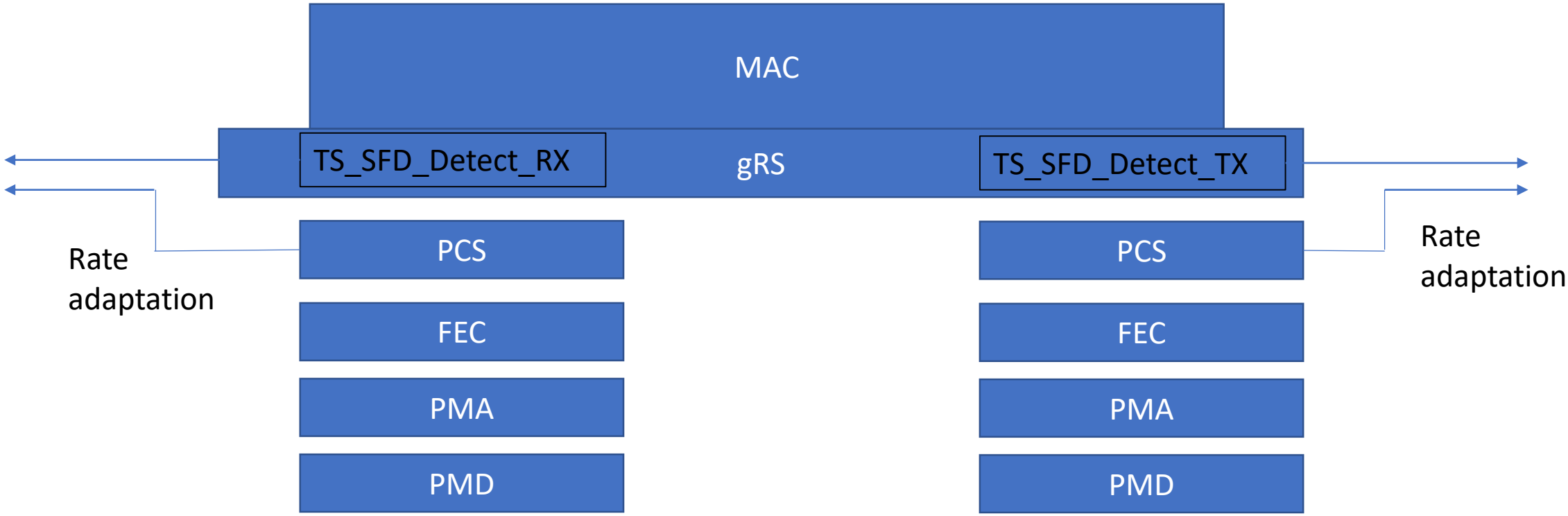
- Agree with Nicholl with proposed text and additions on next page adding clarification that only rate adaptation from AM insertions is applicable, not for CWM.
- In Nicholl Clause 90.7 proposed text to add after existing 90.7 paragraph 2:
  - For a PHY that inserts alignment markers or performs rate adaptation, the transmit path data delay measurement starting point (the beginning of the first symbol after the SFD at the xMII input) should be adjusted to account for alignment marker insertion or rate adaptation that occurs in the PHY (between the xMII input and the MDI output) which impacts the relative location of the beginning of the first symbol after the SFD. Based on this adjustment, the result is a transmit path data delay measurement that appears as if the alignment marker insertion or rate adaptation had been performed before the Tx xMII. Similarly, the receive path data delay measurement ending point (the beginning of the first symbol after the SFD at the xMII input) should be adjusted to account for any alignment markers or rate adaptation that occurred in the PHY (between the MDI input and xMII output) which impacts the relative location of the beginning of the first symbol after the SFD. Based on this adjustment, the result is a receive path data delay measurement that appears as if the alignment marker insertion or rate adaptation had been performed after the xMII.

Proposed Text to Clarify Effect of AM insert/delete and rate adaptation

- Clause 90.7 proposed text to add after existing 90.7 paragraph 2:
  - For a PHY that inserts alignment markers or performs rate adaptation for the purpose of AM insertion, the transmit path data delay measurement starting point ~~(the beginning of the first symbol after the SFD at the xMII input)~~ should be adjusted to account for alignment marker insertion or rate adaptation that occurs in the PHY (between the xMII input and the MDI output) which impacts the relative location of the beginning of the SFD ~~first symbol after the SFD~~. Based on this adjustment, the result is a transmit path data delay measurement that appears as if the alignment marker insertion or rate adaptation for the purpose of AM insertion had been performed before the Tx xMII. Similarly, the receive path data delay measurement ending point ~~(the beginning of the first symbol after the SFD at the xMII input)~~ should be adjusted to account for any alignment markers or rate adaptation for the purpose of AM insertion that occurred in the PHY (between the MDI input and xMII output) which impacts the relative location of the beginning of the SFD ~~first symbol after the SFD~~. Based on this adjustment, the result is a receive path data delay measurement that appears as if the alignment marker insertion or rate adaptation for the purpose of AM insertion had been performed after the xMII

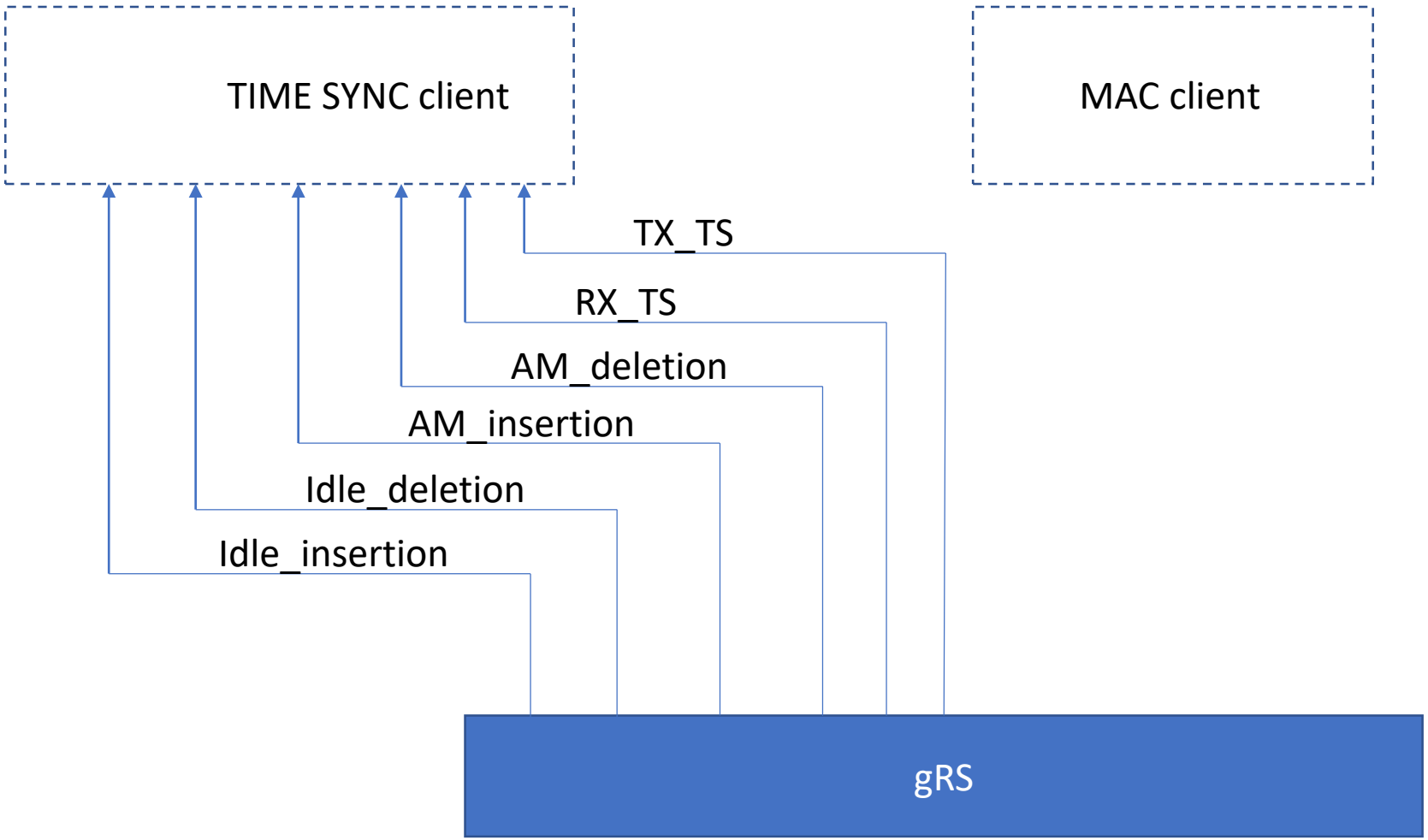
Effect of AM insert/delete and rate adaptation – Problem

- Clause 90.4.2 defines events for SFD RX and TX detection between gRS and TIME SYNC CLIENT through the TSSI
- With the proposed amendment to Clause 90.7 to account for AM insertion and rate adaptation additional information needs to be passed from PHY to TIME SYNC CLIENT through the gRS layer on a packet-to-packet basis.


MAC
TS_SFD_Detect_RX
gRS
TS_SFD_Detect_TX
Rate adaptation
PCS
FEC
PMA
PMD
PCS
FEC
PMA
PMD
Rate adaptation

TSSI interface additions for AM/IDLE insertion/deletion

- The rate adaptation signals in the TSSI would add to describing the proper handling of AM insertion/deletion and/or Idle.
- These signals would take on the value of TRUE when the corresponding event has been performed within the PHY.
- Possible primitives
  - AM_deletion.indication
  - AM_insertion.indication
  - Idle_deletion.indication
  - Idle_insertion.indication


TIME SYNC client
MAC client
TX_TS
RX_TS
AM_deletion
AM_insertion
Idle_deletion
Idle_insertion
gRS

Impact of Lane Distribution

- Agree with Nicholl that Method 2 proposed by Gorshe, is the preferred method and would be suitable for simpler and more complex Phy’s

Summary

- Problematic to redefine timestamp point for 25Gbps with RS-FEC enabled when implementing according to Clause 106 with an 32 bit wide 25GMII.
- Clause 90 and TSSI interface could be augmented by providing packet-by-packet timestamp and delay information through the gRS layer to TIME SYNC CLIENT

Thanks!