Basic Objectives

1. Define a scalable logical framework that can support arbitrary port speeds and counts while retaining as many of the feature in our Feature Objectives as possible.
2. Define an electrical interface to provide connectivity to a **single** Ethernet port with 8 or fewer pins operating at line speeds up to 100 Mb/s.
3. Provide **single** port connectivity without a SerDes.
4. Define an electrical interface to provide connectivity to as many as 8 ports, each with speeds up to 100 Mb/s using 8 or fewer pins.
5. Provide eight-port connectivity with a SerDes not to exceed 2 Gbps.

Feature Objectives

1. Provide an optional in-band MDIO management interface.
2. Support Energy Efficient Ethernet (EEE).
3. Support half-duplex operation.
4. Support Clause 148 PLCA.
5. Support full-duplex operation.
6. Support auto-negotiation (e.g. Clause 28, Clause 98)

Compatibility Objectives

1. Specify a MAC interface that maintains compatibility with Clause 96 PHYs.
2. Specify a MAC interface that maintains compatibility with Clause 97 PHYs.
3. Specify a MAC interface that maintains compatibility with Clause 146 PHYs.
4. Specify a MAC interface that maintains compatibility with Clause 147 PHY including support for Clause 148 PLCA.
5. Do not preclude support for proposed 100BASE-T1L PHYs (P802.3dg).
6. Do not preclude the transmission of PTP timestamps across the interface using in-band data.
7. Do not modify the preamble, thus precluding features that rely on the preamble being passed intact by the MII.