Impulse Immunity and FEC Objective

IEEE 802.3 Single Pair Multidrop Enhancements Study Group

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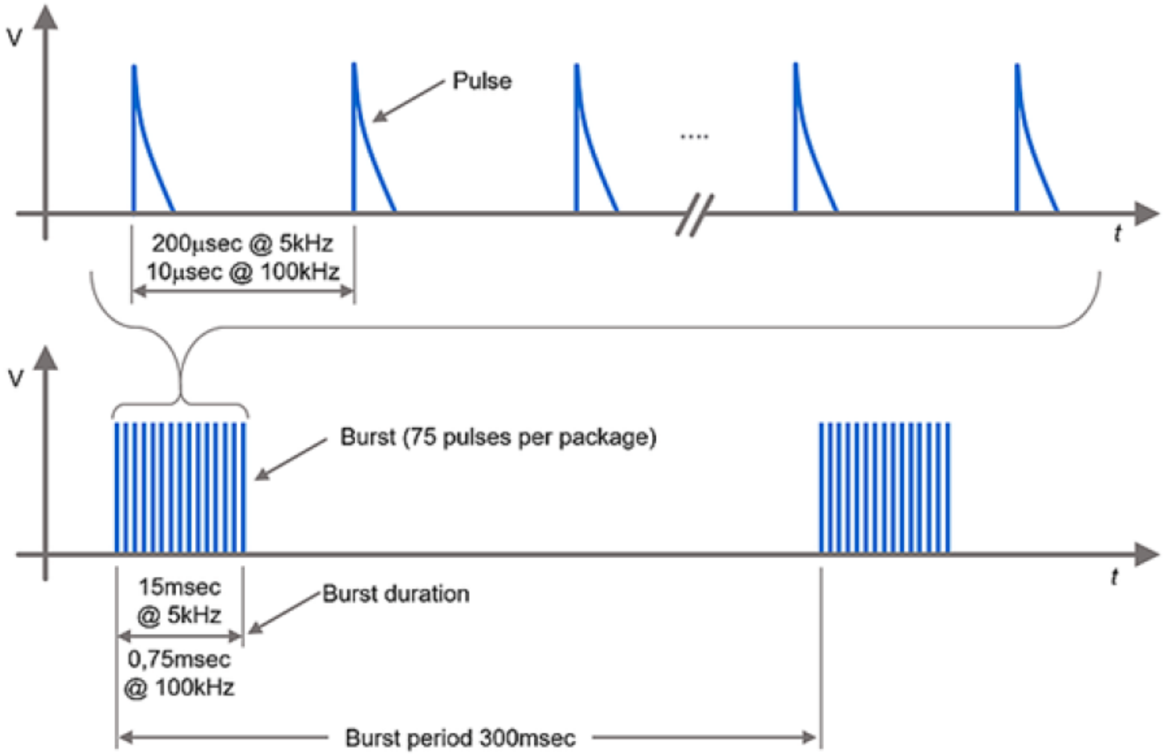
Part 1: Fast Transient Environments

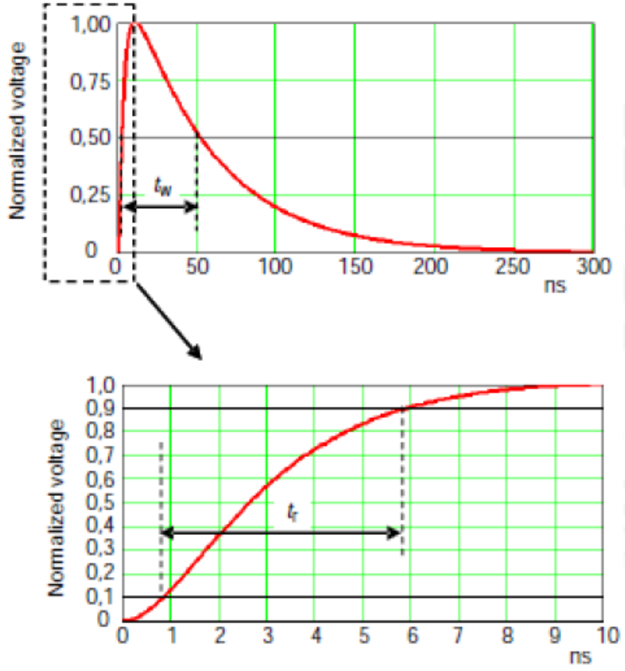
- Industrial, Building, and Vehicular environments have multiple sources of impulse noise
  - Lots of things with large current swings
  - Example: drive noise - http://www.ieee802.org/3/cg/public/May2017/brandt_cg_01b_0517.pdf
- These drive installation requirements which make installation more difficult
- IEC 61000-4-4 (EFT testing) is made to simulate some impulsive interference sources

Background: IEC 61000-4-4 test

Electrical Fast Transients (burst transients) are common mode disturbances coming from an arc when mechanical contact is open due to a switching process.

Similar disturbances could be observed from motor drivers and other load switching signals, if their cables bundled together with SPE cables.





Background: IEC 61000-4-4 setup

The test uses a capacitive clamp, that couples the common mode disturbances onto the SPE communication cable. The cable is run 10cm above the earthed conductive table, which is the reference surface (return path) for EFT pulses.

Open Circuit Test Voltage			61000-4-4 IEC:2012
Level	Power Line	I/O Line	
	Peak Voltage (kV)		Repetition Rate (kHz)
1	0.5	0.25	5 or 100
2	1	0.5	5 or 100
3	2	1	5 or 100
4	4	2	5 or 100
X_1	Special	Special	5 or 100

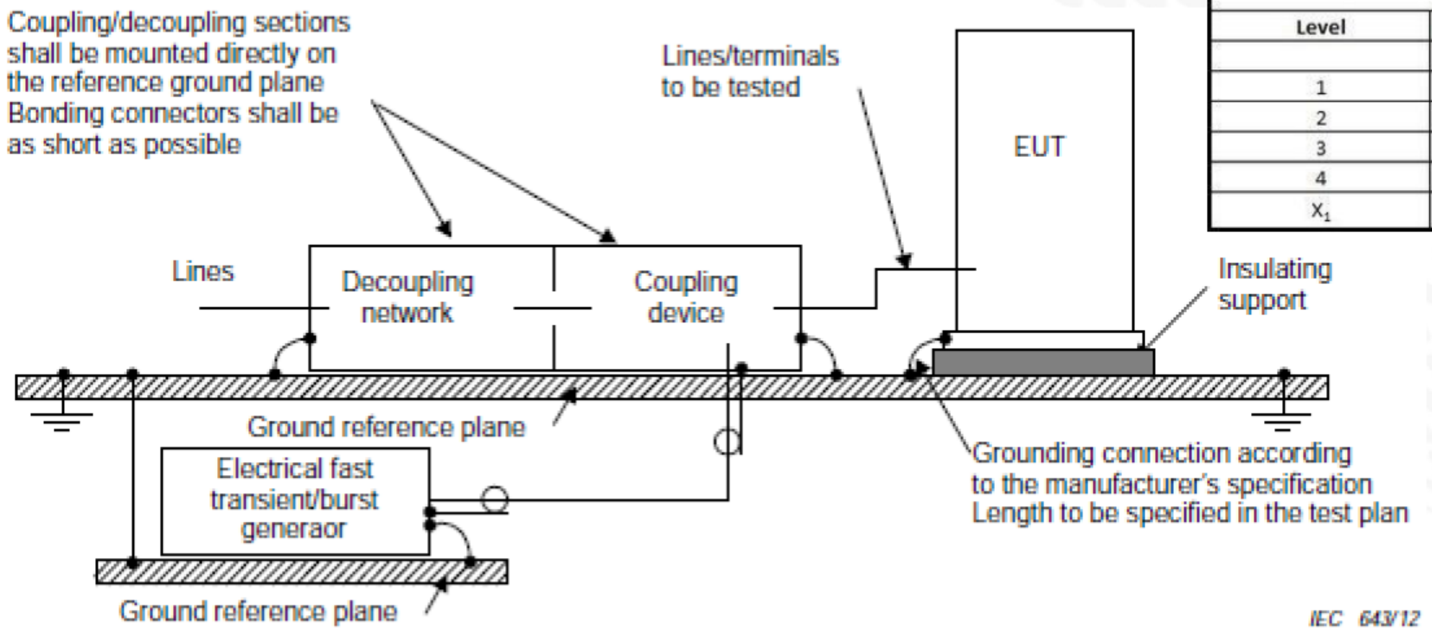


Figure 9 – Block diagram for electrical fast transient/burst immunity test

EFT pulses cause differential noise

Even for a nearly perfect cable with -50dB Mode Conversion, 1kV disturbance (common mode) can induce differential disturbance of 3.16V. In practice, the measured differential disturbances are over 14V in amplitude.

Lack of common mode termination to earth can induce reflections at the ends of the cable, making the disturbance return with increased amplitude. It can also make the pulse last much longer than the original pulse.

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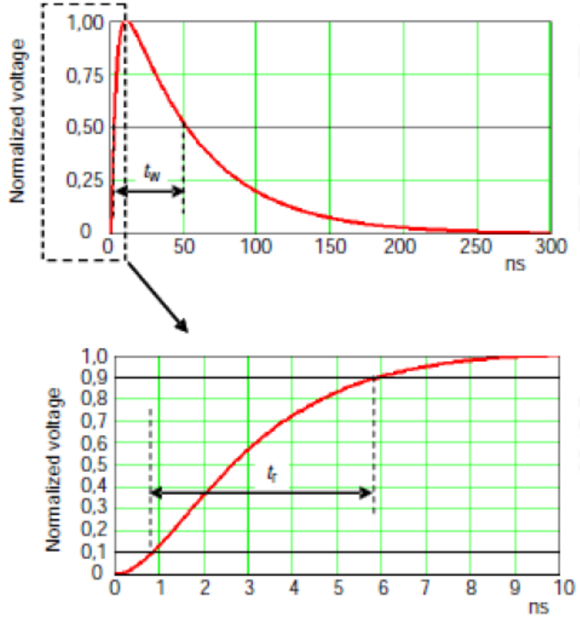
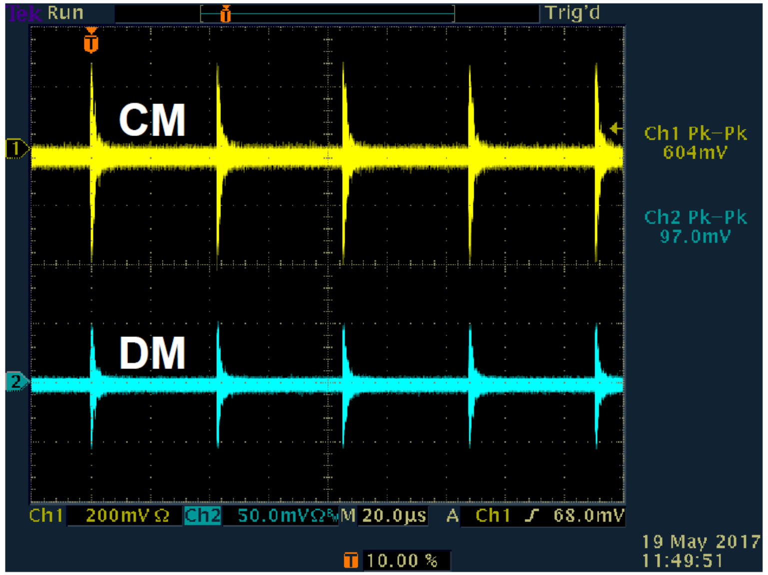


This is a Real-World Effect

Setup: Adjacent cables, Isolated GNDs, 0 Hz
Measurements: Drive end



- ~6x voltage reduction
- ~24 kHz

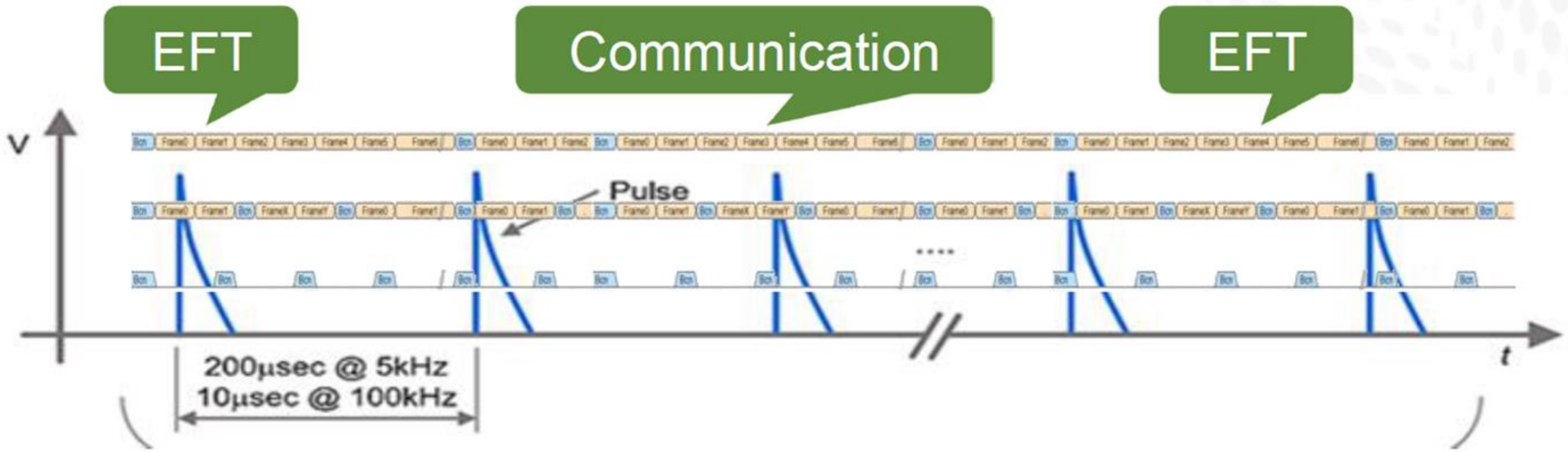
- Source: http://www.ieee802.org/3/cg/public/May2017/brandt_cg_01b_0517.pdf
- Shielding itself is sometimes not enough
- More immunity = more applications with easier installation
- Solutions could apply to point-to-point as well

Possible Solution: FEC for SPE

SPE communication cables can be bundled together with cables for switching loads (e.g. lighting applications), or run in proximity of motor drives (e.g. elevators).

Unlike EFT test, disturbances from motor drives or switching loads are not guaranteed to provide enough time for full, valid PLCA cycle.

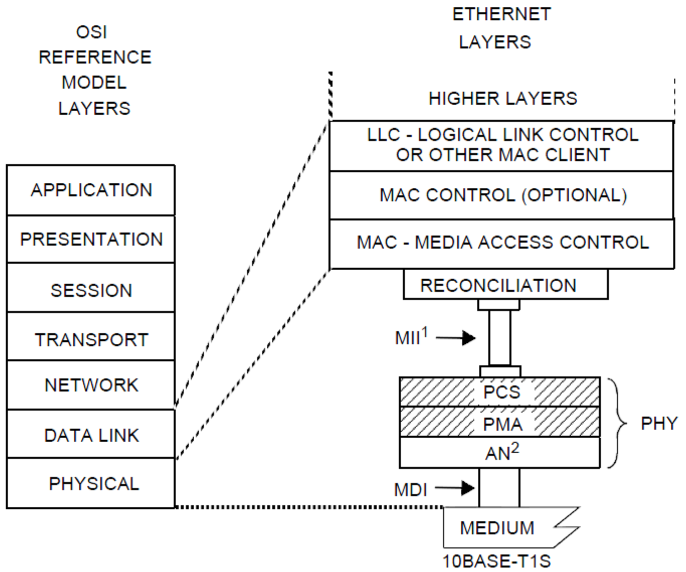
Usually, such disturbances usually destroy single data bits, so Forward Error Correction could prevent them from destroying the whole SPE frame or Beacon signal.



Part 2: FEC Objective/Tech Feasibility

- Potential objective:
- Support operation in impulsive interference environments such as IEC 61000-4-4 EFT testing
- NOTE: FEC is a technical solution, objectives should be about solving problems
  - FEC, a small gate count, is FAR lower relative cost than physical solutions in the installation

Layering in an FEC

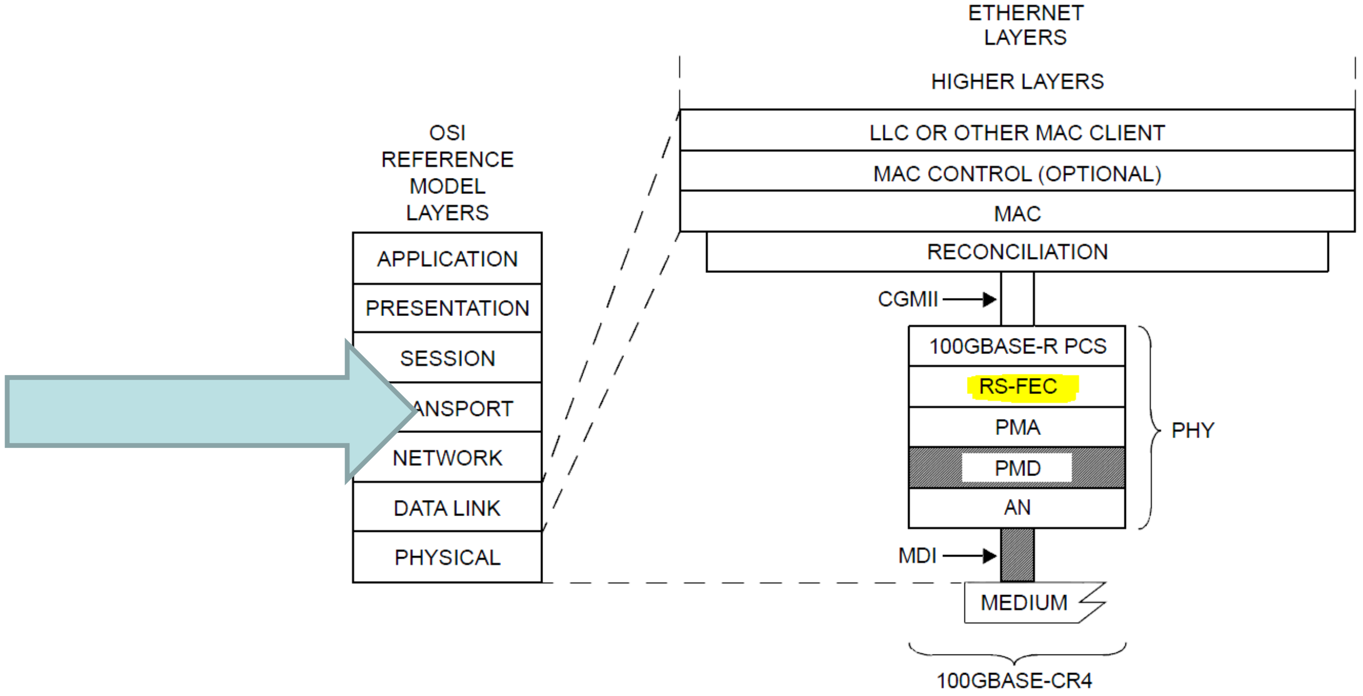


MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE

NOTE 1—MII is optional
NOTE 2—Auto-Negotiation is optional

PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
AN = AUTO-NEGOTIATION

Figure 147–1—Relationship of 10BASE-T1S PHY to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet Model



AN = AUTO-NEGOTIATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Source: IEEE Std 802.3cg-2019, Clause 147

Source: IEEE Std 802.3-2018, Clause 92 (annotated)

Basic requirements of FEC

- Low complexity
- Correct small bursts of errors
  - 50ns pulses generally cause errors in bursts of 5 to 6 bits
- Small block size
  - Fastest bursts (12kHz drive noise) tends to come about every 500 bit times, desire code only gets one burst
- Low overhead
  - Whatever we choose will require some extra transmission
  - Likely candidate is a small increase in DME clock rate

Example Implementation: 6-bit RS FEC

- (63, 59) 2-error correcting Reed-Solomon code
  - Blocks of 354 bits (44 bytes) become 378 transmitted encoded bits
  - Well-known low-complexity decoders correct any 6 bit error burst
    - Correct up to 12 bits if the burst aligns...
  - Overhead is low (6.8%).
- Encode all control and data words
- Provide an alternative mode with 6.8% faster clock-to-clock time
  - Self-clocking DME makes this straightforward

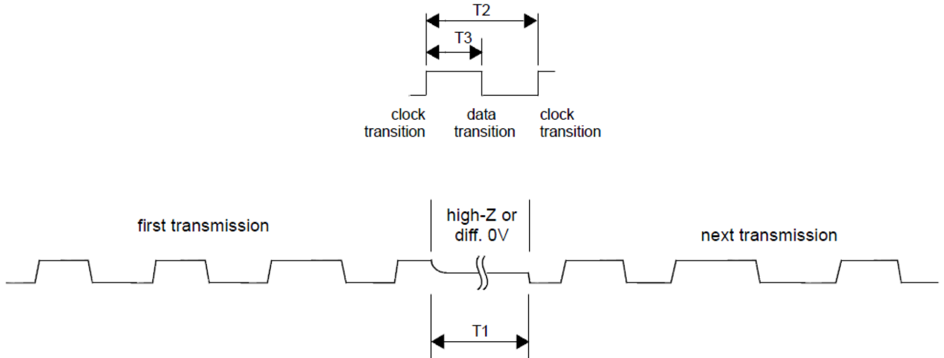


Figure 147–13—DME Encoding Scheme

Table 147–2—DME Timings

Parameter name	Description	Minimum value	Nominal value	Maximum value	Unit of measure
T1	Delay between transmissions	480	—	—	ns
T2	Clock transition to clock transition	–100 ppm	80	+100 ppm	ns
T3	Clock transition to data transition (data = 1)	38	40	42	ns

Becomes 74.92 when code is used

Source: IEEE Std 802.3cg-2019, Clause 147

Issues for Task Force

- Is FEC the right way to address operation in heavy impulsive environments
- Assuming we add FEC:
  – Is the increased rate and FEC a new "mode" for clause 147 or a new PHY type
  – There is no autonegotiation in multidrop – how do we want to signal this capability?
  – Do we modify the 4B/5B coding when used with FEC?

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THANK YOU!

Consensus
WE BUILD IT.

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