Comments on 802.3ab D1.1

ID	1
Commentor	Feuerstraeter
Comment Type	e
Section	
Page	40-37
Line	
Comment	The symbols | should be + in the diagram
Response	Accept, will change.

ID	2
Commentor	Feuerstraeter
Comment Type	e
Section	
Page	40-39
Line	
Comment	The top conditions should be combined pcs_reset=ON + …
Response	Accept in principle.

ID	3
Commentor	Feuerstraeter
Comment Type	e
Section	
Page	40-51
Line	
Comment	In the diagram Technology Direct should read Technology Detect
Response	Accept, will fix

ID	4
Commentor	Feuerstraeter
Comment Type	
Section	
Page	40-53
Line	
Comment	In tables 40-4,5 the Register address should be 10 not '0
Response	Accept, will fix

ID	5
Commentor	Feuerstraeter
Comment Type	e
Section	
Page	40-58
Line	
Comment	Table 40-58 should spell out in binary the message code(9)
Response	Accept, but plan to change--see comment 23

ID	6
Commentor	Feuerstraeter
Comment Type	e
Section	
Page	40-61
Line	
Comment	Table 40-9 has a old T2 statement in Set link_status_T2, should read link_status_1000T
Response	Accept, will change

ID	7
Commentor	Feuerstraeter
Comment Type	e
Section	
Page	40-62
Line	
Comment	Table 40-10 is missing 100Base-T2 Half Duplex
Response	Accept, will add T2 HD

ID	8
Commentor	Feuerstraeter
Comment Type	e
Section	
Page	40-3
Line	
Comment	Line 37 says 1000Base-T2, remove the '2'
Response	Accept, will change

ID	9
Commentor	Feuerstraeter
Comment Type	e
Section	
Page	40-4
Line	
Comment	Figure 40-3, TXD and RXD should be 8 bits wide, add GTX_CLK
Response	Accept, will change

ID	10
Commentor	Feuerstraeter
Comment Type	e
Section	
Page	40-52
Line	
Comment	Remove Editors Note
Response	Accept, will remove

ID	11
Commentor	Feuerstraeter
Comment Type	e
Section	
Page	40-58
Line	
Comment	Line 27, 1000Base-TT should be 1000Base-T
Response	Accept, will correct

ID	12
Commentor	Feuerstraeter
Comment Type	e
Section	
Page	40-58
Line	
Comment	Line 16, Message code should be 9, not 7
Response	Accept, in principle, actually it will be "8"--see comment 23

ID	13
Commentor	Feuerstraeter
Comment Type	e
Section	
Page	40-2
Line	
Comment	igure 40-1, should AUTONEG be shown the way it is?
Response	Figure 40-1 follows style of Clause 32

ID	14
Commentor	Feuerstraeter
Comment Type	e
Section	
Page	40-15
Line	
Comment	Add GTX_CLK to diagram
Response	Accept, will add

ID	15
Commentor	Feuerstraeter
Comment Type	e
Section	
Page	40-51
Line	
Comment	Transition term: NP=not capable should come from Base Page Exchange, not INIT state. Also NP capable/not capable refer to link partners ability, not local ability
Response	Accept, will fix

ID	16
Commentor	Feuerstraeter
Comment Type	e
Section	
Page	40-54
Line	
Comment	Bit 9.6 mispellings Se->See THis->Thi
Response	Accept, will fix

ID	17
Commentor	Feuerstraeter
Comment Type	e
Section	
Page	40-56
Line	
Comment	Bit 10.8 mispellings Se->See THis->This
Response	Accept, will fix

ID	18
Commentor	Feuerstraeter
Comment Type	e
Section	
Page	40-58
Line	
Comment	Add Note that Bits 15-11 are used by the auto negotiation process.
Response	Accept, will add

ID	19
Commentor	Feuerstraeter
Comment Type	e
Section	
Page	40-61
Line	
Comment	Line 13, SB15 should be SB10
Response	Accept, will change

ID	20
Commentor	Feuerstraeter
Comment Type	e
Section	
Page	40-61
Line	
Comment	Line 21, Change XXXXX to 2^10
Response	Accept, will change

ID	21
Commentor	Feuerstraeter
Comment Type	e
Section	40.3
Page	
Line	
Comment	I also have numerous comments regarding the training sequence and associated timers, but after talking with Sailesh, I'll wait till after Dallas to submit. This section is likely to change a good deal.
Response	OK

ID	22
Commentor	Kardontchik
Comment Type	T
Section	40.3
Page	
Line	
Comment	With the present state machine, as described in Fig 40-4,1) The Master is not guaranteed to be able to achieve DFE/FFE/timing_acquisition (in Phase II) before going to Echo/Next acquisition (in Phase III). The maximum that is guaranteed is DFE/FFE coefficients acquisition, but with wrong timing, since the Slave is allowed to transmit IDLES using its own internal clock during Phase II. 2) The Slave could achieve DFE/FFE/timing_acquisition (in Phase I) and then proceed to Echo/Next acquisition (in Phase II) ONLY IF IT CAN FREEZE ITS RECEIVER PLL DURING THE WHOLE DURATION OF PHASE II (1 msec ? 2 msec ?), since there are no transitions at its receiver input during Phase II. That is, there is no smooth transition from Phase I to Phase III for the Slave. Advantages of the proposed change: 1) The Master is not guaranteed to be able to achieve DFE/FFE/timing_acquisition (in Phase I) before going to Echo/Next acquisition (in Phase II). The maximum that is guaranteed is DFE/FFE coefficients acquisition, but with wrong timing. The Master could store these coefficients (acquired in Phase I) and load them in Phase III, if it wishes so. In other words, the proposed change does not affect the Master negatively. All what the Master can achieve in the present state machine, it can also achieve it with the new state machine I propose. 2) The Slave achieves DFE/FFE/timing_acquisition (in Phase II) and then proceeds to Echo/Next acquisition (in Phase III) WITHOUT ANY NEED TO FREEZE ITS RECEIVER PLL AT ANY TIME. The transition from Phase II to III is a smooth transition for the Slave. The scheme I propose presents therefore a significant advantage for the Slave, while it does not make any harm to the Master or to what a Master could achieve using the present state machine (Fig 40-4). Notice that the Slave has tougher tasks, such as 1) the Slave has to be able to perform both frequency and phase acquisition, whereas the Master needs to perform only phase acquisition. (*)2) the Slave has to transmit using the recovered clock, whereas the Master transmits using a clock derived from its local crystal oscillator. This puts another burden on the Slave, since it still has to comply with the same transmitted jitter specifications. Therefore, a protocol modification as I propose it, presents significative advantages to the Slave, that has clearly more difficult tasks to accomplish, without making in any way more difficult the tasks of the Master. (*) Frequency acquisition is not needed in the Master, if the Master decides to postpone any signal processing until Phase II. (Diagrams on file)
Response	Rejected as per vote at January interim.

ID	23
Commentor	Mick
Comment Type	T
Section	40.6.1.1
Page	40-52
Line	2
Comment	Change 1000BASE-T Technology Ability code from "9" to "8"
Response	Accept, fix

ID	24
Commentor	Mick
Comment Type	e
Section	40.6.1.1
Page	40-52
Line	1
Comment	delete spurious "12"
Response	Accept, will fix

ID	25
Commentor	Mick
Comment Type	e
Section	40.4.1.2
Page	40-16
Line	11
Comment	change "pairs of" to "four"
Response	Accept, will fix

ID	26
Commentor	Mick
Comment Type	e
Section	40.6.3.3
Page	40-58
Line	5
Comment	Should be figure 40-15
Response	Accept, will fix

ID	27
	Mick
	e
	40.6.3.3
	40-58
	11
Comment	Should be figure 40-15
Response	Accept, will fix

ID	28
Commentor	Mick
Comment Type	T
Section	40.6.3.3
Page	40-58
Line	16
Comment	Message Code should be "8"
Response	Accept, will fix

ID	29
Commentor	Mick
Comment Type	T
Section	40.6.3.4
Page	40-58
Line	23
Comment	Message Code should be "8"
Response	Accept, will fix

ID	30
Commentor	Mick
Comment Type	e
Section	40.6.3.4
Page	40-58
Line	30
Comment	Delete "Unformatted" from table heading--table shows formatted and unformatted next pages
Response	Accept, will change

ID	31
Commentor	Mick
Comment Type	e
Section	40.6.3.4
Page	40-58
Line	
Comment	In table identify type of page with page number (e.g., Page 0=Message Page)
Response	Accept, will do

ID	32
Commentor	Mick
Comment Type	T
Section	40.6.3.4
Page	40-58
Line	
Comment	Value for page 0 is (10-0) 00000001000
Response	Accept, will change

ID	33
Commentor	Mick
Comment Type	e
Section	40.6. 3.4
Page	40-58
Line	
Comment	Message Code should be 8
Response	Accept, will fix

ID	34
Commentor	Mick
Comment Type	e
Section	40.8.3.1
Page	40-88
Line	30
Comment	error rate specified in 40.1
Response	Accept, will fix

ID	35
Commentor	Creigh
Comment Type	T
Section	40.7
Page	
Line	
Comment	replace jitter section with new proposed text (as per emailed PDF
Response	Accept, will replace as per emailed PDF. Revised jitter equations (lines 6, 22 on 40-83 modified as per vote at January interim.

ID	36
Commentor	Koeman
Comment Type	e
Section	40.8.6.2.2
Page	40-90
Line	17
Comment	It appears that MDELFEXT is specified in an unusual manner: each of the 3 wire pairs involved has a different ELFEXT requirement. This may not be supported by the TIA. However, it seems that voltage sum performance is of concern. Why not request a voltage sum specification for ELFEXT? Once you know how to measure ELFEXT in the field (not a small problem to do this reliably, because of the sensitive range of FEXT, which is actually measured), a voltage sum computation and test is a snap.
Response	Accept in principle, resolution in process

ID	37
Commentor	Koeman
Comment Type	e
Section	40.8.2.3.1
Page	40-88
Line	8
Comment	There must be a typo in the frequency range for which RL > 15 - 10*log(f/20): intended must be 20 to 100 MHz.
Response	Accept, will fix

ID	38
Commentor	Koeman
Comment Type	e
Section	40.8.2.3
Page	40-88
Line	1
Comment	Both the transmittor and the receiver should have a source and load return loss specification respectively. These numbers interact worst case with the RL sources of the link itself. Note that the link definition does NOT include the instrument connection. To include the connector as part of the defined link is not really an option, because that makes verification of link return loss performance impossible.
Response	Reject, specified in 40.7.1.4.1

ID	39
Commentor	Koeman
Comment Type	e
Section	40.8.6.2.2
Page	40-90
Line	17
Comment	The FEXT performance of both the instrument connections at both ends must be specified. The very unfortunate situation that the FEXT of these connections should be added worst case to the ELFEXT performance of the defined link (of course the FEXT of the instrument connectors are subject to attenuation of the link). Since FEXT performance of connecting hardware can be very poor, this may have a significant impact on being able to run on cat 5 cabling. Fortunately, it is possible to design connections to the instrument with reasonably good FEXT performance. But it should be specified and testable.
Response	Accept in principle, will address with resolution of comment 50.

ID	40
Commentor	Creigh
Comment Type	tr
Section	40.3.5
Page	40-14
Line	4-45
Comment	The current state diagram sets a minimum duration of the various stages of the sequenced startup at 1 us. This will be too short and should be increased. For example, consider phase 2 where the Master is sending zeros and the Slave is sending Idles. This phase lasts until the Master starts transmiting idles. During this time the Master may be converging the DFE or it may be doing nothing if it plans to do blind convergence later. In this case the Master could switch on its transmitter after 1 us; however, the Slave has only had 1 us to converge its echo canceller which is not long enough so the canceller will not be properly converged. A better minimum duration time for each phase would be something like 1 ms. Therefore I propose that a 1 ms minphase_timer be added and the condition minphase_timer_done be added to the transitions between phases.
Response	Accept in principle, implementation in process

ID	41
Commentor	Creigh
Comment Type	tr
Section	40.4.1.2.3
Page	40-19,20
Line	25-30,40-45
Comment	loc_rcvr_status = Ok or !Ok.
Response	Accept subject to verification by Sailesh

ID	42
Commentor	Creigh
Comment Type	t
Section	40.4.1.2.3
Page	40-19
Line	36-40
Comment	The current method of encoding Sc(n)[0] results in 2 types of idles depending on whether tx_mode is SEND_I or SEND_N. This is an unnecessary complication when using 3-level idles during SEND_I. Currently tx_mode=SEND_I is used to stop the switching of Sc(0)[n] between Sy(n)[0] and ~Sy(n-1)[0] so that the scrambler state can be easily acquired during SEND_I; however, it is not necessary to have Sc(0)[n] switch between Sy(n)[0] and ~Sy(n-1)[0] at any time since Sc(n)[3:1] are switching this way and only 3 pairs must switch this way to allow a distinction between idle and data. The following change should reduce the number of IDLE types being monitored. Define Sc(n)[0] as: 0 if (tx_mode=SEND_Z) Sc(n)[3:1]=Sy(n)[3:1] else
Response	Accept in principle, implementation TBD

ID	43
Commentor	Creigh
Comment Type	t
Section	40.4.1.2.4
Page	40-20-21
Line	46-52,1-5
Comment	cext and cext_err are not specifically defined to exclude their being set during SEND_I although the text surrounding it could be read that way. To explicitly avoid their being set during SEND_I by signals at the GMII which would complicate the receiver alignment process cext(n) and cext_err(n) can be defined as: (n subscripts omitted) tx_error if ((tx_enable=0)&(Tx_D[7:0]=0x0F)&(tx_mode=SEND_N)) cext = 0 else tx_error if ((tx_enable=0)&(Tx_D[7:0]=0x1F)&(tx_mode=SEND_N)) cext_err = 0 else
Response	Withdrawn

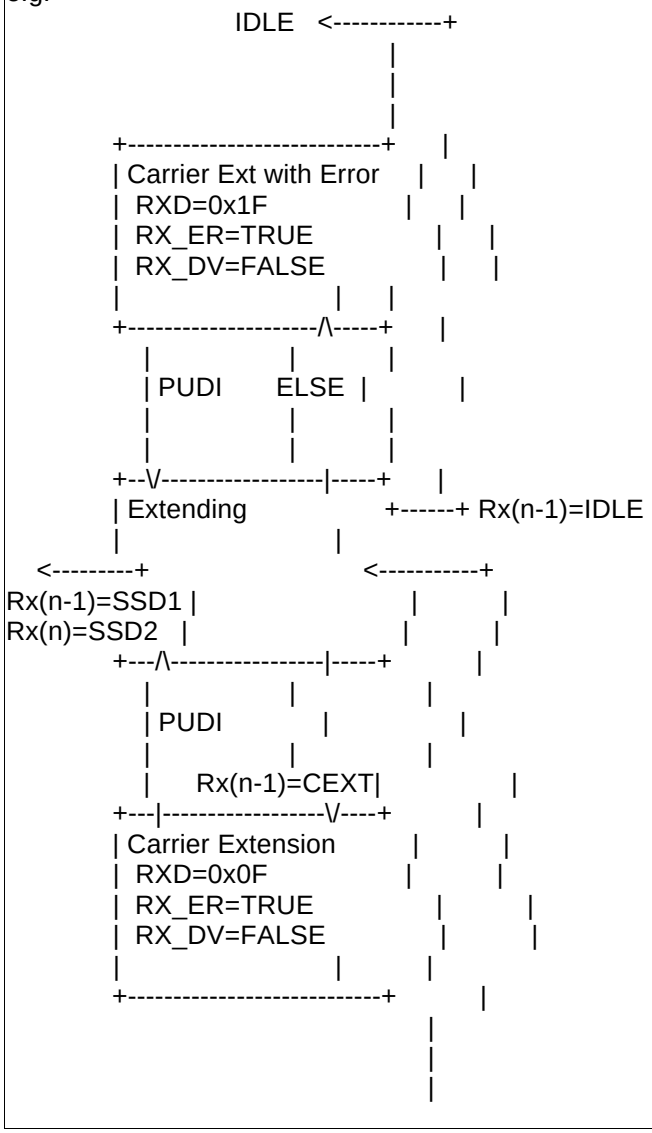
ID	44
Commentor	Creigh
Comment Type	t
Section	40.4.5.2
Page	40-38
Line	1-50
Comment	The condition: (tx_enabe=FALSE)&(tx_error=TRUE)&(TXD!=0x0F)&(TXD!=0x1F) is not covered from several states of the PCS Transmit State Diagram. Specifically, "ERROR CHECK", "1st CSExtend VECTOR", "2nd CSExtend VECTOR", and "ESD1 VECTOR with Extend" do not cover this case and should have an exit to the appropriate left most column of states. Additionally, the states "1stCSExtend_Err VECTOR", "2nd CSExtend_Err VECTOR", and "1st ESD_Ext_Err VECTOR" have an exit on tx_error=TRUE that should be conditioned as: (tx_error=TRUE) & (TXD=0x0F | TXD=0x1F) The exit tx_error=FALSE on these states should be conditioned as: (tx_error=FALSE)|((tx_error=TRUE)&(TXD!=0x0F)&(TXD!=0x1F)) Additionally, the if statement in the "SEND IDLE/CARRIER EXTENSION" case should read: if (tx_error=FALSE)|((tx_error=TRUE)&(TXD!=0x0F)&(TXD!=0x1F)) tx_symb_vector<=IDLE else if (TXD=0x0F) tx_symb_vector<=CEXT else if (TXD=0x1F) tx_symb_vector<=CEXT_Err
Response	Withdrawn

ID	45
Commentor	Creigh
Comment Type	t
Section	40.4.5.3
Page	40-39
Line	1-5
Comment	The state "LINK FAILED" should set receiving=FALSE to avoid an ambiguity about what happens once "LINK FAILED" is entered. There is an exit to "IDLE" that would then set receiving=FALSE but there is also an entry to the "LINK FAILED" state when (loc_rcvr_status!=OK)&(receiving=TRUE) which is not conditioned by coming from any state. Thus the intent of setting RX_ER true for one symbol interval and then shutting off receiving is ambiguously stated since the (loc_rcvr_status!=OK)&(receiving=TRUE) entry into "LINK FAILED" could be considered as having precedence over the PUDI exit to "IDLE".
Response	Accept, will fix

ID	46
Commentor	Creigh
Comment Type	t
Section	40.4.5.3
Page	40-39
Line	18-20
Comment	This is more a philosophical question about rxerror_status. Currently the state machine indicates rxerror_status when the idle is interrupted by a non-idle that is not at SSD only; however, the premature end of a frame can also be considered an error. Should we not add rxerror_status=ERROR to the "PREMATURE END" state?
Response	Withdrawn

ID	47
Commentor	Creigh
Comment Type	t
Section	40.4.5.3
Page	40-39
Line	15-25
Comment	The transitions out of Carrier Extension and Carrier Extension with Error are missing the PUDI qualifiers or the transitions out of ESD to CEXT_Err2 and ESD to CEXT2 need to be fixed or Carrier Extension and Carrier Extension with Error need to be changed to a structure like Data Error/Receive/Data (depending on the intent). Solution: Depends on what was originally intended.

e.g.



Response	Accept--apply to IDLE state as well
ID	48
Commentor	Campbell
Comment Type	tr
Section	40.7.1.4.1
Page	40-84
Line	32
Comment	Suggest the title of this sub-clause be changed from `MDI differential impedance' to `MDI Return Loss' since return is the requirement stated in the clause.
Response	Accept
ID	49
Commentor	Campbell
Comment Type	tr
Section	40.7.1.4.1
Page	40-84
Line	37,45
Comment	Suggest 125 MHz be changed to 100 MHz since the cable frequency limit is only 100 MHz.
Response	Accept

ID	50
Commentor	Campbell
Comment Type	t
Section	40.9.1
Page	40-91
Line	6
Comment	Recommend a requirement be included in this section for a FEXT loss requirement for the MDI connector. This is important because the FEXT noise buildup in the Category 5 link must be limited to ensure the BER objective is achieved. Although not specified in this section it is assumed the other electrical requirements will be those specified for connectors in ISO/IEC 11801. Suggest the following: The FEXT loss between all sets of contact pairs shown in Table 40-17 shall be at least 42 dB over the frequency range 1-100 MHz. This will require another column be inserted in Table 40-17 that will show the contact pairing.
Response	Accept in principle, values TBD, Editor's note: The connector is the connector provided with 1000BASE-T equipment

ID	51
Commentor	Campbell
Comment Type	tr
Section	40.8.2.3.1
Page	40-88
Line	7-16
Comment	Line 7: Add the following: The return loss for each duplex link shall be: Line 12: Change `2-100 MHz' to`20-100 MHz'. Line 8: Change `I5' to `15'. Line 14: Add the following: The reference impedance shall be 100 ohms. Line 16: Change Note to read: The Return Loss proposed for the next version of ISO/IEC 11801 meets this specification.
Response	Accept

ID	52
Commentor	Hinrichs
Comment Type	t
Section	40.8.2.3.1
Page	40-88
Line	12
Comment	On page 40-88, line 12, under section 40.8.2.3.1 Channel Return Loss, frequency range should be 20-100 MHz, not 2-100 MHz.
Response	Accept, will fix

ID	53
Commentor	Mlinarsky
Comment Type	t
Section	40.8.2.2.
Page	40-87
Line	26
Comment	Suggest omitting characteristic impedance as it is not an official Channel or Basic Link specification in either ISO 11801 nor TSB67. The return loss specification for a Channel or Basic Link adequately describes the required characteristic impedance.
Response	Accept in principle, will modify text to rpovide guidance sans "shalls" shall 1 to is, shall 2 to should. PROPOSED TEXT INSERT: "The differential characteristic impedence of the components used to provide the duplex link segment shall be 100 ohms as specified in ISO/IEC 11801 for Category 5.

ID	54
Commentor	Mlinarsky
Comment Type	t
Section	
Page	40-90
Line	26-35
Comment	Suggest replacing this description of ELFEXT limits with a worst case pair to pair ELFEXT specification and a worst case power or voltage sum ELFEXT specification. Specifying 3 different pair to pair limits is unconventional and inconsistent with the emerging addendum to TIA-568. Such a specification is also inconsistent with the specification for NEXT and will be very confusing to the end users.
Response	Accept in principle, will fix

ID	55
Commentor	Gladstone
Comment Type	t
Section	40.4.1.3
Page	40-28
Line	34-35
Comment	This section is not clear. It describes receive once sync has occured. But it is not clear how sync occurs. We can implement something but we are unsure if it will meet the intent of the std.
Response	Withdrawn

ID	56
Commentor	Gladstone
Comment Type	e
Section	40.4.4.2
Page	40-34
Line	33
Comment	There is no pp. 40.6.1.2.6
Response	Accept, will fix

ID	57
Commentor	Gladstone
Comment Type	e
Section	40.6.3.2.3
Page	40-57
Line	13
Comment	bc_rcvr_status s/b loc_rcvr_status
Response	Accept, will fix

ID	58
Commentor	Gladstone
Comment Type	e
Section	40.6.3.3
Page	40-58
Line	11
Comment	Figure 40-20 references the wrong figure
Response	Accept, will fix

ID	59
Commentor	Campbell
Comment Type	tr
Section	40.8.3.2
Page	40-89
Line	6
Comment	Recommend the requirement for ELFEXT loss be relaxed from 19 - 20Log(f/100) to 18 - 20Log(f/100) in order to accommodate 8-pin modular connectors with lower FEXT loss. This implies the PSELFEXT loss will also be reduced.
Response	Accept, resolve with #54

ID	60
Commentor	Dove
Comment Type	tr
Section	40.5.1.3.1
Page	40-44
Line	15
Comment	The variable "Signal_Detect" which is referred to in 40.3.3 and used in the PCS control state machine should be defined here. The variable has values of TRUE or FALSE which indicates whether the received signal amplitude (discounting tranmsitted signal) is above a threshold for a specific amount of time. I intend to have a diagram with specifics for the amplitude and time values to be included.
Response	Accept, resolution pending timer solution

ID	61
Commentor	Dove
Comment Type	tr
Section	40.9.1
Page	40-91
Line	38
Comment	The MDI labeling only accounts for one end of the link. I understand that 1000BT uses full-duplex channels, however, the autonegotiation function requires that you transmit FLPs on a different pair than the one you receive FLPs on. We either have to specify that FLPs will be transmitted onto both the 12 and 36 pairs (and received on both) or we have to specify an MDI-X assignment.
Response	Accept in principle. Default solution will be to add MDX column to table 40-17. Dan Dove to start reflector discussion on possible automated alternative.

ID	62
Commentor	Dove
Comment Type	tr
Section	40.7.1.3.1
Page	40-83
Line	41
Comment	If we want to ensure reliable and robust interoperability between different products, it would be prudent to incorporate a differential noise immunity specification. While 100BASE-T did not do this, other LAN technologies like 10BASE-T do. I will provide a detailed recommendation on test methodology in Dallas.
Response	Accept in principle. Dan Dove to post proposal to the reflector for discussion at the February interim.

ID	63
Commentor	Gladstone
Comment Type	e
Section	40.4.1.2.1
Page	40-16
Line	51
Comment	should read ... PHYC_CONFIG.indicate = SLAVE
Response	reject, ok as is

ID	64
Commentor	Gladstone
Comment Type	e
Section	40.4.1.2.4
Page	40-19
Line	47
Comment	should read ... Sdn[8:0] that represents …
Response	accept, will fix

ID	65
Commentor	Gladstone
Comment Type	e
Section	47.14.7.1
Page	40-111
Line	1
Comment	Table is mis-labeled 100BASE-T2
Response	accept, will fix

ID	66
Commentor	Kelly
Comment Type	e
Section	40.6.3.1.1
Page	40-54
Line	52
Comment	should read ... The default values for bits 9:15:13 are all zero
Response	accept, will fix

ID	67
Commentor	Creigh
Comment Type	e
Section	40.7.1.1.1
Page	40-63
Line	35-52
Comment	Figure 40-16 is a back level version of the figure. This should be replaced with the one I sent Colin.
Response	accept, will change

ID	68
Commentor	Creigh
Comment Type	e
Section	40.7.1.2.3
Page	40-74
Line	1-53
Comment	Figure 40-24 is a back level version of the figure. This should be replaced with the one I sent Colin.
Response	accept will change

ID	69
Commentor	Creigh
Comment Type	tr
Section	40.3
Page	40-14
Line	1-50
Comment	If a PHY takes the transition from SEND IDLE OR DATA or SEND IDLE to SLAVE DFE CONVERGENCE, it will attempt a startup without synchronization with the remote PHY. Given the current state diagram. The remote PHY will simply go to the SEND_IDLE state forever. This should be dixed by forcing synchronization of the two PHYs via the changes to the state diagram shown in the attached figure (figure distributed at January 98 interim.) This requires the definition of a new timer, sync_timer that has a duration of 10 us and further requires that the PHYs detect LOSS of signal within 10 us of receiving continuous SEND_Z from the remote transmitter.
Response	Agree in principle, implementation TBD

ID	70
Commentor	Creigh
Comment Type	tr
Section	40.3
Page	40-14
Line	1-50
Comment	A maxwait timer has been defined in the current draft but is not used. The phy control state diagram should be modified as shownh in the attached figure (see comment 69) to allow the expiration of the maxwait timer to force restart of the convergence process and to ensure that the maxwait timer is restarted whenerer training is restarted. Furthermore I recommend the maxwait timer duration should be 10ms instead of 750ms.
Response	withdrawn

ID	71
Commentor	Creigh
Comment Type	tr
Section	40.3
Page	40-14
Line	1-50
Comment	The current phy control descriptioon does not allow the PHY to properly handle failure conditions such as disconnection of the cabling. Currently there is no mweans to tell autonegotiation that the link has failed since there is no path out of the convergence/normal operation loop leading to link_status<=FAIL. The current PHY control is inconsistent with the linhk monitor state diagram of Figure 40-13 as well which only allows link failure upon detection of loc-rcvr_status not ok and no retries of the convergence. The phy control state diagram should be modified as shown in the attached figure (see comment 69) to include a path to link_status <=FAIL after the PHY has failed to converge after a number of attempts. Additionally, the link monitor state diagram of Figure 40-13 should be removed and any editorial changes to the text made as needed since the phy control now shows link monitor behavior. This requires the definition of an attempt counter with a limit of MaxAtempts (recommended set to 5 attempts.)
Response	withdrawn

ID	72
Commentor	Castellano
Comment Type	e
Section	40.6.2
Page	
Line	47
Comment	The serial management interface is not called the GMII (which stands for Gigabit Media Independent Interfaces.) It is called the "MII Management Interface" and is defined in section 22.2.4. The interface does not change for gigabit PHYs, only the register content changes. PROPOSED RESOLUTION: Replace the sentence on line 47 with "This interface is referred to as the MII Management Interface, and is defined in 22.2.4."
Response	Accept, will fix

ID	73
Commentor	Castellano
Comment Type	e
Section	40.6.3.1.3
Page	40-55
Line	15
Comment	It is no clear from the text how the result of the automatic master/slave configuration is reported. PROPOSED RESOLUTION: Define a status bit for result of master/slave configuration resolution. I believe the status register.) If this is the intent, I propose replacint 40.6.3.1.3 with the following text: 40.6.3.1.3 MASTER-SLAVE Configuration Value "When to manually configure the PHY as MASTER or SLAVE. Setting bit 9.11 to logical zero configures the PHY as SLAVE. When MASTER-SLAVE result of automatic MASTER_SLAVE configuration for the local PHY. When auto-negotiation has completed, bit 9.11 shall be logical zero when the PHY has been configured as SLAVE."
	Accept in principal, changes to Auto-Negotiation will be discussed at the February Interim.

ID	
Commentor	Thompson
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Section	
	40-9,10
Line	
	It appears from this text that there are two line codes, one providing 6dB, the other 3dB. Options in a standard are an area of concern. Please explain
Response	Accept in principle, resolution in process.