QUASI-CONSTANT POWER DISSIPATION IN THE PSE SWITCH MOSFET

Power Dissipation During Startup For Constant Current vs. Ramped Current

- Describe two alternative current limit vs. load voltage schemes
- Show simulation results
- Summarize findings / Get feedback from group

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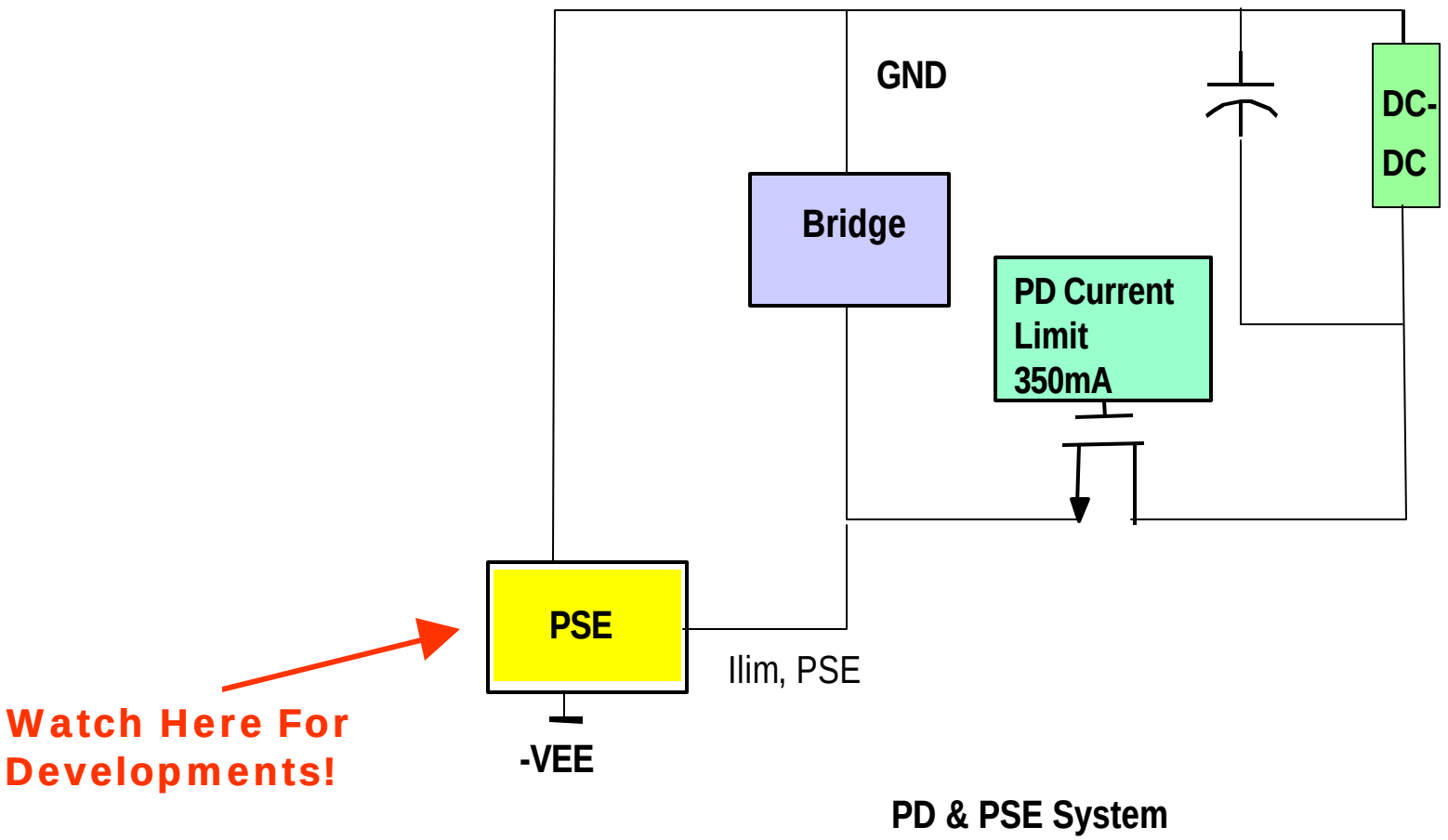
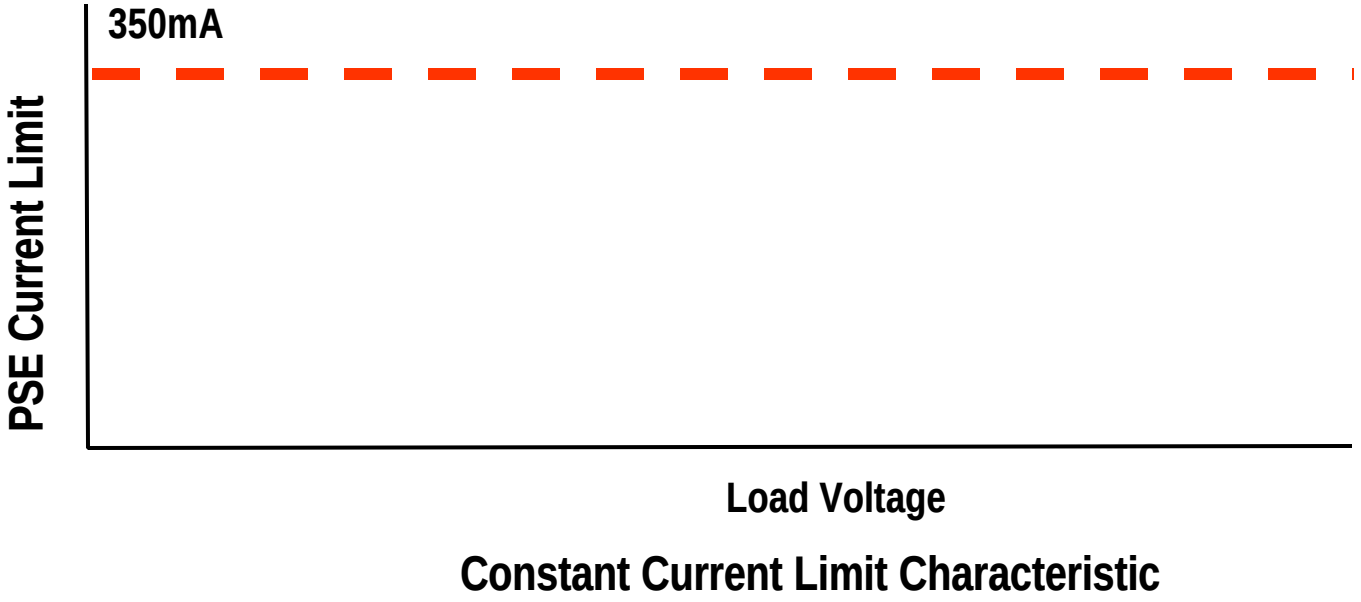
Two alternative PSE I_{LIMIT} vs. PD voltage characteristics



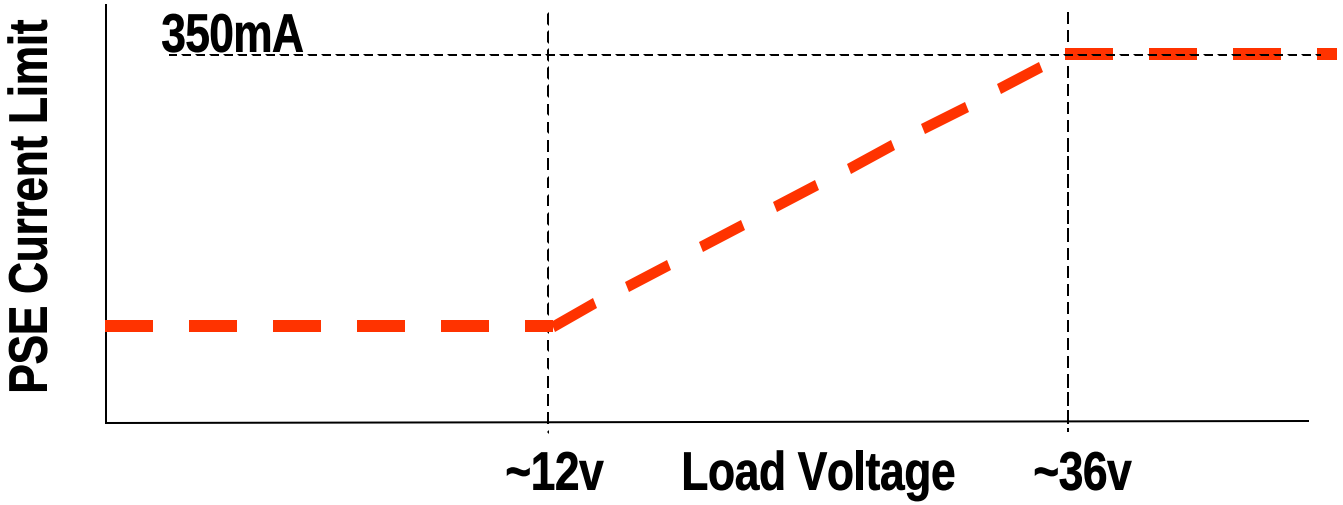
Constant PSE Current Limit During PD Charge-Up



Constant Current Limit Characteristic

- **Current limit constant over load voltage**
  - **PD capacitance charges slightly faster**
  - **Greater thermal stress on PSE power device**

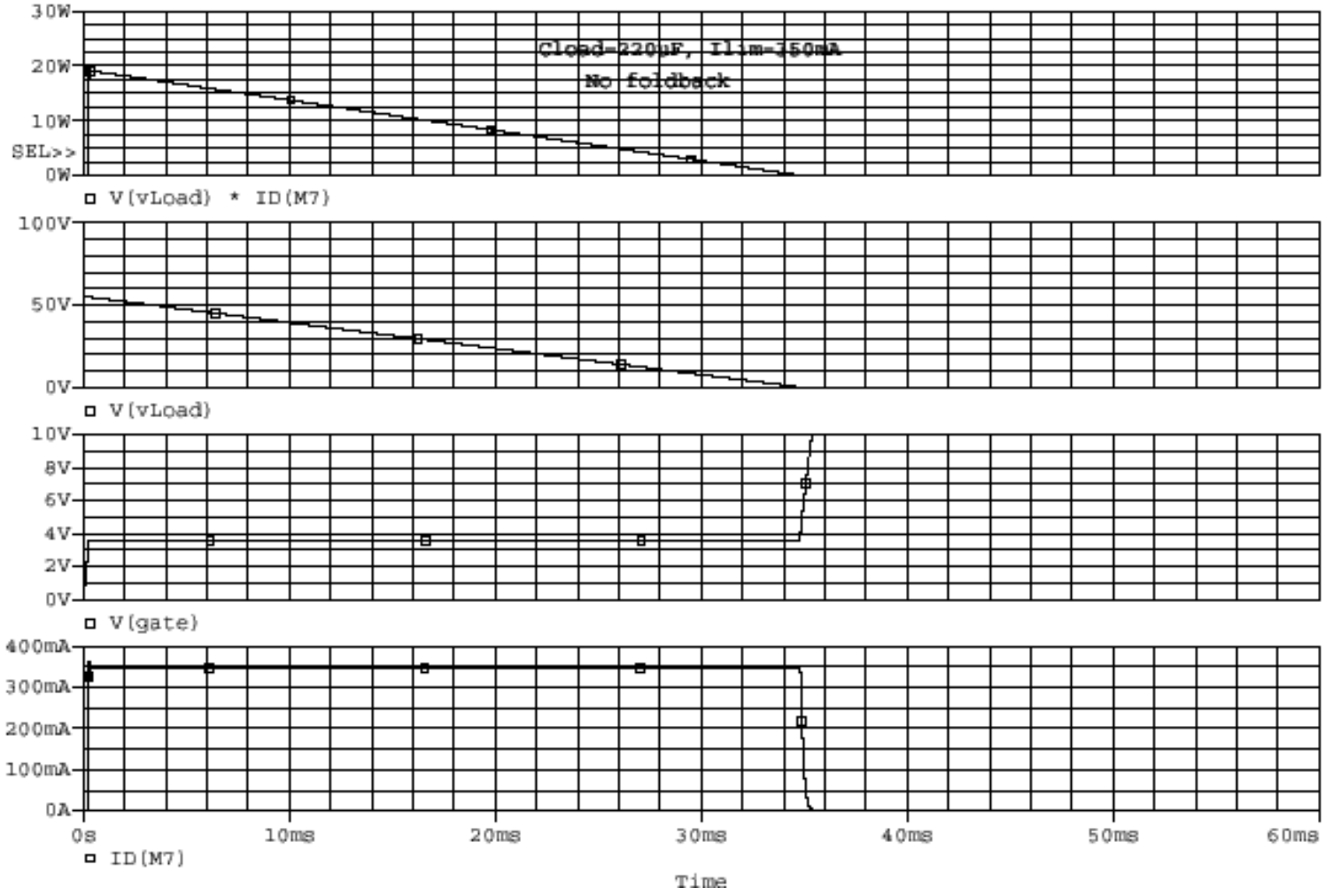
Ramped or "Foldback" Current Limit



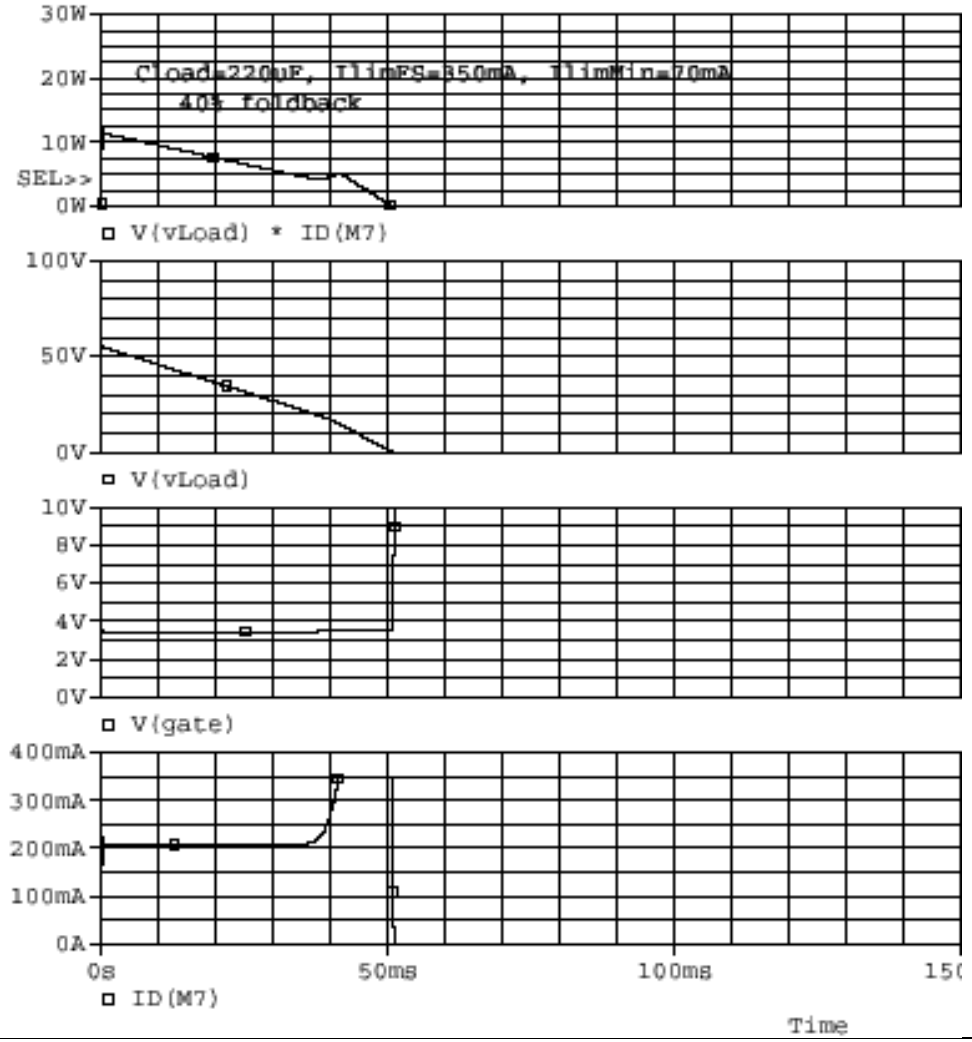
Ramped or Foldback Limit Characteristic

- **Current limit rises to full level as load voltage rises to final value.**
  - **Reduces power dissipation in PSE power device**
  - **Slightly increases time for PD voltage to achieve final value**

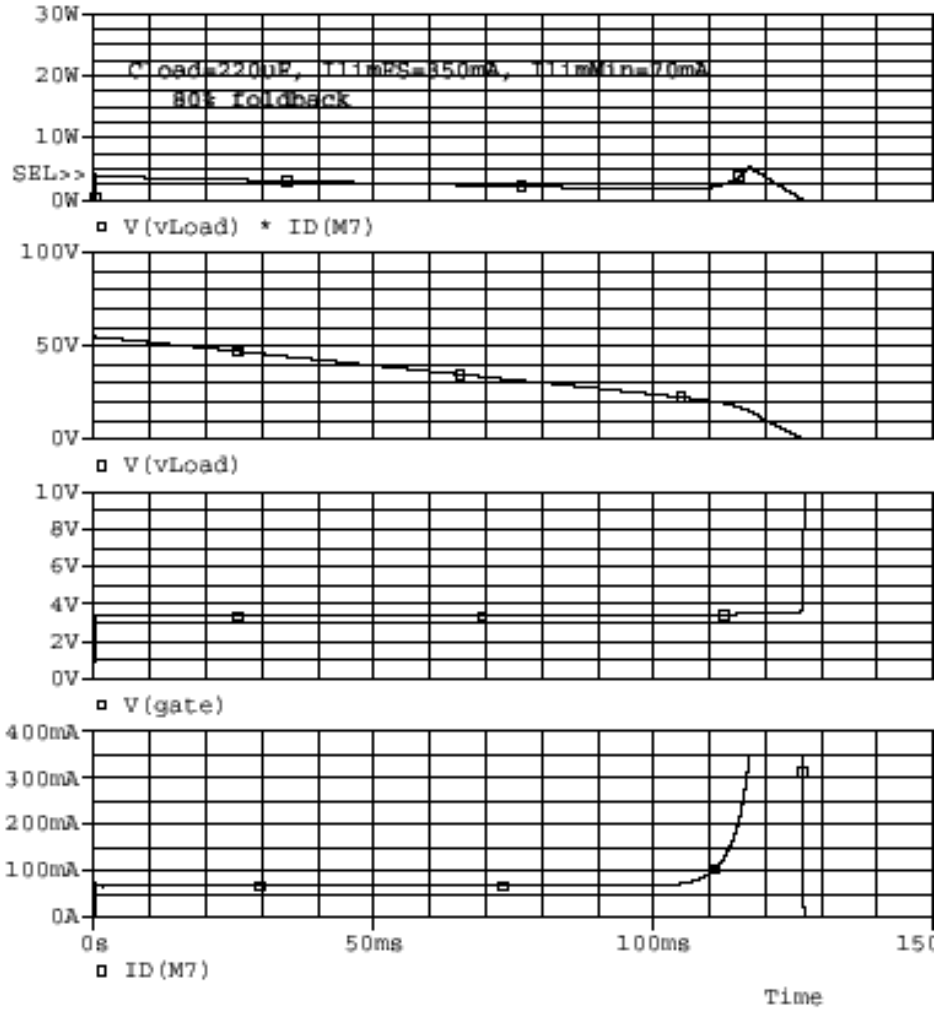
C_{PD} = 220µF, No PSE Foldback



C_{PD} = 220µF, 40% PSE Foldback



C_{PD} = 220µF, 80% PSE Foldback



Summary

Foldback current limit

- lowers power dissipation
- slightly extends startup time
- lowers thermal stress on PSE

- Suppose thetaJA is 30°C/W
- Thermal time constant of PSE power device of ~125mS
- How much temp rise occurs during startup?

Under foldback, average power is 3W for 120mS

so temp rise = (1-1/e)*3*30 = .63*3*30 = 54°C

Under constant current, average power is 10W

so temp rise = 10*0.3*30 = 90°C

Summary

Foldback current limit

- allows smaller power device in PSE
- lowers power dissipation
- lengthens startup time

Question:

Even if there is no need to require PSE switch foldback limiting, is there any desire to forbid it?