Power Turn-On

IEEE 802.3af DTE Power via MDI

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Dieter Knollman
AVAYA
djhk@netzero.net

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Outline

- Simulate Power in PSE and PD Switches
  - Switch Junction Temperature
- Examine PSE Current Limiting
  - Options to Reduce Switch Stress
- Examine PD Current Limiting
  - Options to Reduce Switch Stress
- Propose Low Power Solution

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Switch Power Dissipation

- Energy = Voltage * Current * Time
- Voltage – Initial Voltage
- Current – Limit Value
- Time – Charge Capacitor

- Power = V * I = 57V * 0.7 A = 40 watts
- E = 57V * 0.7 A * 0.1 sec = 4 joules

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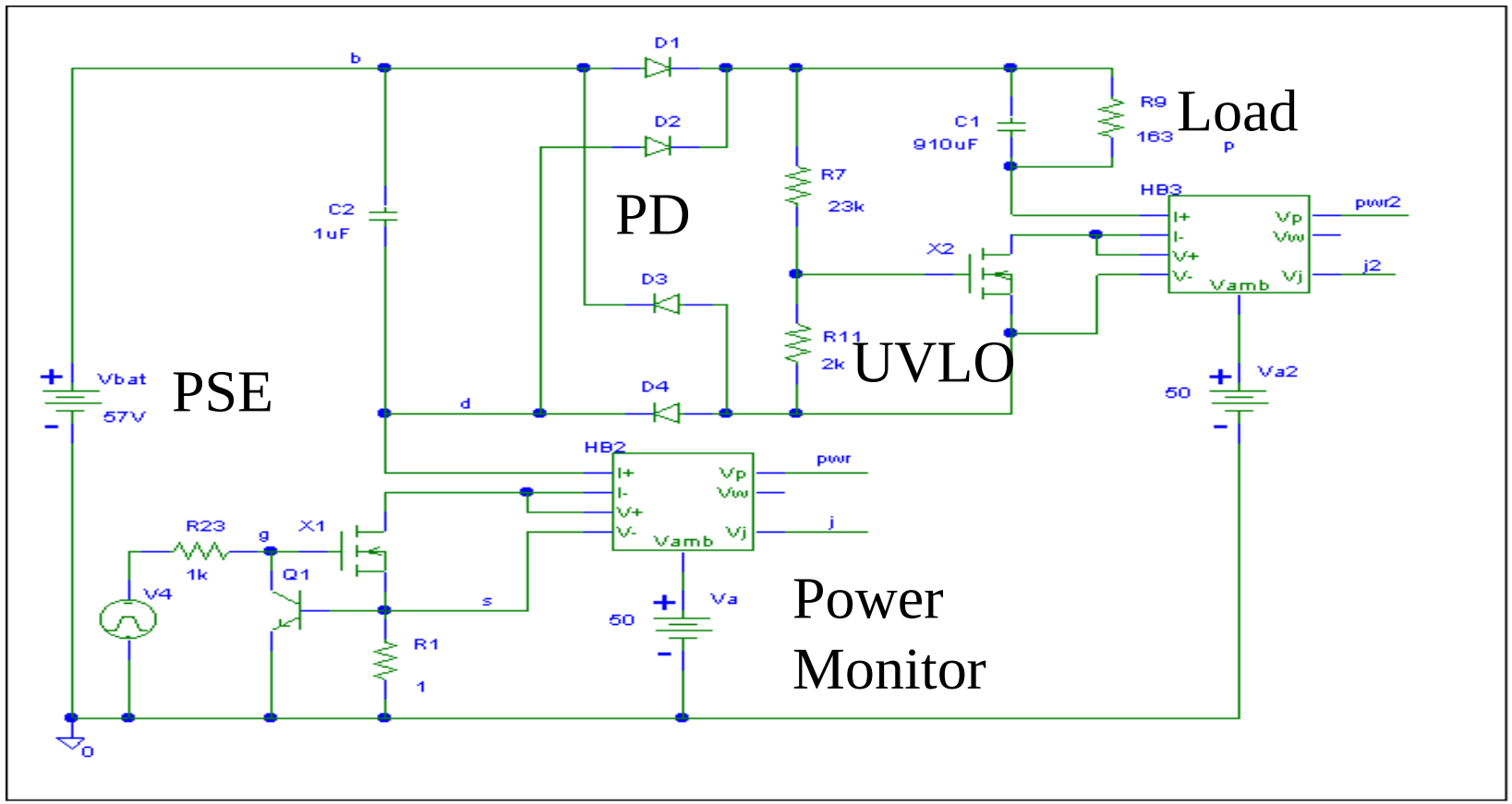
Current Limit Requirements

- PSE Current Limit– required
  - Protect PSE Interface
  - Protect Cabling
  - May need Fuse, PTC, limited Source
- PD Current Limit - optional
  - Desirable to Limit Input Capacitor Current

Start Up Sequence

- Detection Successful
- PSE Turns Power ON
- Line Capacitor charges
- PD Turns ON – then choice of:
  - PSE limits current
  - PD limits current
- PD Converter Turns ON

PSE Current Limit Test Circuit



Test Circuit

- MOSFETS for PSE and PD
- Simple Transistor current limit circuit
- Simple UVLO circuit
- Power Monitor Blocks
- Line Capacitance = 1UF
- PD load Capacitance = 910uF
- Supply Voltage = 57 volts

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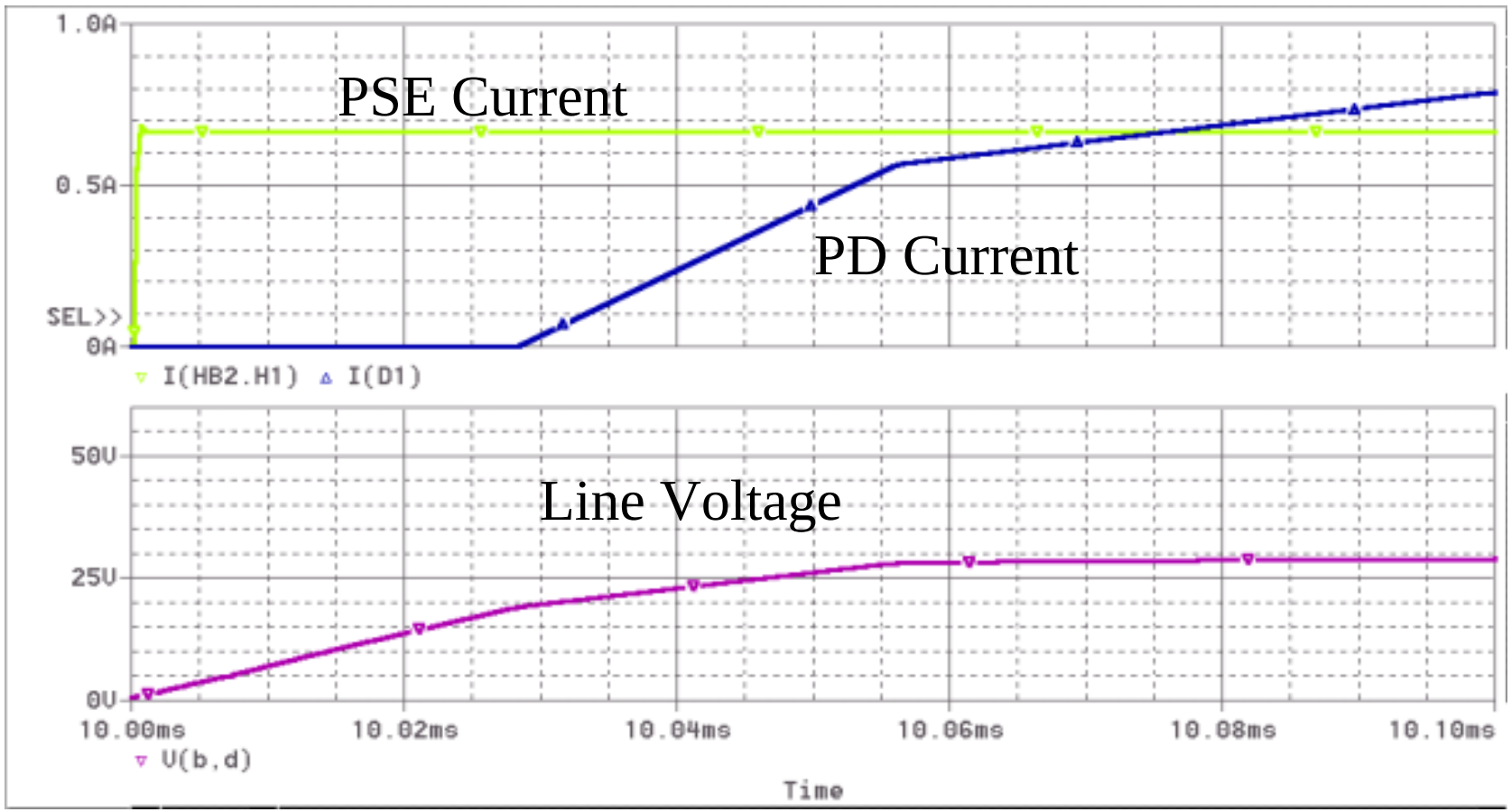
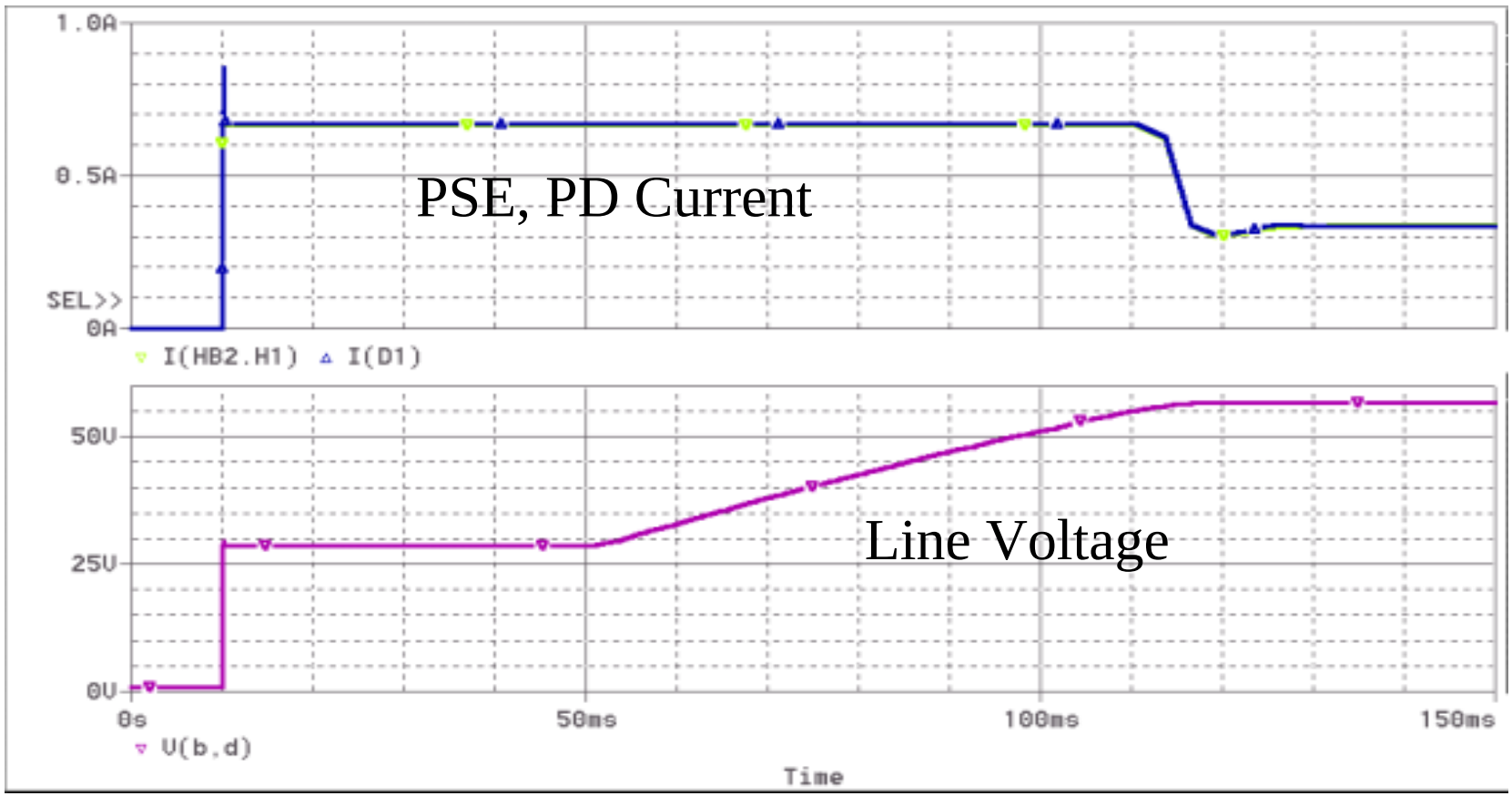
First 100 uS


1.0A
0.5A
SEL>>
0A
PSE Current
PD Current
I(HB2.H1)
I(D1)
50U
25U
0U
Line Voltage
10.00ms
10.02ms
10.04ms
10.06ms
10.08ms
10.10ms
V(b,d)
Time

Initial Time

- PSE Switch Turn On
  - limited by 1K source impedance
- PSE goes into current limit
- Line Capacitor charges to PD UVLO
  - Time about 25us
- PD turns ON

PSE Current Limiting
Start Up Line Voltage, Current



Start Up – PSE Current Limit

- Power Supply Voltage
  - Split between PSE and PD
- PSE Switch Voltage
  - Battery voltage – PDon Voltage
  - Decreases after PD Cap Voltage > PDon Voltage
- PD Switch Voltage
  - PDon Voltage – PD Cap Voltage
  - Decreases after PD Cap Voltage > PDon Voltage
- **Power Dissipation in PSE and PD Switches**

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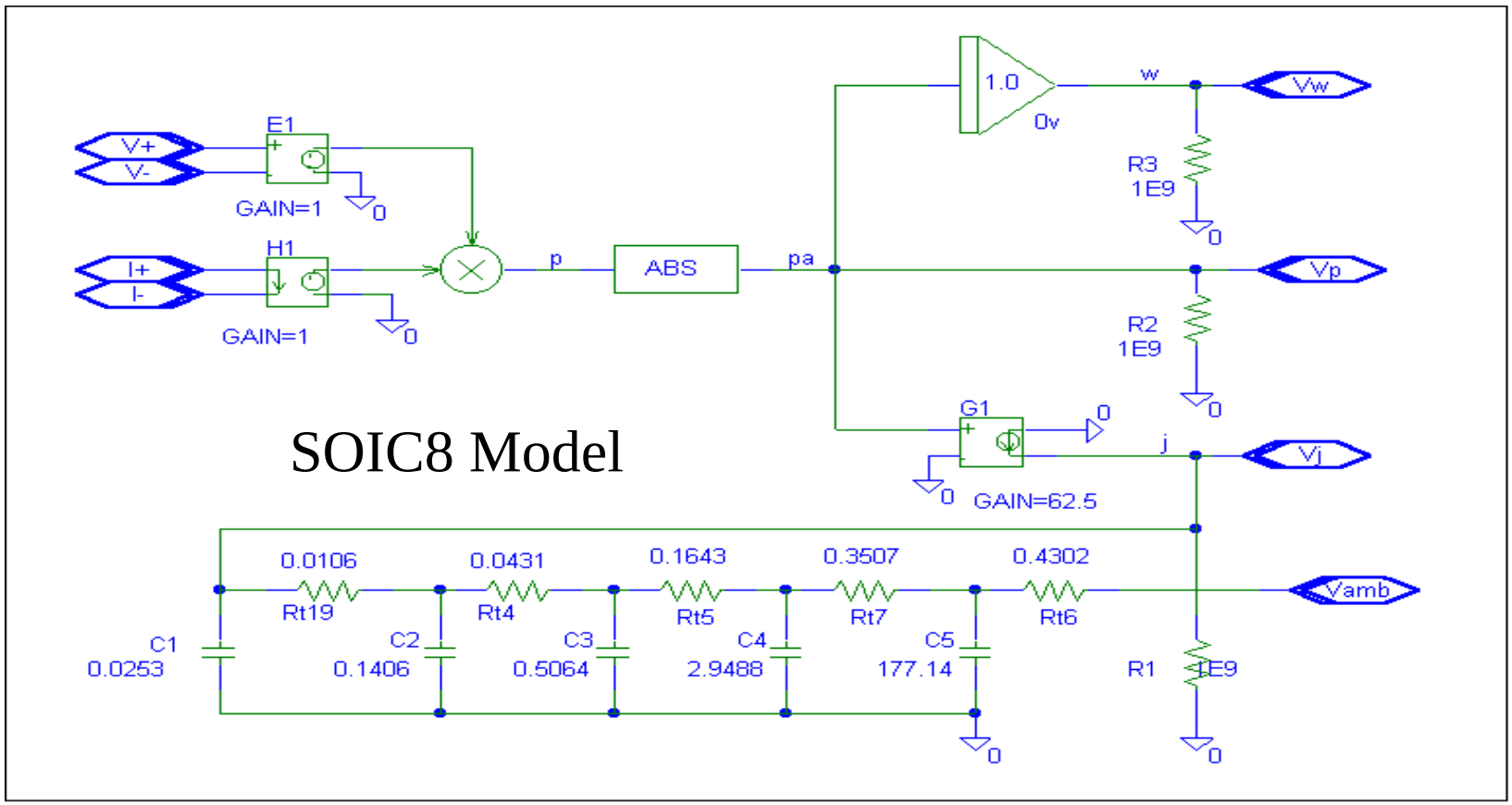
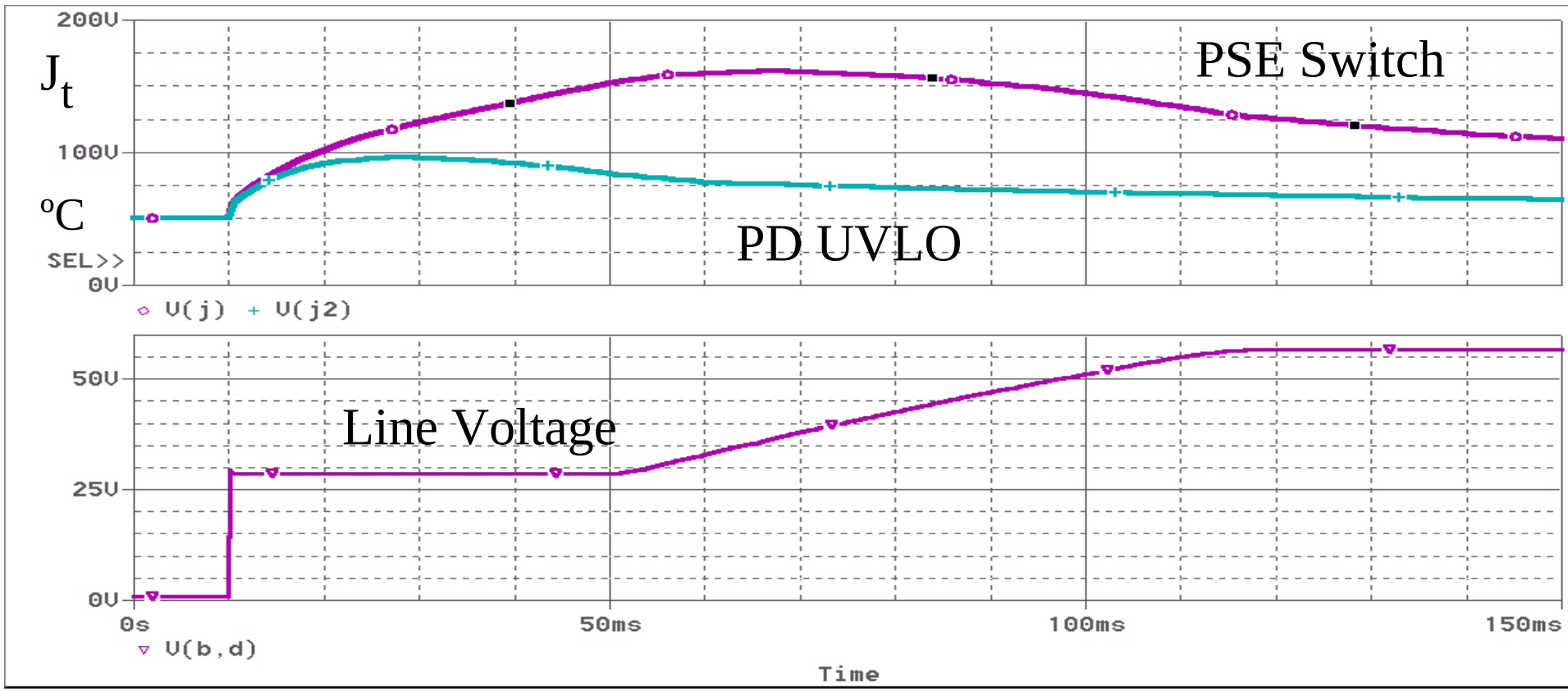
Thermal Monitor Schematic



Thermal Model

- E & H source monitor V and I
- P = ABS (V * I)
  - ABS allows reverse connections
- Power is transformed to I by G1
- I drives thermal resistance model
  - SOIC8 Package
- Ambient temperature is added by Vamb

Switch Junction Temperature
PSE Current Limit



PSE Current Limit
Power Dissipation

- PSE Switch Initial Power
  - P = (57V – 30V) * 0.65A = 17.5 Watts
  - Constant for First 50ms
- PD UVLO Initial Power
  - P = 30V * 0.65A = 19.5 Watts
  - Decreases as Cap Charges
- PSE Switch has biggest stress

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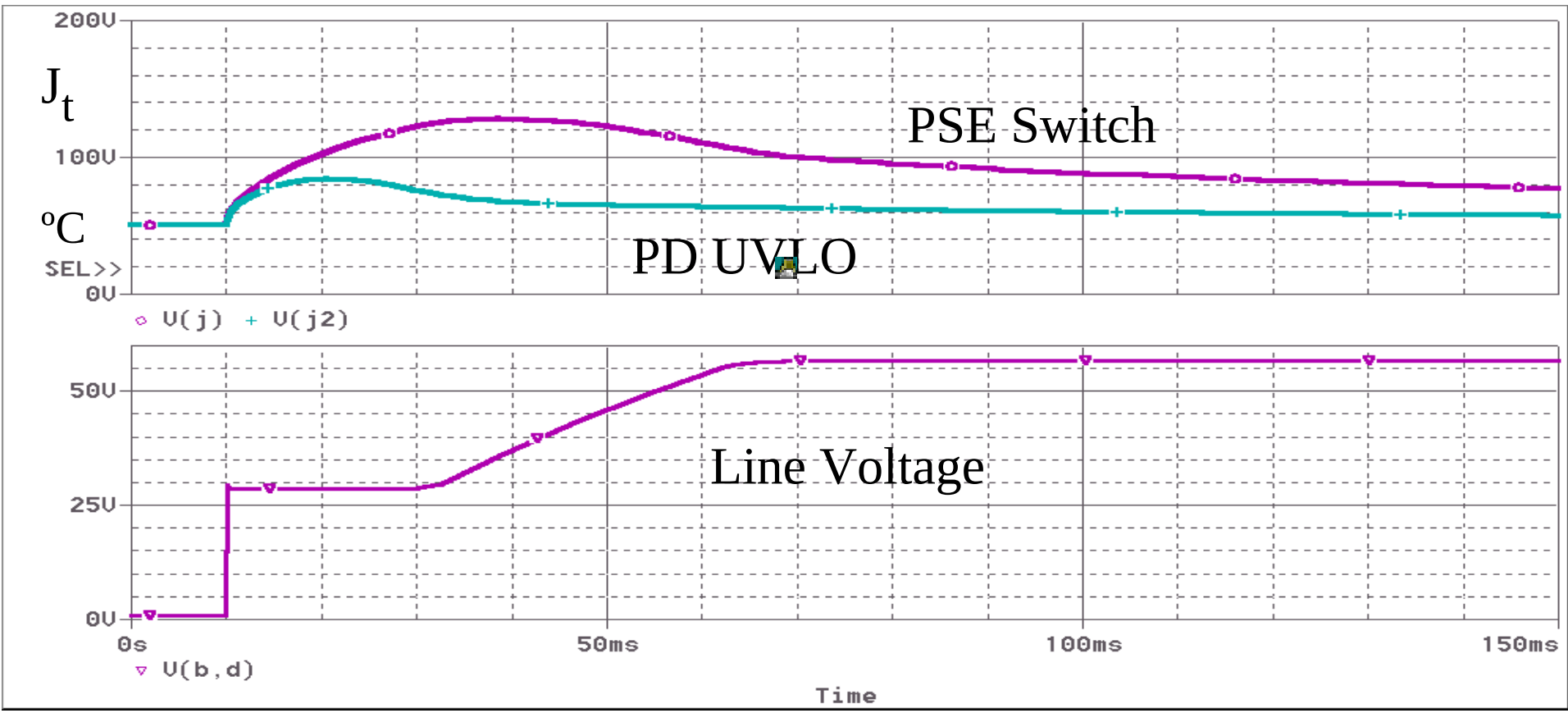
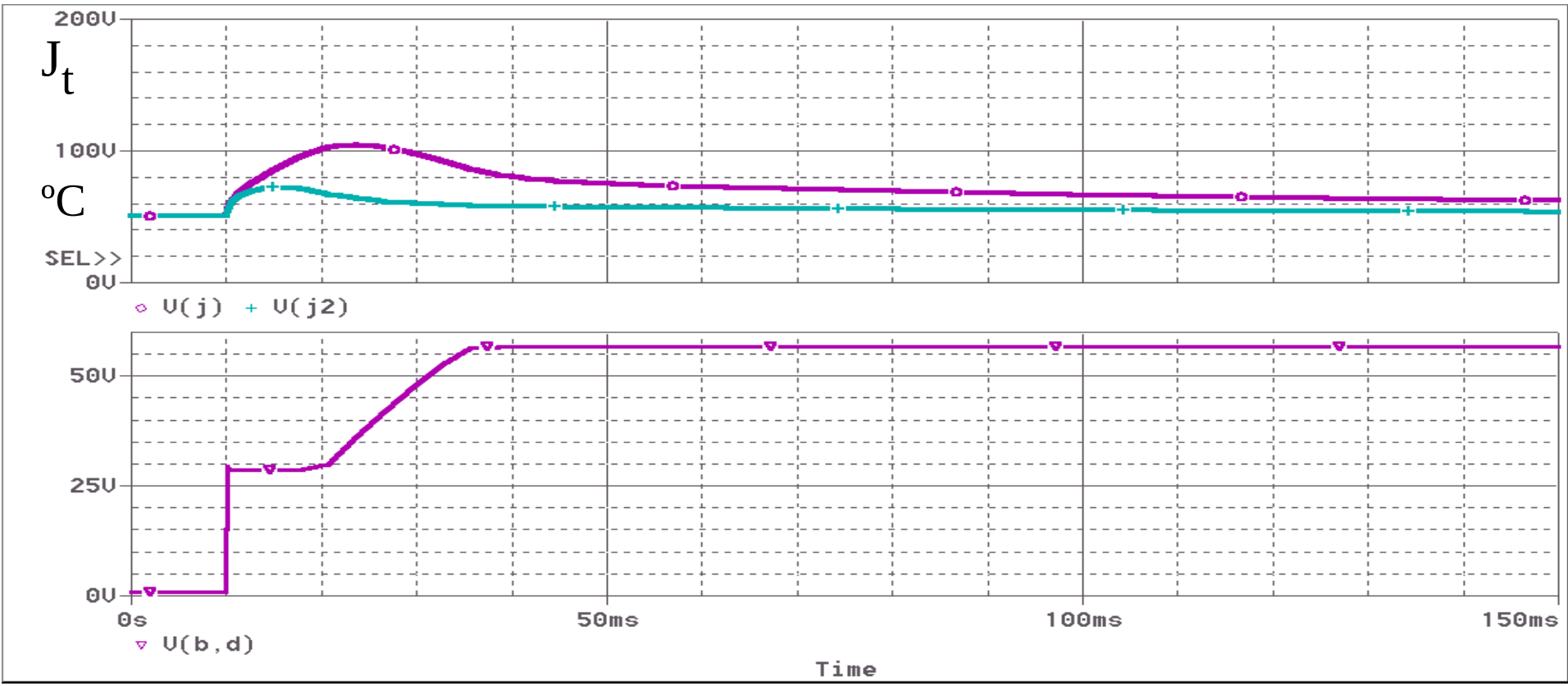
PSE Current Limit Options

- PSE Switch Dissipation
  - Primarily dependent on PD cap charge time
- Reduce PD Capacitance
- Other Options – Not Viable
  - Increase PD UVLO voltage
  - Decrease Current

PSE Current Limit
470uF PD Cap



PSE Current Limit
220uF PD Cap



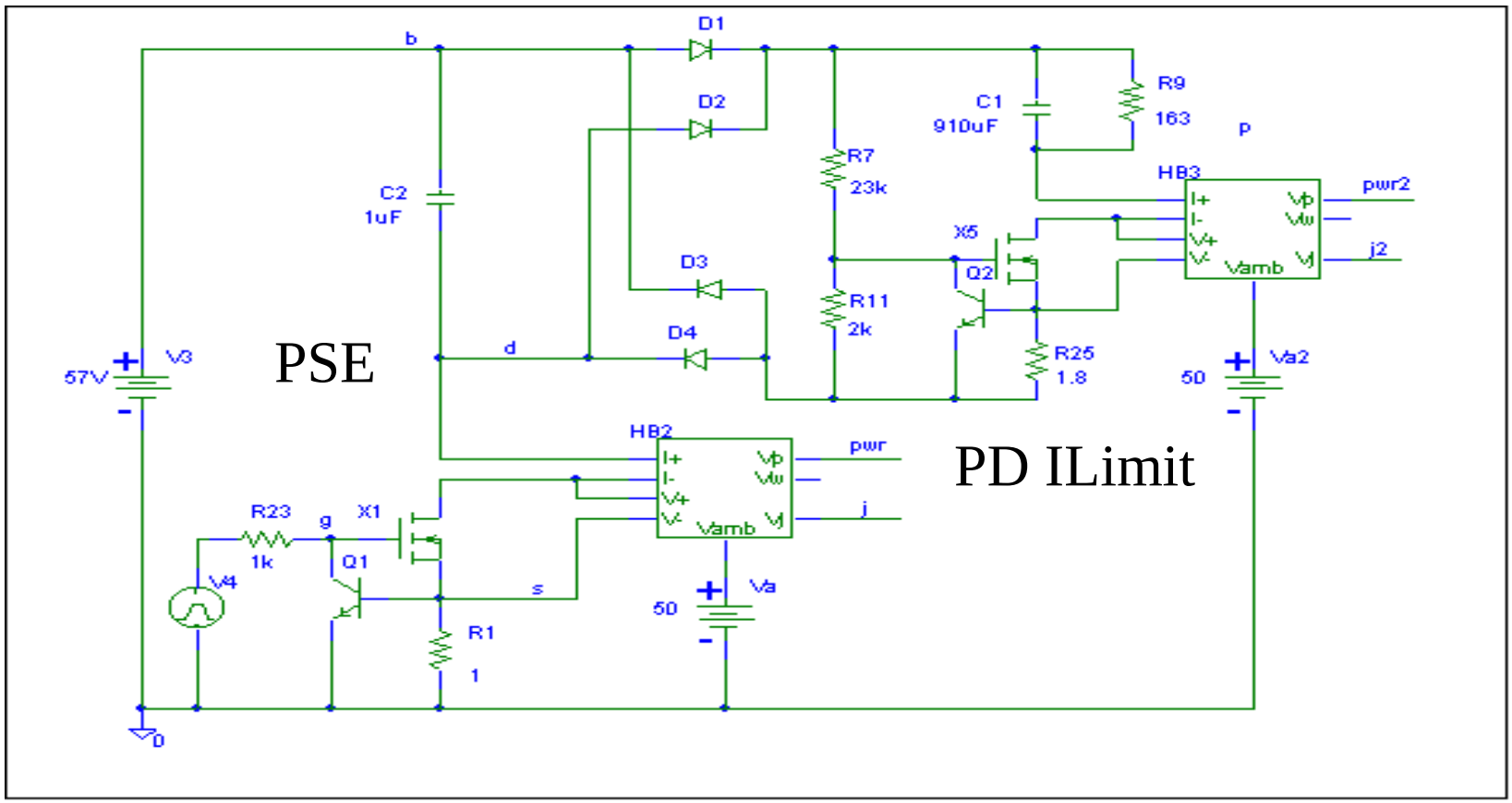
PSE Current Limit Summary

- Stress in PSE and PD Switches
- Requires a Time limit
  - Requires a limit on PD Capacitance

PD Current Limiting

- PD Current Limit < PSE Current Limit
  - PD Current Limit > Minimum Current
- Line Voltage Ramps to Supply Voltage
- Short PSE Current Limit Time
  - to charge Line Capacitance

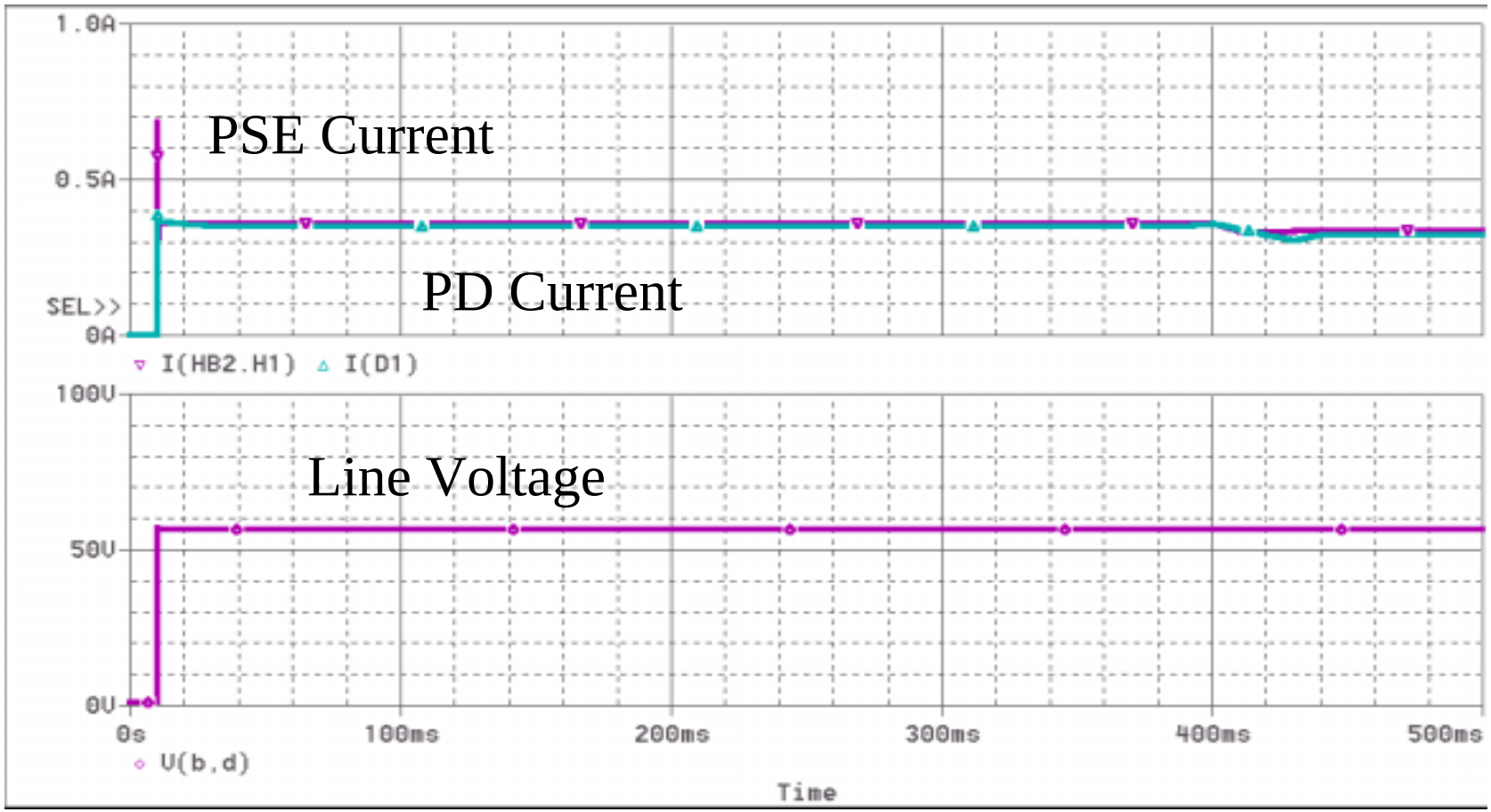
PD Current Limit Test Circuit



PD Current Limit Test Circuit

- Simple Transistor Circuit Added
- R25 sets current limit to Vbe / R25
- C1 – PD Converter Input Capacitance
- R9 – Converter Load

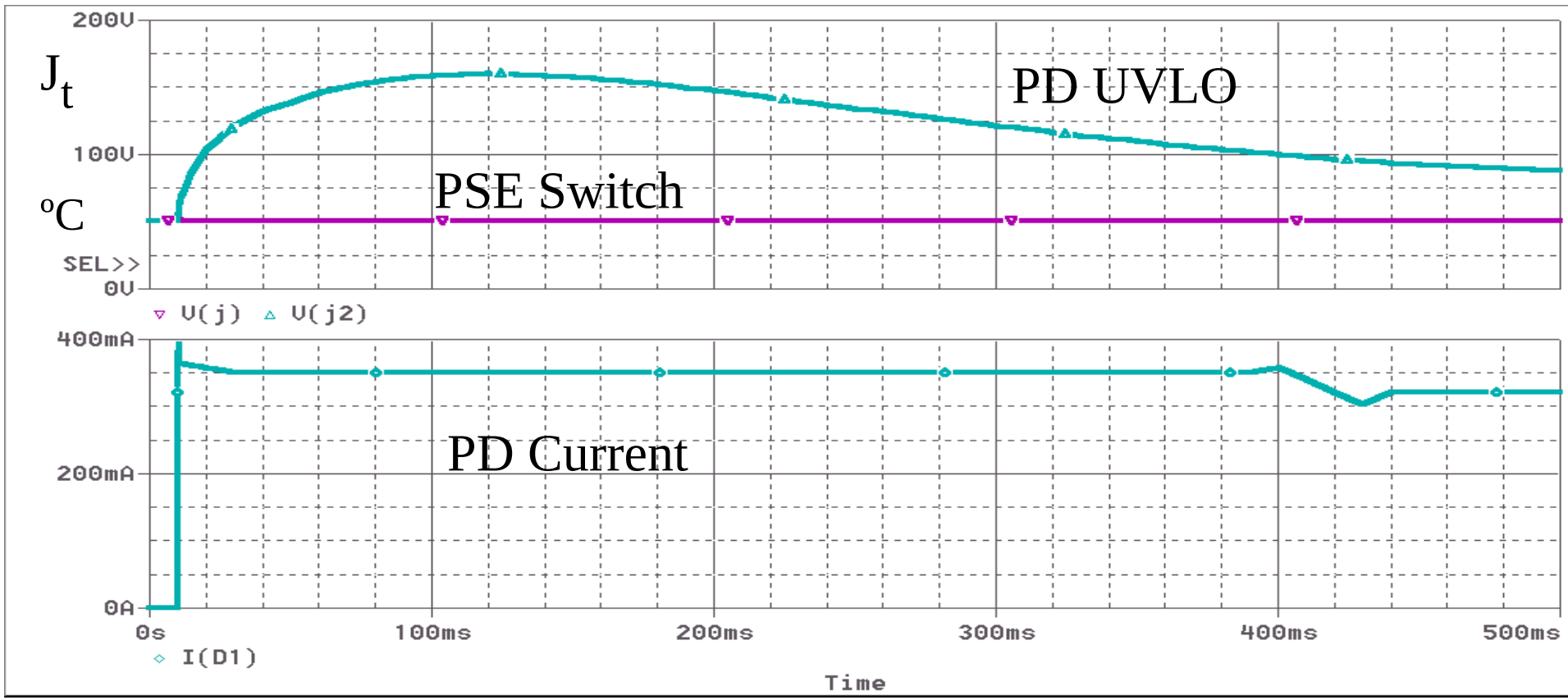
PD Current Limiting



Start Up – PD Current Limit

- Power Supply Voltage
  - Across PD Switch
- PSE Switch Voltage - Zero
  - Current Limit While Line Cap Charges
- PD Switch Voltage
  - Power Supply Voltage – PD Cap Voltage
- Longer Charge Time

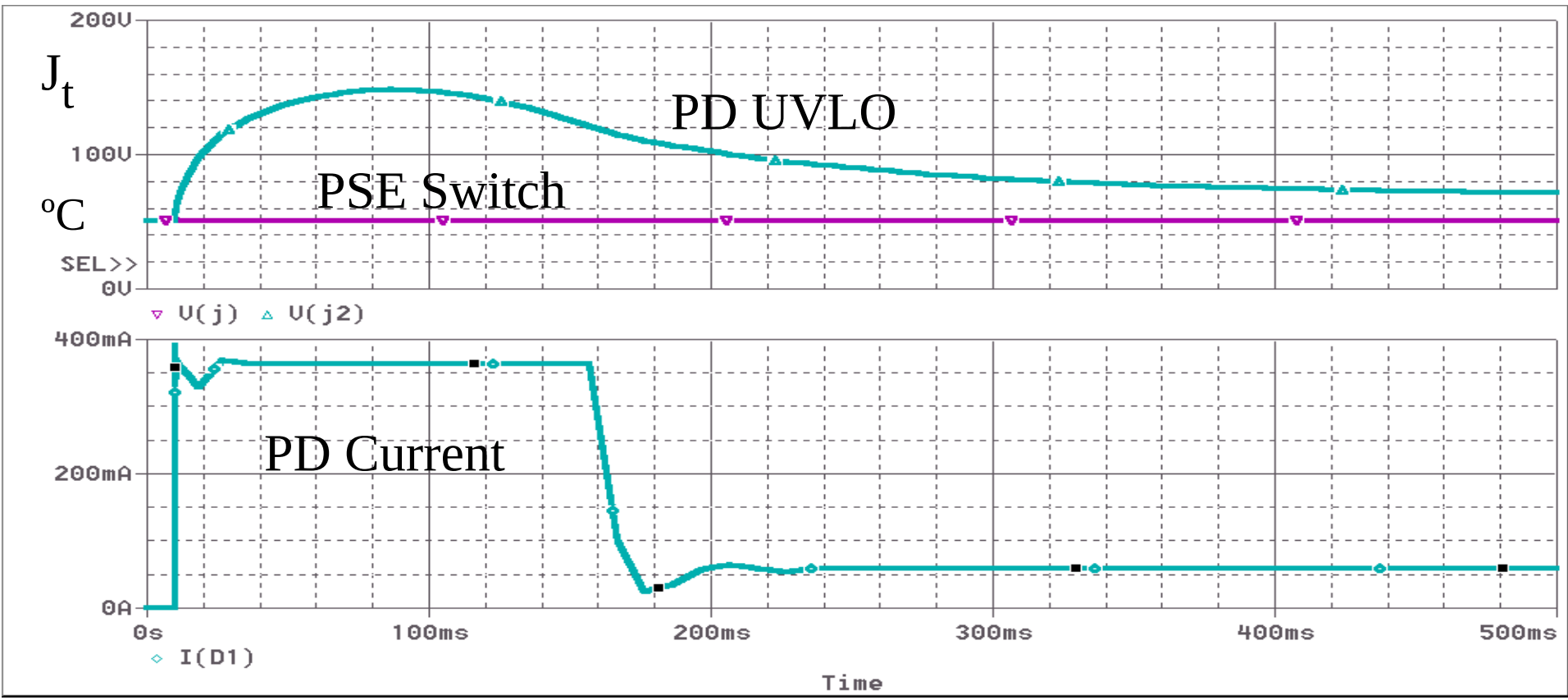
Switch Junction Temperature
PD Current Limit



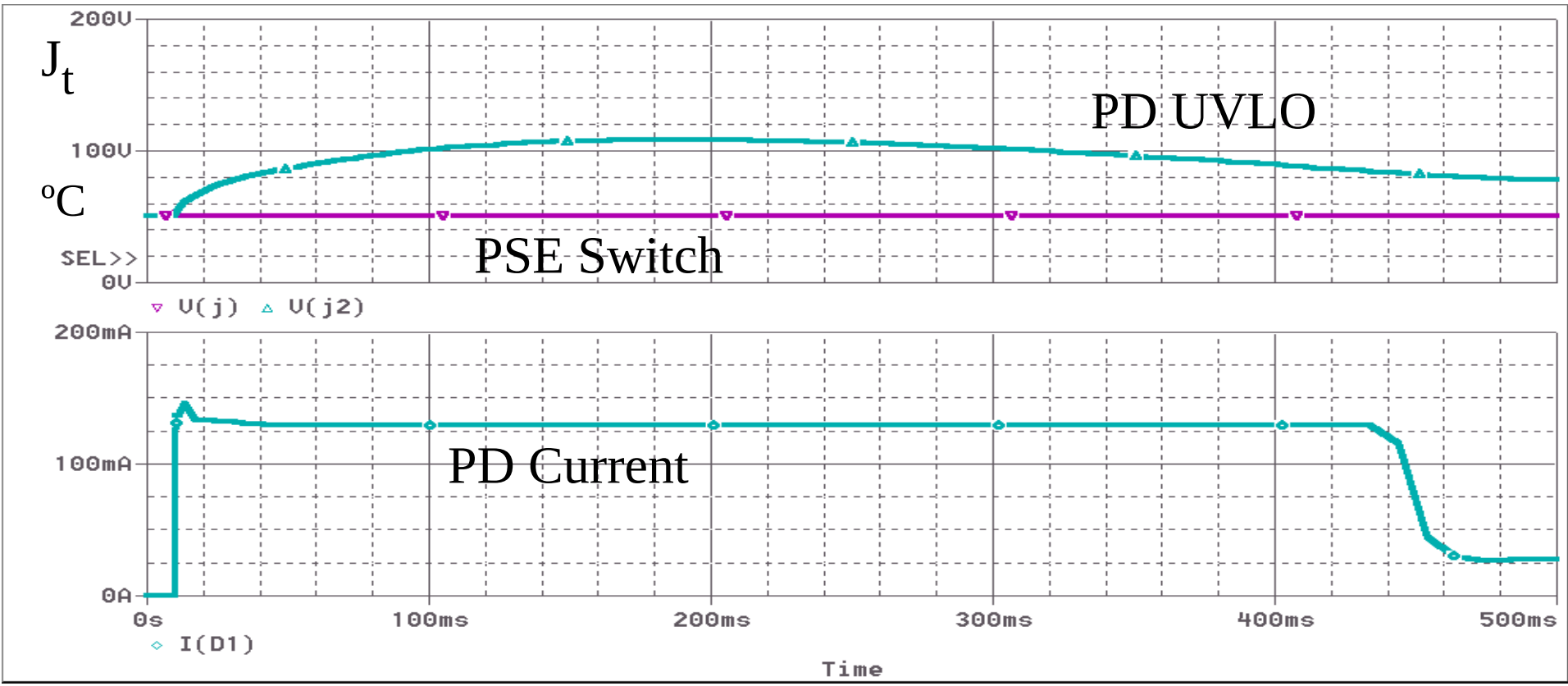
PD Switch

- Supply Voltage across PD Switch
  - Current Charges Capacitor and Load Current
- Temperature Reduced by:
  - Delay Load Turn On
  - Reduce Current Limit

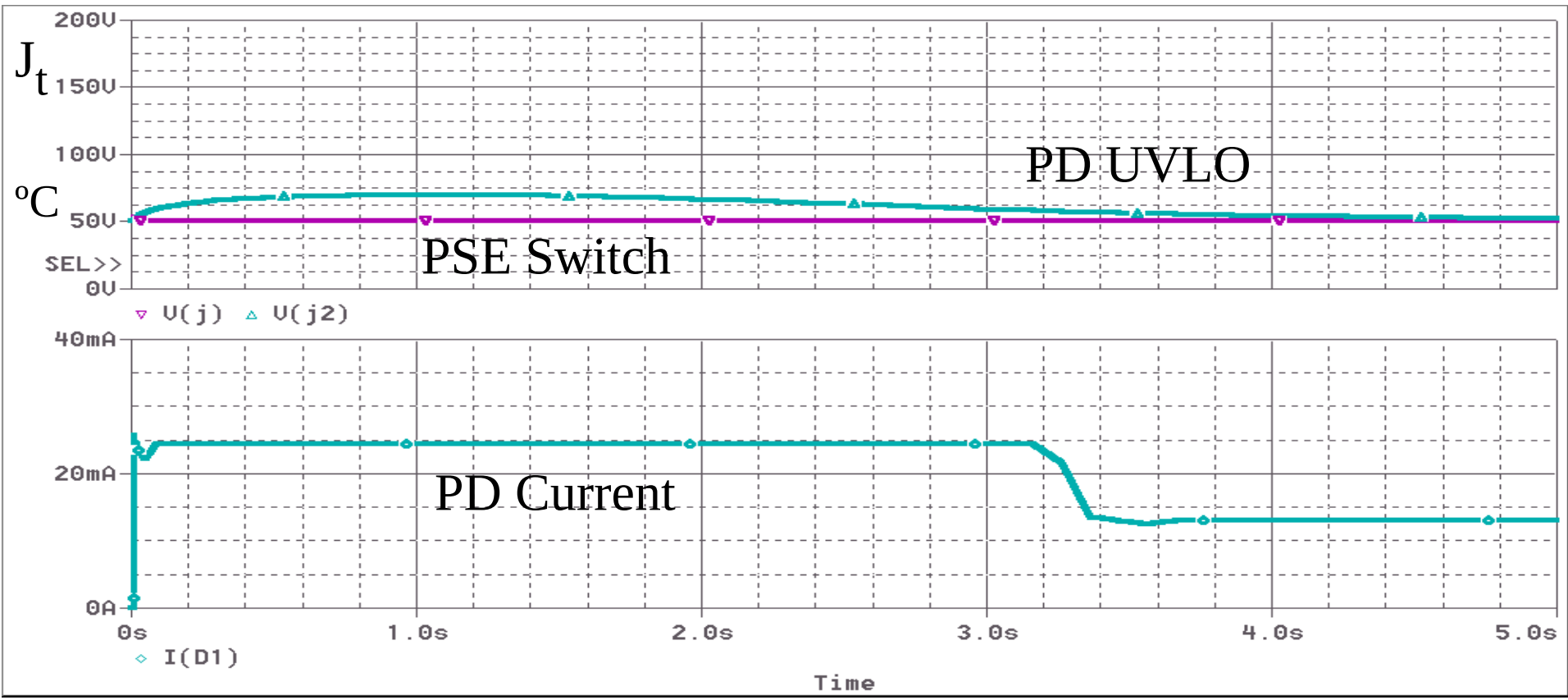
PD Current Limit
Delayed Load



120ma PD Limit



30ma PD Limit



PD Current Limit Summary

- Low PSE Switch Stress
- PD UVLO Stress
  - Function of Current Limit
- Tradeoff between Start Up Time & Stress

Current Limit Comparison

- PSE Current Limiting requires
  - Maximum PD Capacitance
  - Maximum Overload Time
- PD Current Limiting
  - Low PSE Dissipation
  - Charge Cap, Then Turn Load
  - Low Initial Current Limit

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Require PD Current Limiting

- Minimum PSE Switch Stress
  - Allow Fast PSE Switch Trip Time
- Flexible PD Implementation
  - Trade off between PD Stress and Start Time
- Allows Integration in PSE and PD
- Lowest Cost
  - More PSE's than PDs

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