IEEE 802.3af DTE Power via MDI

Can Electronic Components Survive the High Voltages Associated with Safety and ESD Immunity Tests?

Proposal By PowerDsine: Avinoam Levy - avinoaml@powerdsineusa.com

Rick Frosch - rickf@powerdsineusa.com

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YES!!!

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High Voltage Related Safety Standards Requirements EN60950, UL1950

- 3KVrms dielectric strength test, from AC input to RJ-45
- 500Vrms dielectric strength test, output to chassis
- Tests performed when unit is not operating
- These are standard requirements for off-line of the shelf power-supplies.
- Meeting these requirements will not impose real stress on the outputs of the PSE.

High Voltage Related ESD Standard Requirements IEC-61000-4-2

- Up to 15KV charged on a human body simulated network - capacitor in series to resistor.
- The standard provides guidelines to select the appropriate class and hence the voltage level.
- Pass criteria - defined by user, typically we design the equipment to survive with no performance degradation.

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Examples of Silicon Components Used in Similar Conditions and Applications

- SLIC Ic's (Subscriber Line Interface Card)
- Telephone Ring Generators
- Solid state relays used in telephony circuits
- Phone Ic's.
- Many more

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Protection Circuits

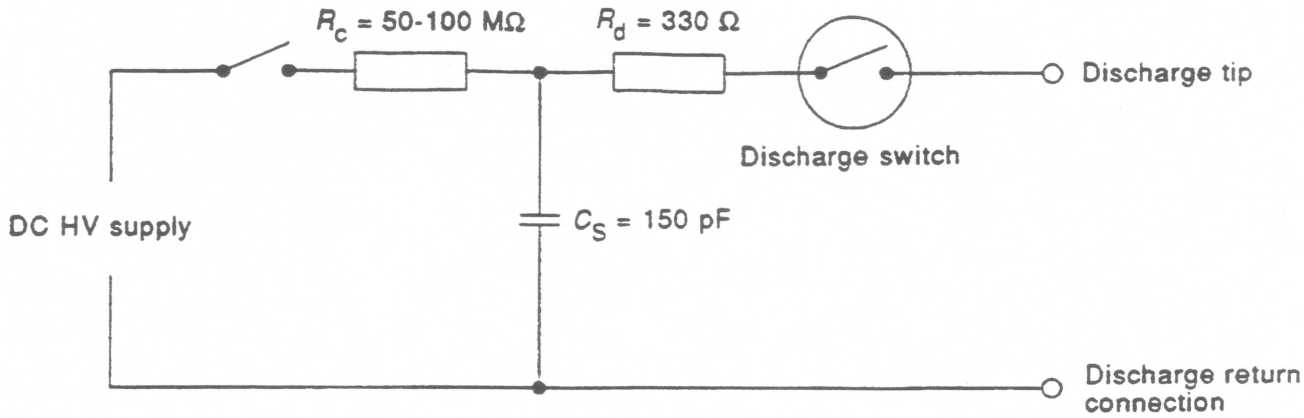
Typically, components such as: Spark Gaps, Surge Arrestors, Transorbs and others are used in telephony circuits.

That will not be the case in our situation!

The Data Communication network is in much more benign conditions so the requirements are less severe.

What are the Standard Requirements

ESD Generator



NOTE – C_d, omitted in the figure, is a distributed capacitance which exists between the generator and the EUT, GRP, and coupling planes. Because the capacitance is distributed over the whole of the generator, it is not possible to show this in the circuit.

Figure 1 – Simplified diagram of the ESD generator

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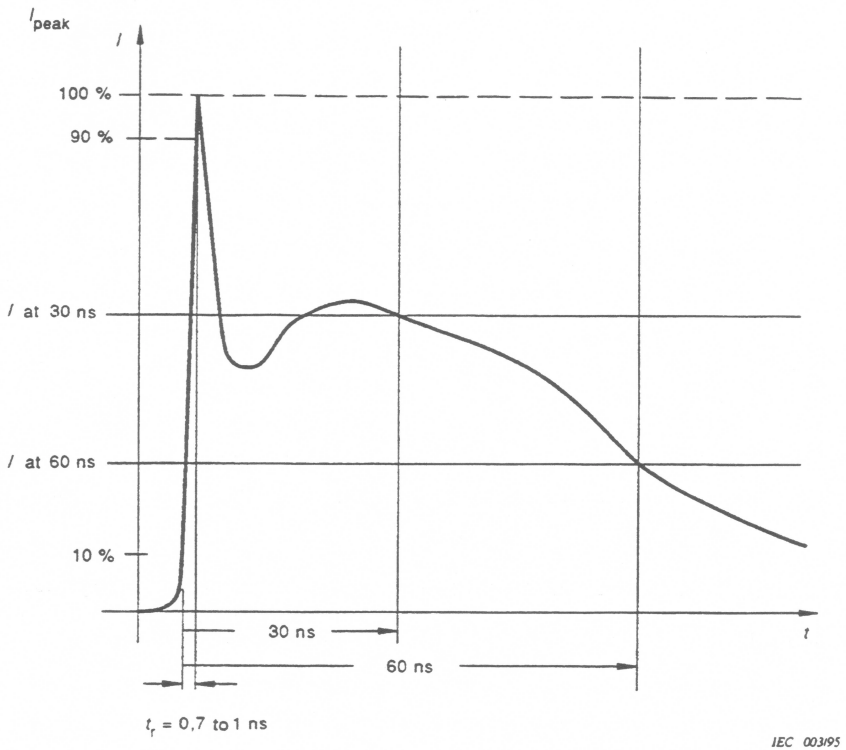
Voltage Levels

Table A.1 – Guideline for the selection of the test levels

Class	Relative humidity as low as %	Antistatic material	Synthetic material	Maximum voltage kV
1	35	x		2
2	10	x		4
3	50		x	8
4	10		x	15

The installation and environmental classes recommended are related to the test levels outlined in clause 5 of this standard.

Pulse Current Shape



Values are given in table 2.

Figure 3 – Typical waveform of the output current of the ESD generator

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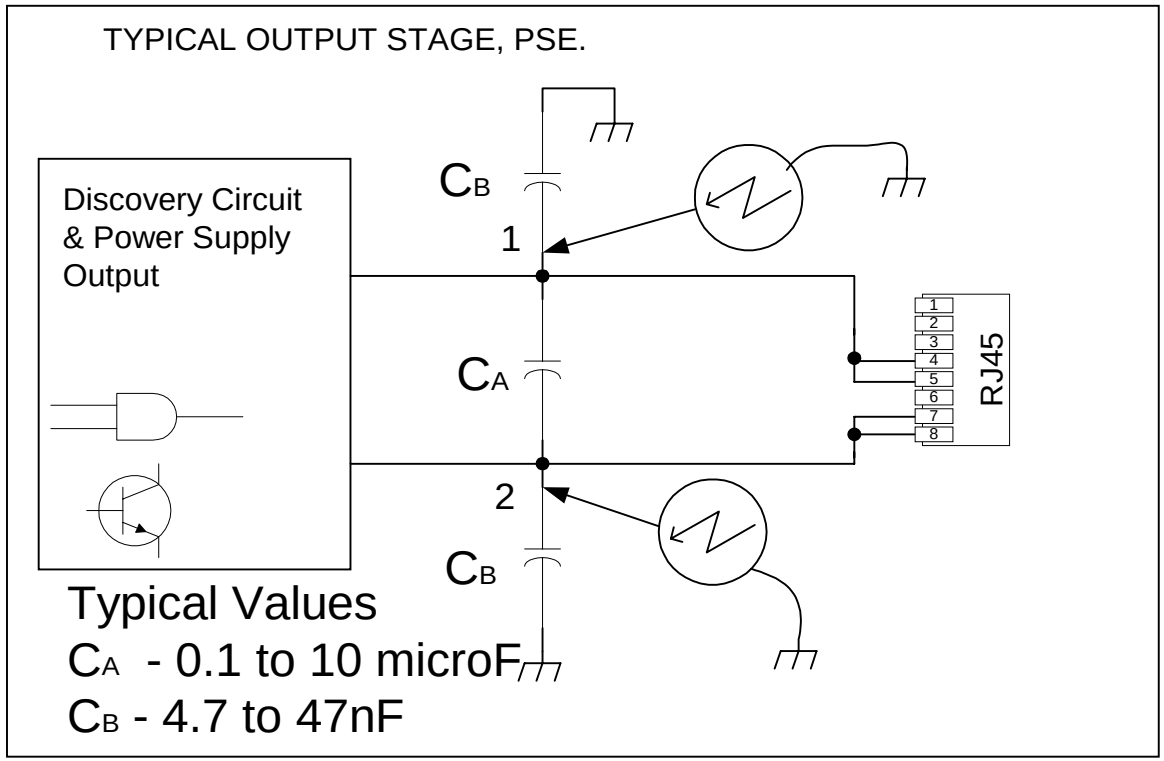
Application Method

- Direct/Indirect discharge on accessible metal parts
- Indirect discharge on the accessible isolated parts
- Horizontal coupling plane
- Vertical coupling plane

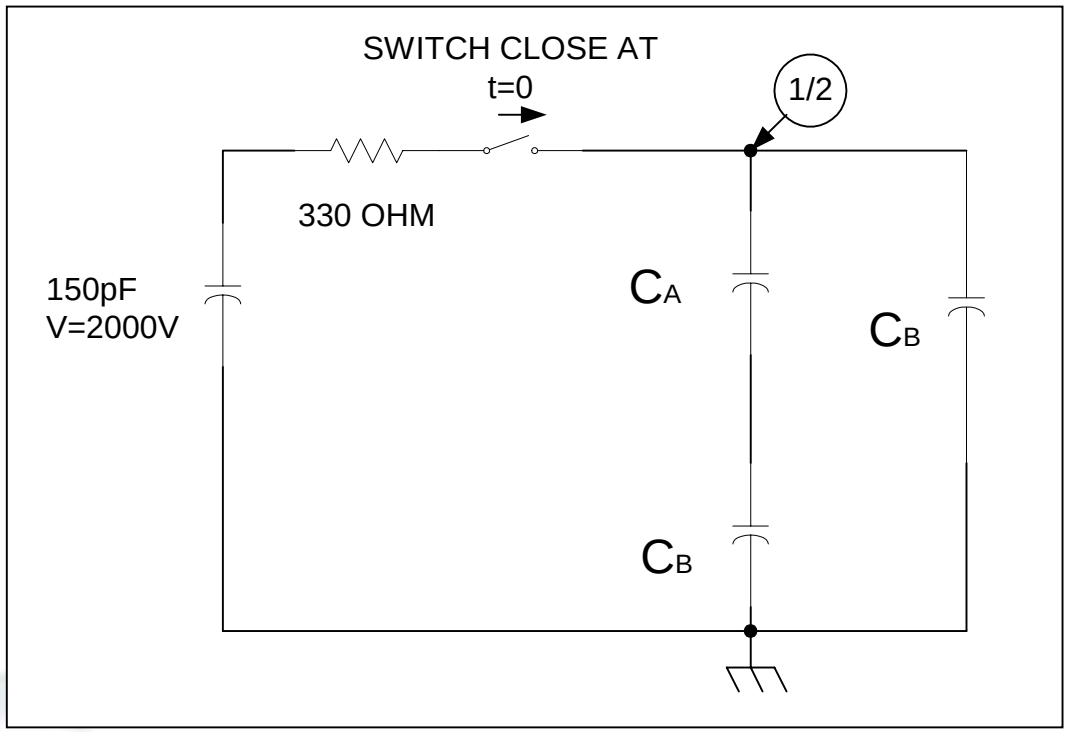
In general, the direct discharge method is recommended, as it is more repetitive than air discharge.

How do these Pulses Impact the Design?



What do we have here?

Equivalent circuit for discharge on point 1or 2



Assuming:

$C_A = 0.47\mu F$
$C_B = 0.0047\mu F$
As $C_A >> C_B$
$C_A + C_B = C_B$
Total capacitance after switch close is $\cong 2C_B$

Some calculations…

We know that:

Q @ t = 0^- = Q @ t = 0^+

$$Q = V * C \quad \Rightarrow \quad C1 * V1 = C2 * V2$$

TOTAL CHARGE IN THE SYSTEM BEFORE DISCHARGE EQUAL TO CHARGE AFTER DISCHARGE.

Where: C1=150pF, C2=2C_B, V1=V@t=0^-=Vs=2KV and V2=$V_{1/2}$@t=0^+

$\Rightarrow V_{1/2}$ @ t = 0^+ = 32V

$\Rightarrow V_{1/2}$ is the voltage developed on the contact point (can be point 1 or 2 on the system schematics), referenced to the chassis.

For V @ t = 0^- = 8KV, $V_{1/2}$ @ t = 0^+ = 127V

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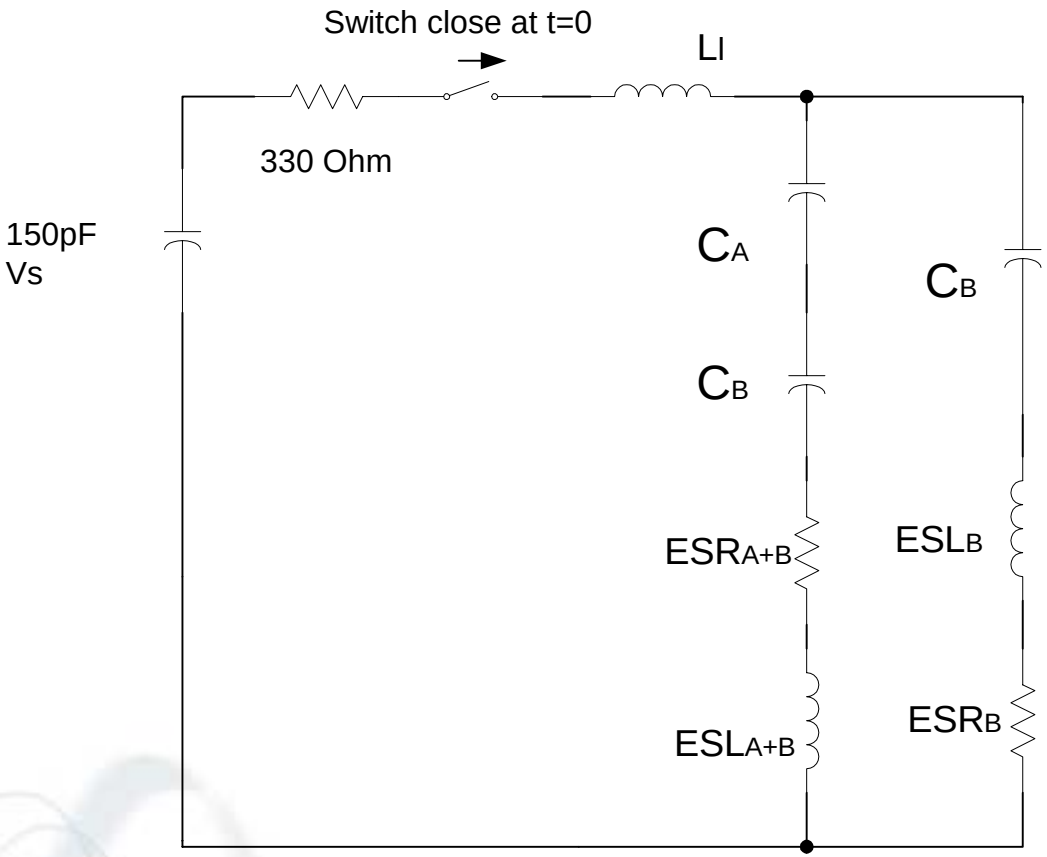
Some more numbers…

Replacing CB to 10nF will reduce the developed voltage by 50%

As the charge is on the CB and CA branch is equal on both capacitors, the voltage across these two capacitors will be reveres proportional to its values. In our case, the voltage on CA - the cross output capacitor will be roughly 10% of the calculated voltage.

Let's add Real Life Conditions



Typical values

ESL - few nH to tens of nH

ESR - few mOhms to tens of mOhms

For the simulation, we assumed:

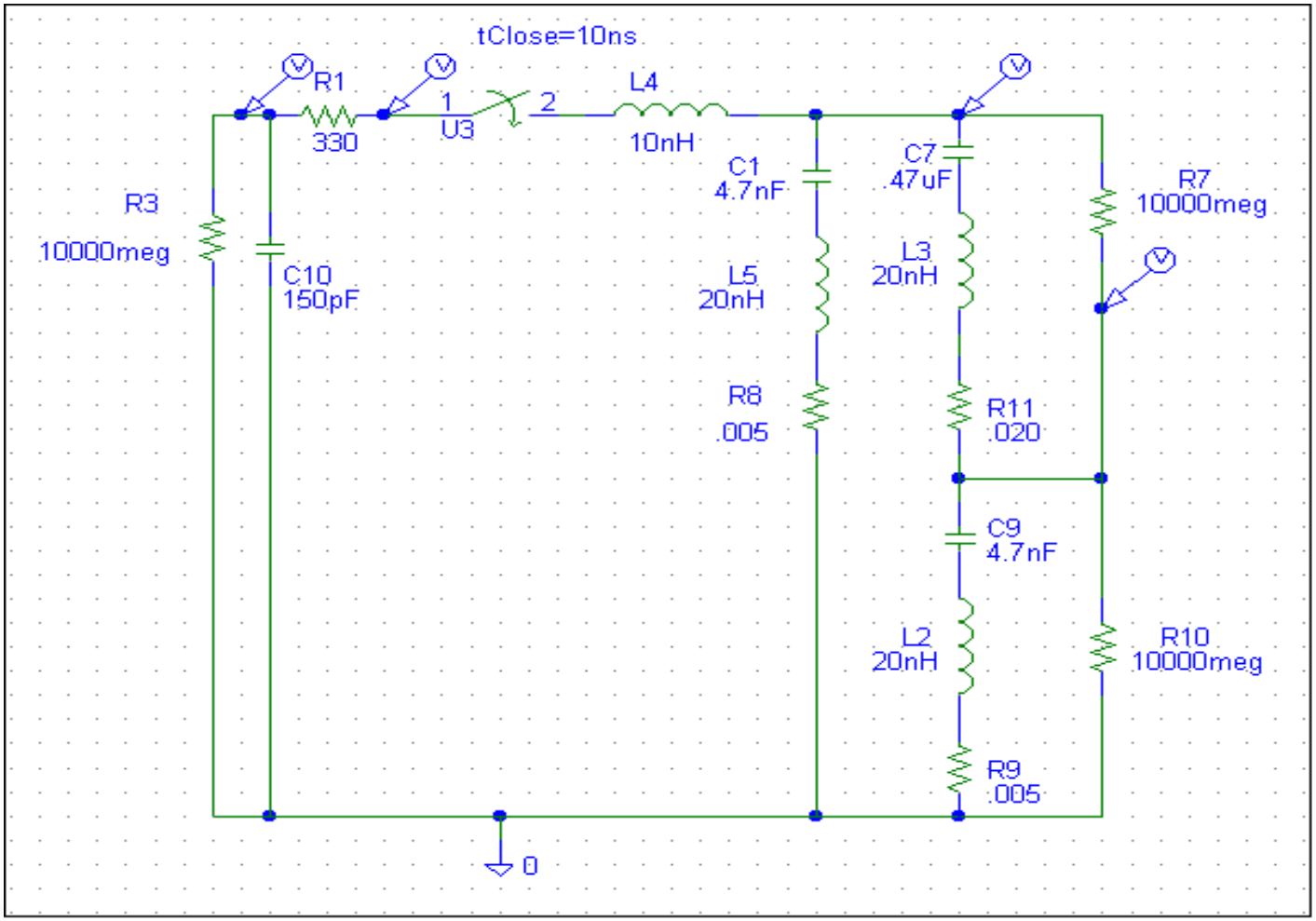
ESL=20nH for all caps

ESR=5mOhm for the ceramics, 20mOhm for the film cap.

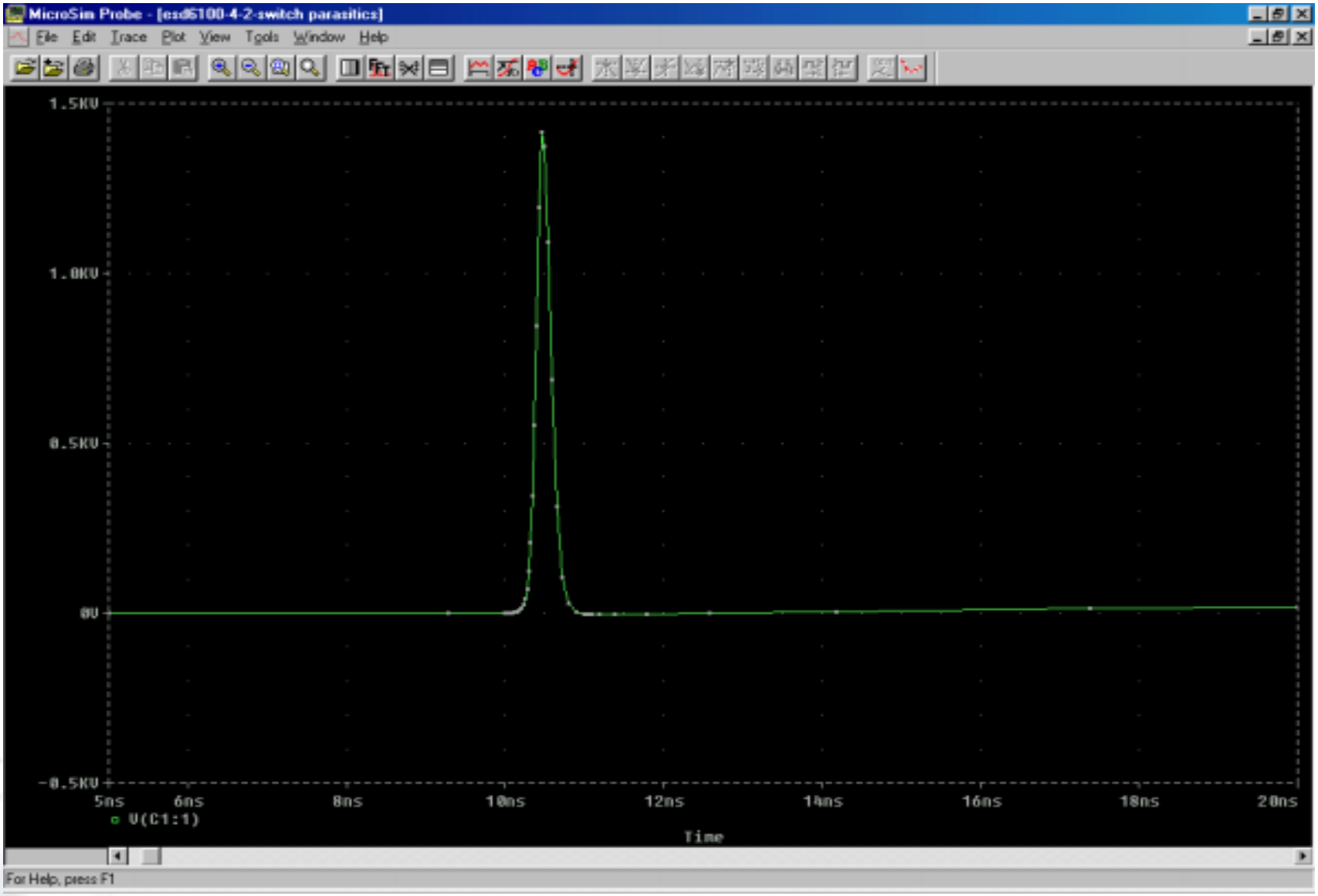
Lr = 10nHy - or 500nHy (Bid?)

Vs = 8KV (class3)

Simulation Results - Spice Model



Voltage Across Cap to Chassis (8kV Arc) Li= 10nH



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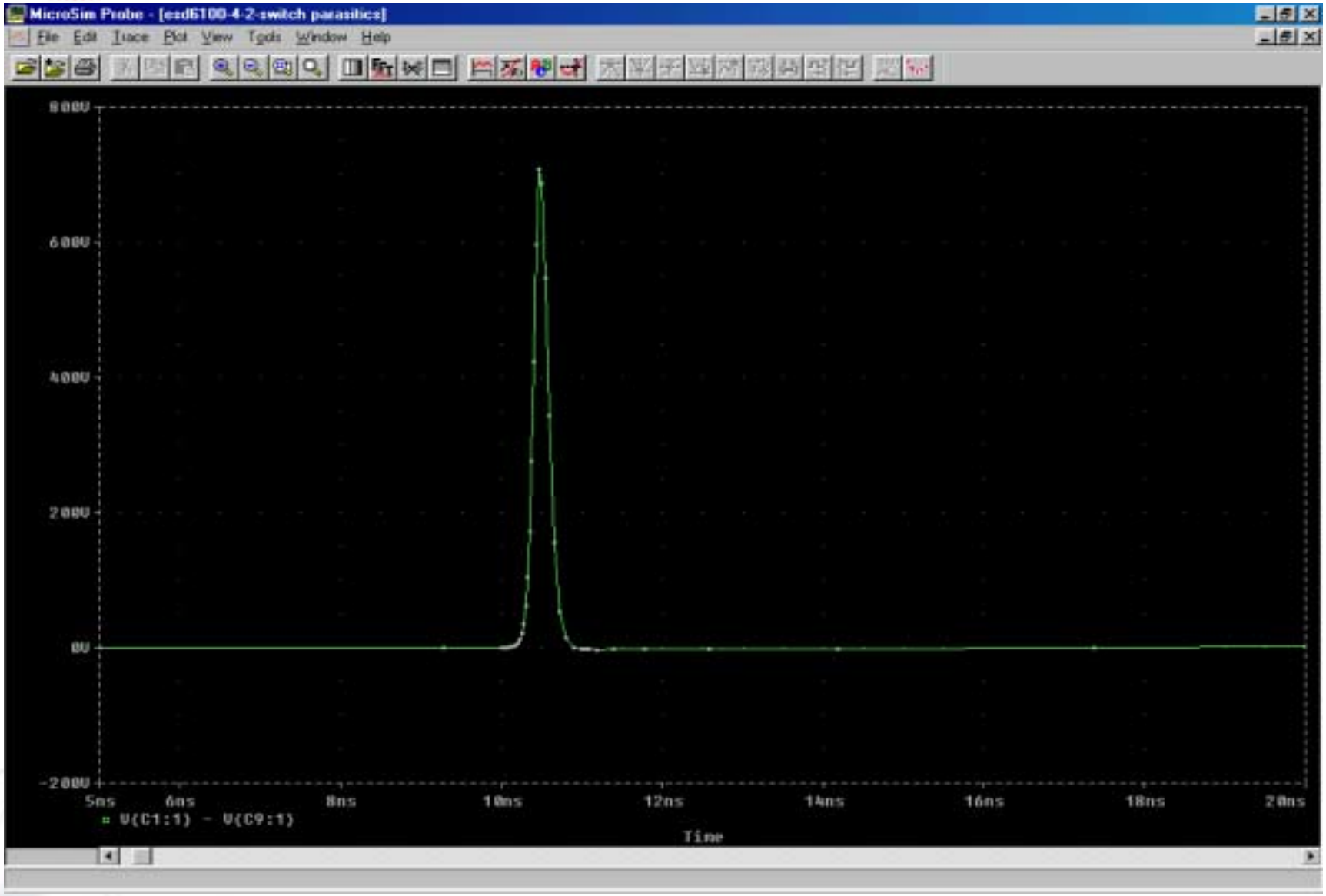
Voltage Across Input Cap (8kV Arc) L_I = 10nH



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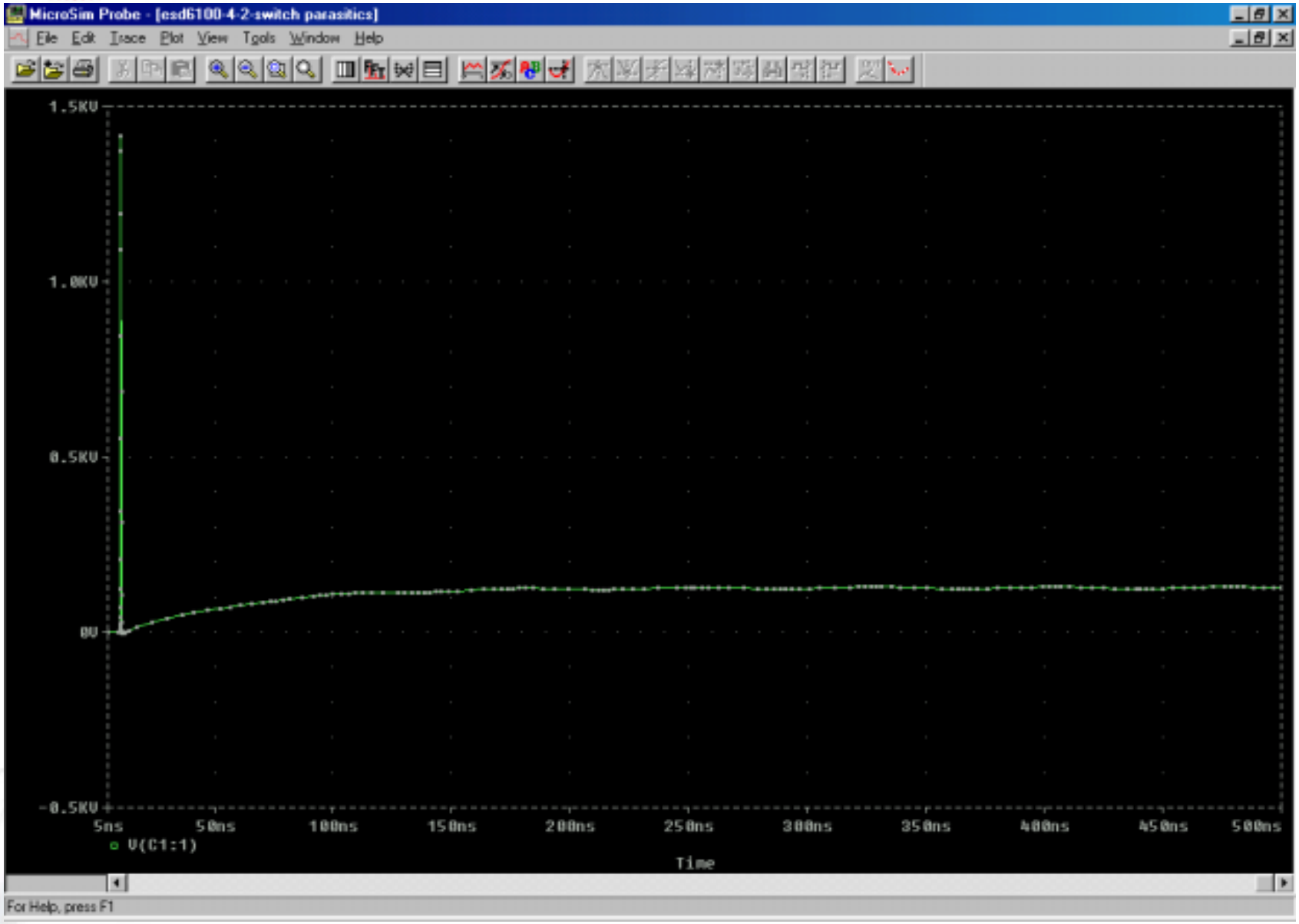
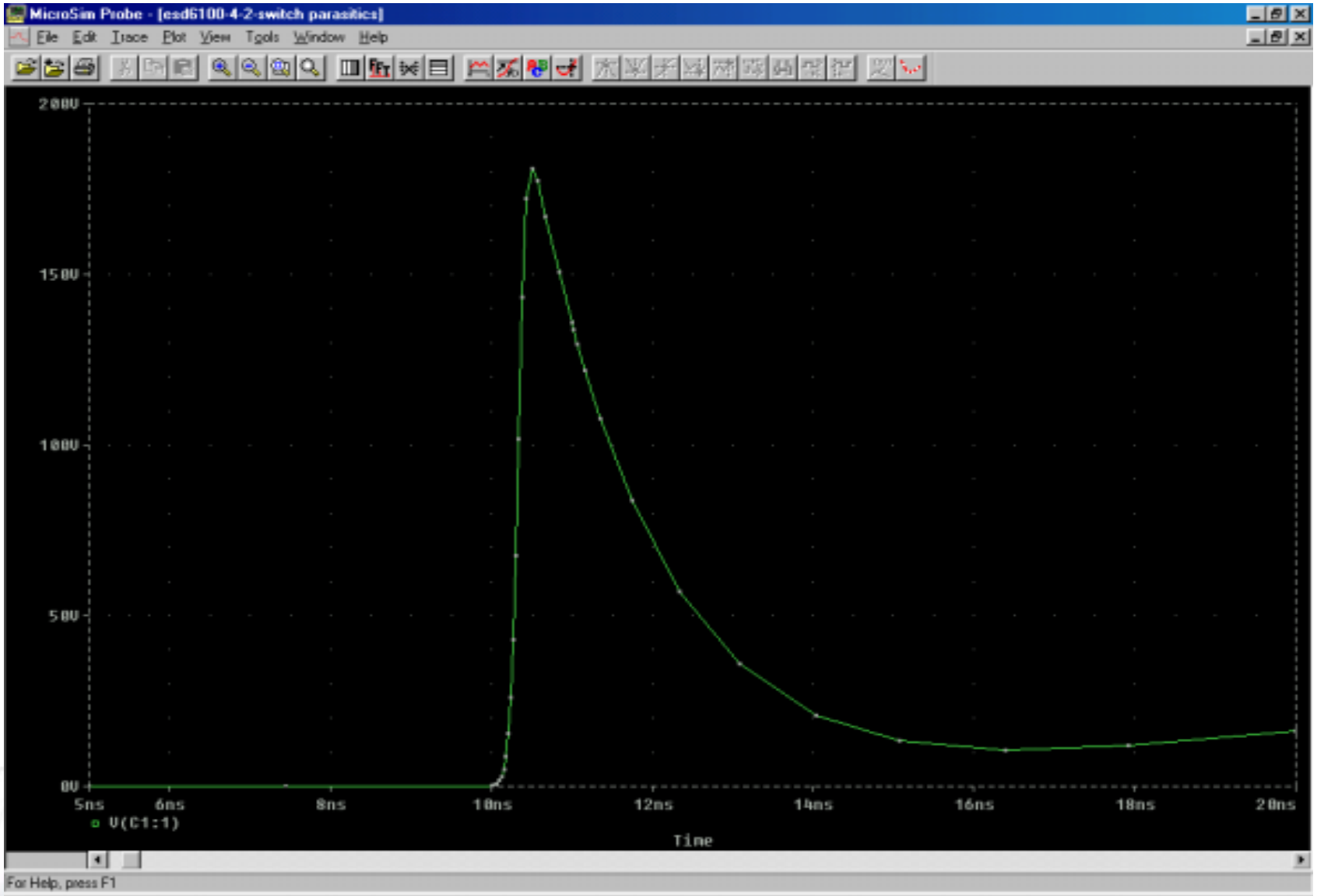
Voltage Across Cap to Chassis Steady State (8kV Arc), LI = 10nH



Voltage Across Cap to Chassis (8kV Arc) L_I = 0.5uH



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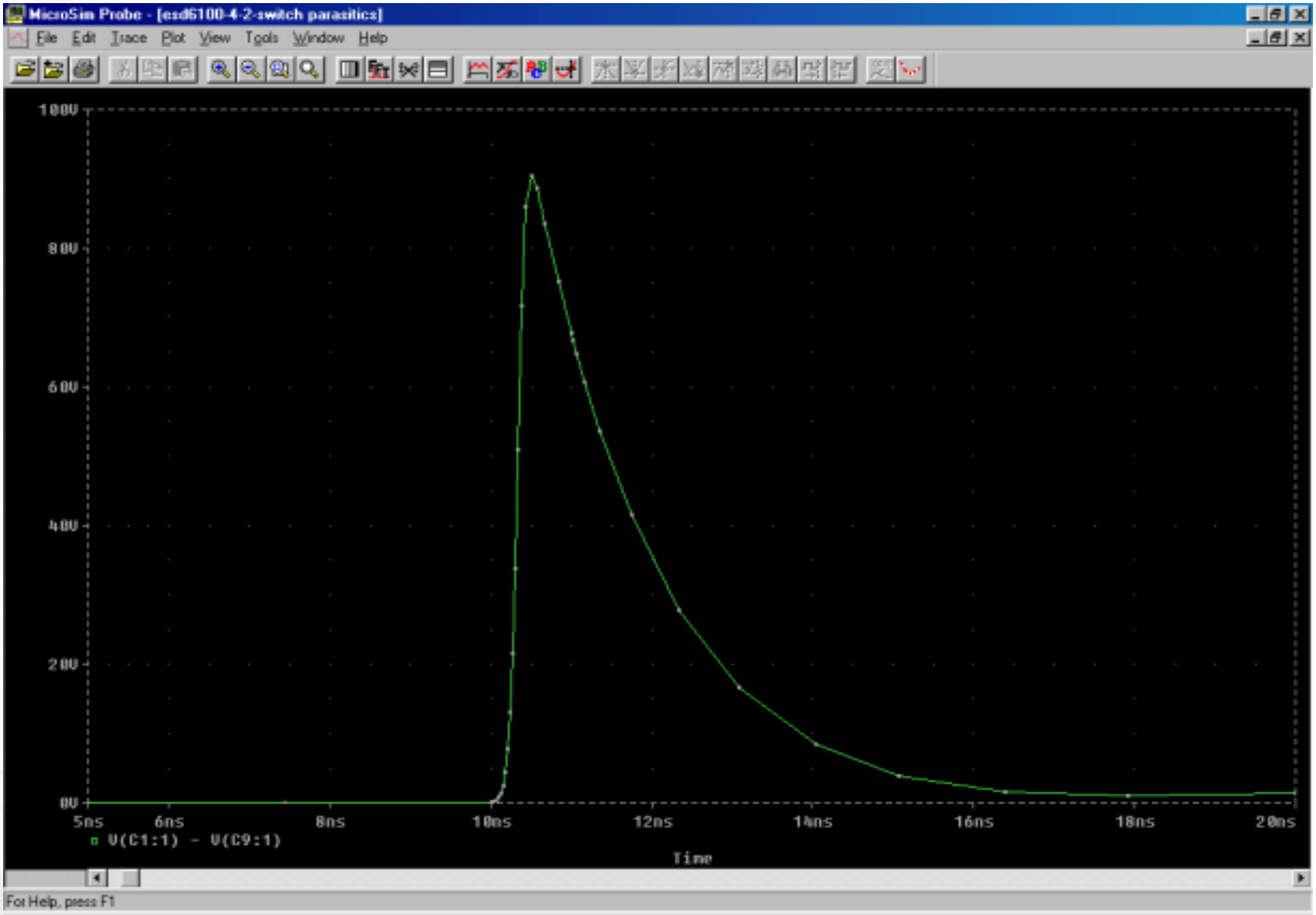
Voltage Across Input Cap (8kV Arc) LI = 0.5uH



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Conclusions

- The presentation showed that with typical power supply and typical feeding port elements the voltage stresses on the PSE components are within manageable limits.
- Some basic design guidelines where given to enable meeting Electro-Static-Discharge.
- Isolation transformer is not a must for a reliable PSE unit that will not degrade the ESD immunity of the network.
- A well protected and robust design is also economically feasible.