Vport static and transient response

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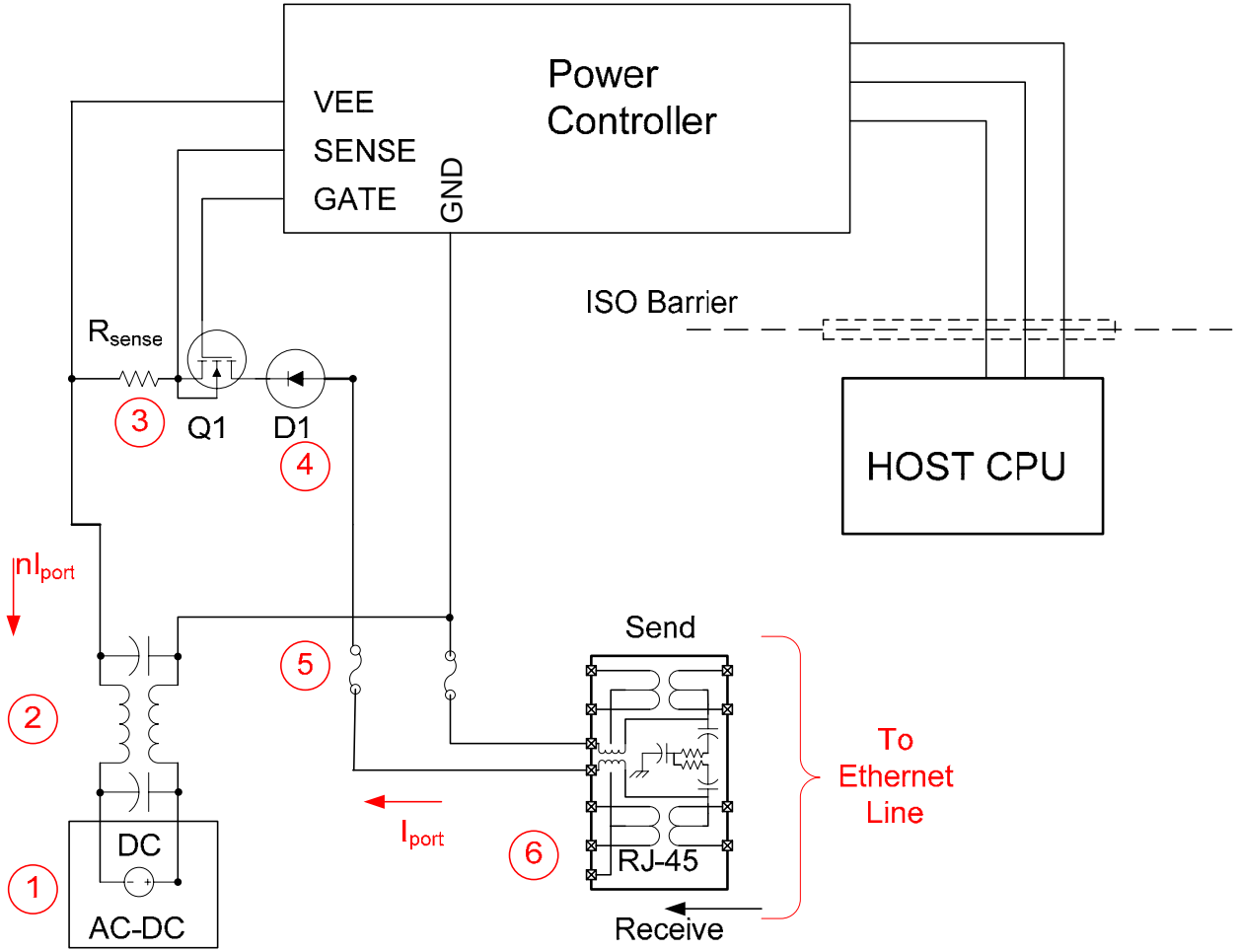
Agenda

- **Estimate the minimum static MDI voltage.**
- **Cover the team's next step.**

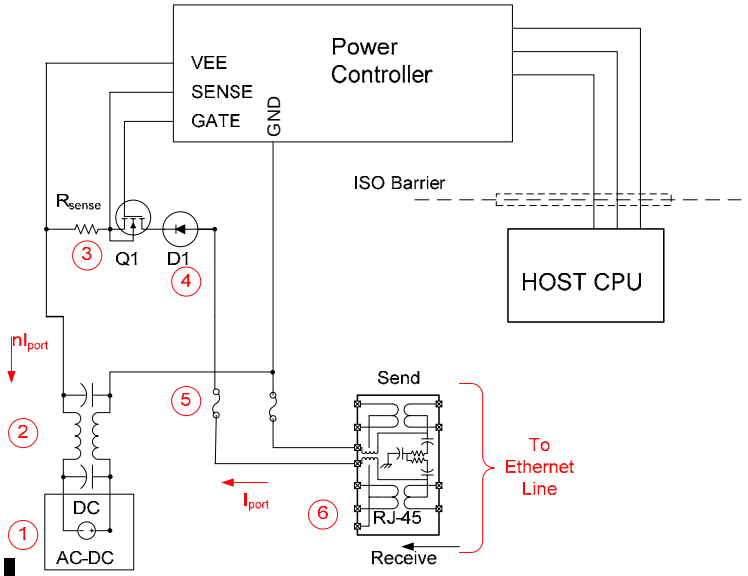
Typical PSE



One port of a multiport PSE providing power on 2-cable pairs.

Major Voltage Drop Sources

1) AC-DC Power Supply
   - Tolerance
   - Load
   - Transient response
2) CM Choke & PCB
3) Rsense & MOSFET
   - Value, internal/external
4) Pass diode
   - Presence & type
5) Fuses
   - Presence & type
6) PHY Transformer



Considerations

- **Multiple system designs use the same power supply.**
- **Systems have different:**
  - **Circuit topology**
  - **Circuit elements**
  - **PoE modules**
- **Systems need to work under all loading conditions:**
  - **< 0.5 W to PoEplus per port**
  - **1 to n ports**

Main Parameters

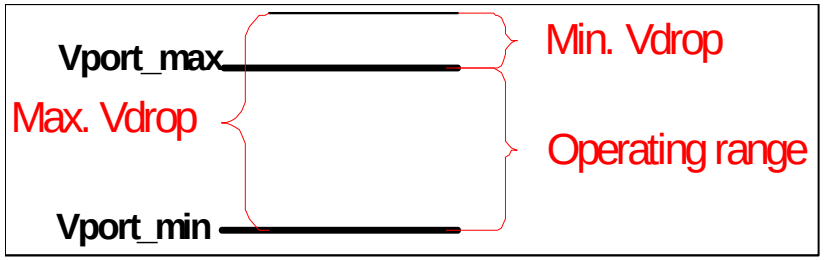
- **AC-DC**
  - **±3.7% tolerance**
  - **50 mohm output resistance**
  - **CM choke + PCB, 30 mohm**
- **Port**
  - **Rsense + MOSFET 0.53 to 1.5-ohm**
  - **Diode 0 to 0.7-V**
  - **Fuse 0 to 2x0.5-ohm**
  - **Transformer and choke 0.5 ohm**
  - **48 ports**
- **Cable**
  - **CAT-5**

Why 48 ports?

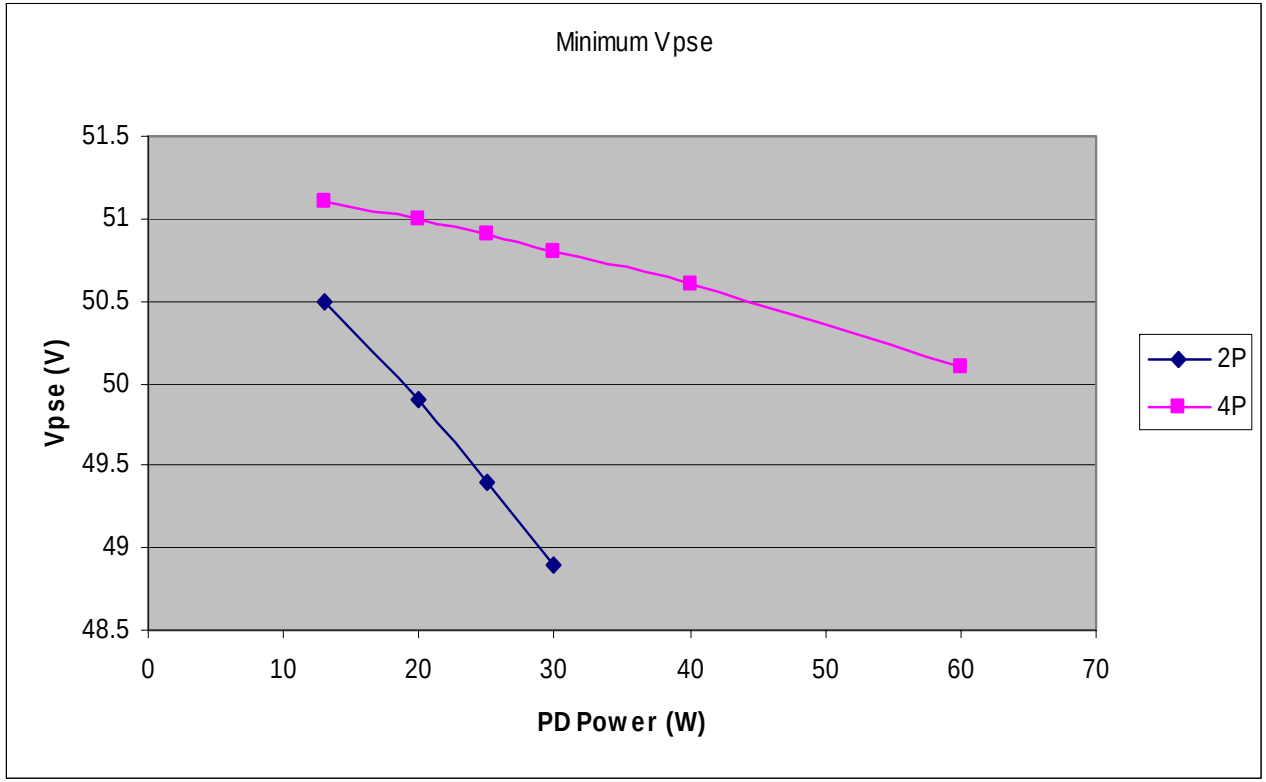
- **Focus on broadest part of the market.**
  - **15.4 W x 48 = 740 W for PoE**
  - **Lower power levels fit within this constraint.**
- **15 A, AC power circuit in Japan (100 VAC)**
  - **700 W of PoE power available**
  - **200 W of nonPoE power available**
  - **75% breaker derate, 80% AC-DC efficiency**
- **Higher port count systems need to be optimized to fit within the calculated values.**

Method

- **Calculate the maximum and minimum drops from the power supply to the MDI.**
- **Maximum drop:**
  - **Maximum PoE power draw.**
  - **Largest path resistance and voltage drops.**
- **Minimum drop:**
  - **One port on at minimum holding current.**
  - **Lowest path resistance and voltage drops.**
- **Optimize results for the always-present minimum voltage drop.**

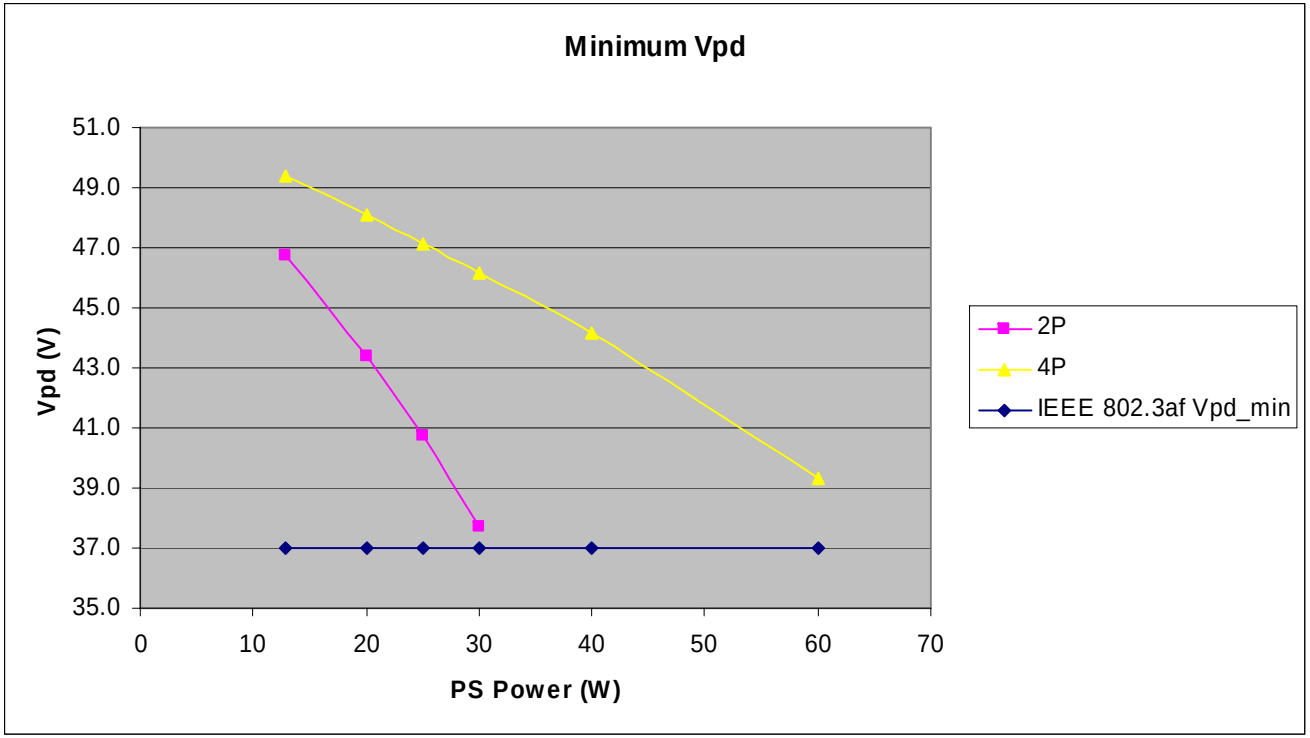


Minimum Static PSE Port Voltage



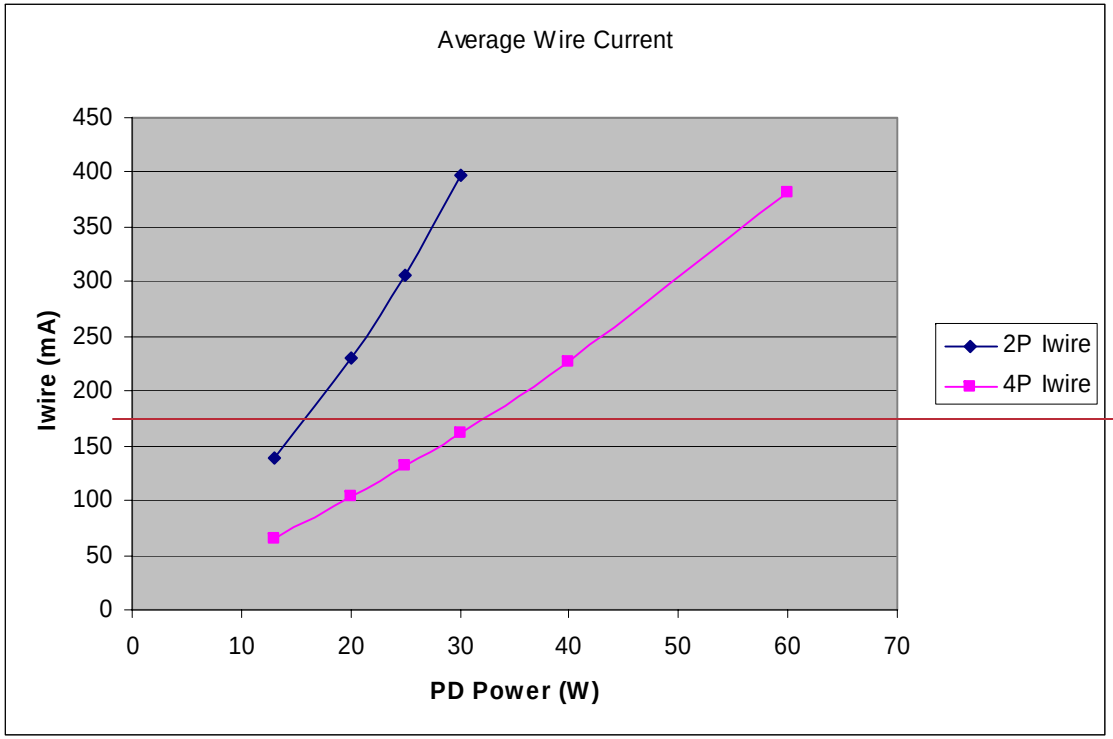
2-pair 48.9 V, 4-pair 50.1 V

Minimum Static PD Port Voltage



2-pair 37.7 V, 4-pair 39.3 V

Nominal Wire current



Can the minimum port voltage be increased?

- **A change in MDI voltage leads to a similar change in MDI current.**
- **Three things that reduce the MDI current (2 pair shown):**

  Move to DC-disconnect (0.7V →0V)

  Iwire **398→390mA**, Vport_min **48.9→49.4V**

  Improve AC-DC tolerance (±3.7%→±1.5%)

  Iwire 390→357mA, Vport_min 49.4→**52.1V**

  Use a wire fuse and better MOSFET (2.5→1.5ohm)

  Iwire 357→**350mA**, Vport_min 52.1→**52.8V**

- **A minimum port voltage in the range of 49 to 53-V is achievable but increasing the voltage above 49 V can reduce suppliers-supporting the the IEEE 802.3at specification.**

Recommendations for Static Port Voltage

- **The PD minimum port voltage ensures compatibility with IEEE 802.3af.**
- **The 30 W 2 pair IEEE 802.3at requirement has been met.**
- **The PSE minimum port voltage is raised from 44 V to 50 V.**

  PD circuit margin is 2.2 V.

  PD circuit margin for IEEE 802.3af was 1.0 V.

At a PSE port voltage of 48.5 V, the PD margin is the same as it is for IEEE 802.3af.

At a PSE port voltage of 44.0 V, the wire current increases 25% for a 2-pair system, and the PD voltage would drop to 29.8 V (30 W @ PD).

Agenda

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- **Cover the team's next step.**

Dynamic Port Voltage

- **Goal: Specify the dynamic port voltage. Provide bounds that designs can meet.**
- **Identify existing constraints.**
  - **Load change**
    - **di/dt 35 mA/uS (This may be a condition for a requirement.)**
    - **dV/dt 3.5 V/uS.**
    - **I_{CUT}**
    - **I_{LIM}**
- **Dealing with backing up the system power supply.**
- **Review system solutions for dealing with transients.**

Questions …

… or comments