Vport ad hoc discussion
November 2006

Fred Schindler

Cisco Systems

Andrew Smith	Power Integration
Anoop Vetteth	Cisco Systems
Bill Delveaux	Cisco Systems
Brian Buckmeir	Bel
Chad Jones	Cisco Systems
Christain D. ?	ST Microelectronics
Clay Stanford	Linear Technology
Daniel Feldman	PowerDsine
David Law	3COM
Derick Koonce	Independent
Frank Yung	SystemX
Fred Schindler	Cisco Systems
Helen Kastner	Cisco Systems
Jean Picard	Texas Instruments
Keith Hopwood	Phihong
Matthew Landry	Silicon Labs
Michael Altmann	Akros Silicon
Ramesh Sastry	Cisco Systems
Raul Lozano	Pulse
Sajol Ghoshal	Akros Silicon
Taufique Ahmed	Akros Silicon
Thong Nguyen	Maxim
Thuyen Dinh	Pulse
Tim Parker	Nortel Networks
Wael Diab	Broadcom
Yair Darshan	PowerDsine

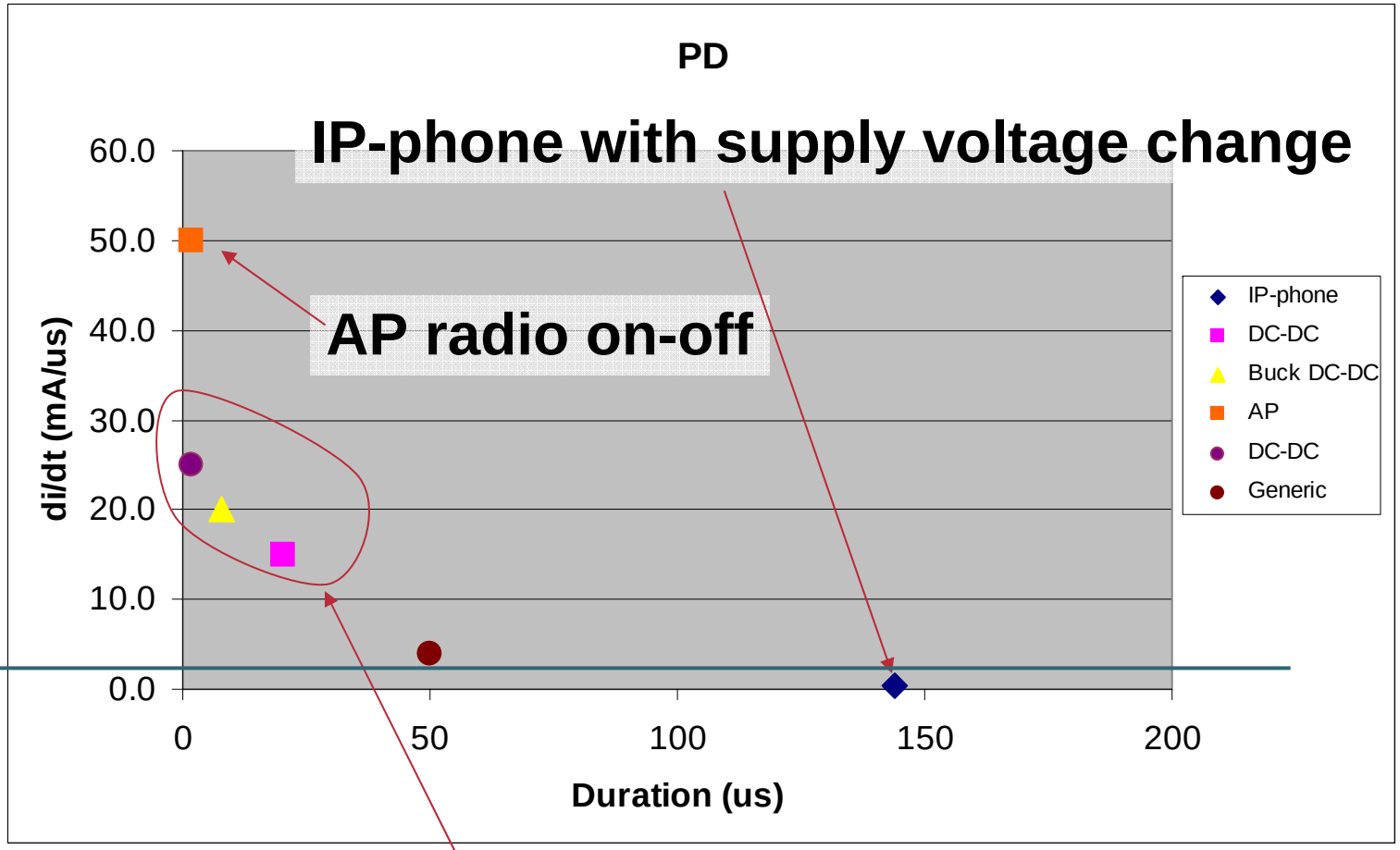
Agenda

- **di/dt**
- **Data collected.**
- **Current limits.**
- **An option for dealing with voltage transients.**
- **The need for new current limits and approach.**
- **Next step.**

PD di/dt limits?

- **33.2.8.2 Load regulation**
  PSE dv/dt < 3.5 V/us @ di/dt = 35 mA/us
- **dv/dt = |Z| di/dt, |Z| = 100 ohms**
- **Table 33-5, item 3 and table 33-12 item 7.**
  < 1 MHz, Vpp < 0.1 Vpp
  dv/dt (max) = $V_p 2\pi f$ = 0.3 V/uS
- **PD di/dt limit. di/dt = dv/dt/R**
  di/dt = 0.3/(100 + 12.5) = 2.7 mA/us
- **There are no PICS for PD di/dt limits.**

Sample PD di/dt values

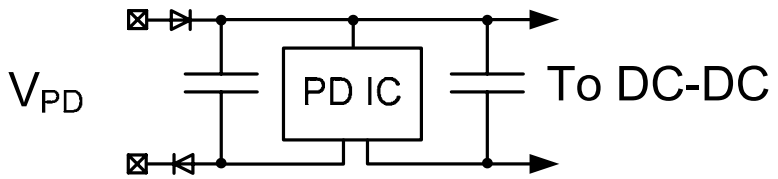


Indirect IEEE 802.3 limit 2.7 mA/us

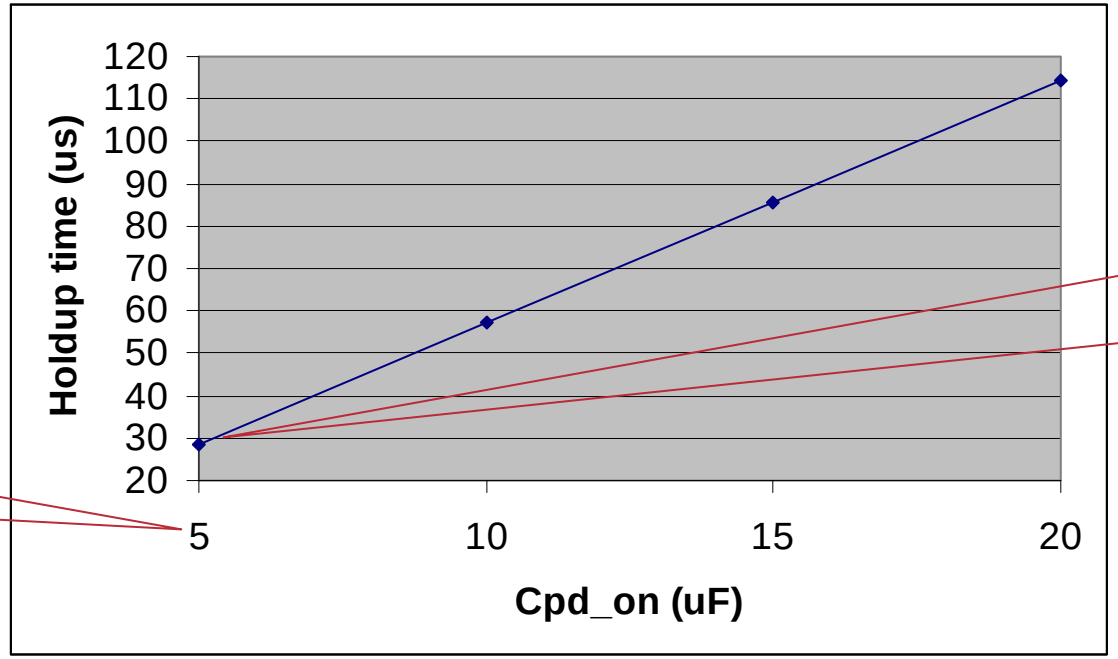
DC-DC load changes

PD di/dt and PSE voltage droop

- **Most sample PDs violate the indirectly calculated di/dt limit!**
- **Many PDs are UNH tested and pass.**
- **The di/dt threshold needs to be called out more directly.**
- **PD di/dt demands are supported by PD bulk capacitance or PSE output capabilities.**
- **The PSE voltage droop permissible and the maximum cable current help determine whether the PD bulk capacitance or the PSE output provide the current demanded.**



Fast transients



802.3 minimum

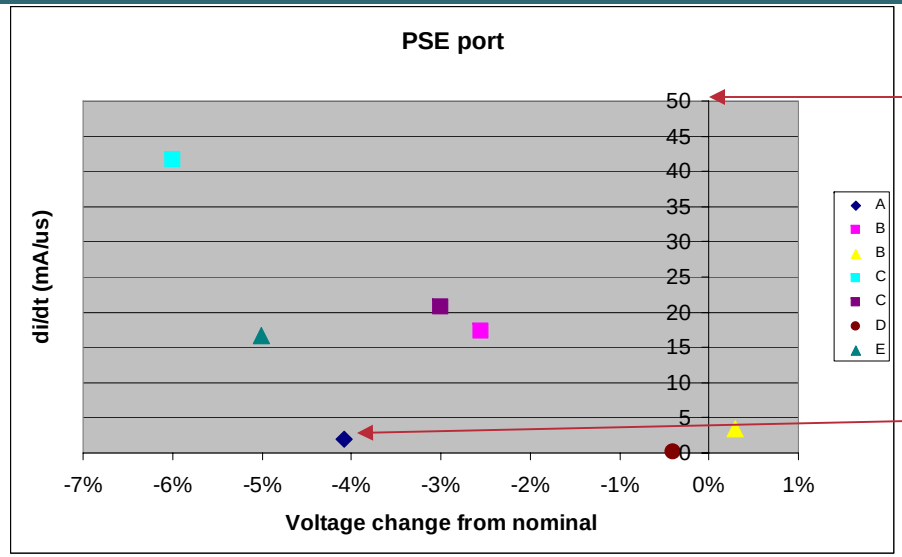
Most sample PDs have a transient duration of less than 30 us.

When the PD bridge is reverse biased the PD bulk capacitance provides the PD power.

Sample PDs with durations 50 uS or longer have a di/dt of less than 5 mA/us and result in less than a 5% V_{PSE} change for PSEs in the sample set.

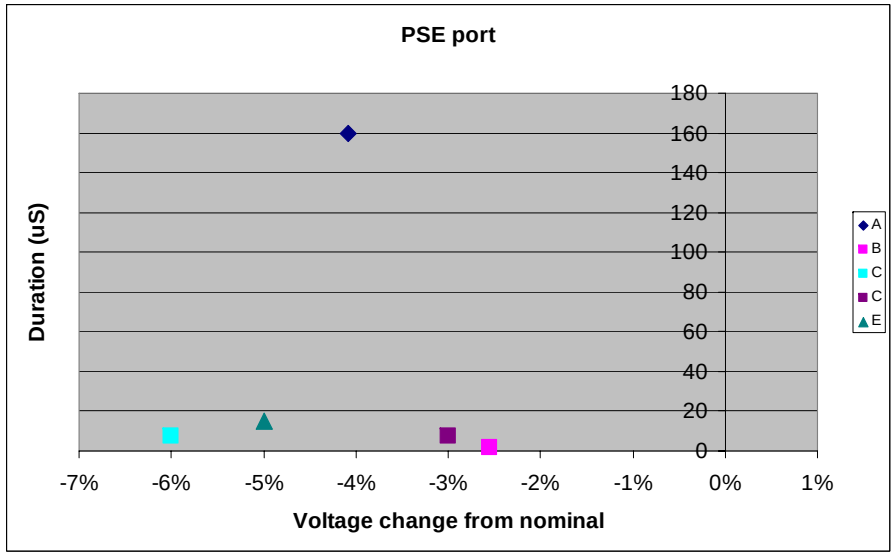
dt = CdV/I, I = I_{LIM_MIN} = 840 mA, at this current a 30 W PD has at least 36 V at its input.

Sample PSE load change effects



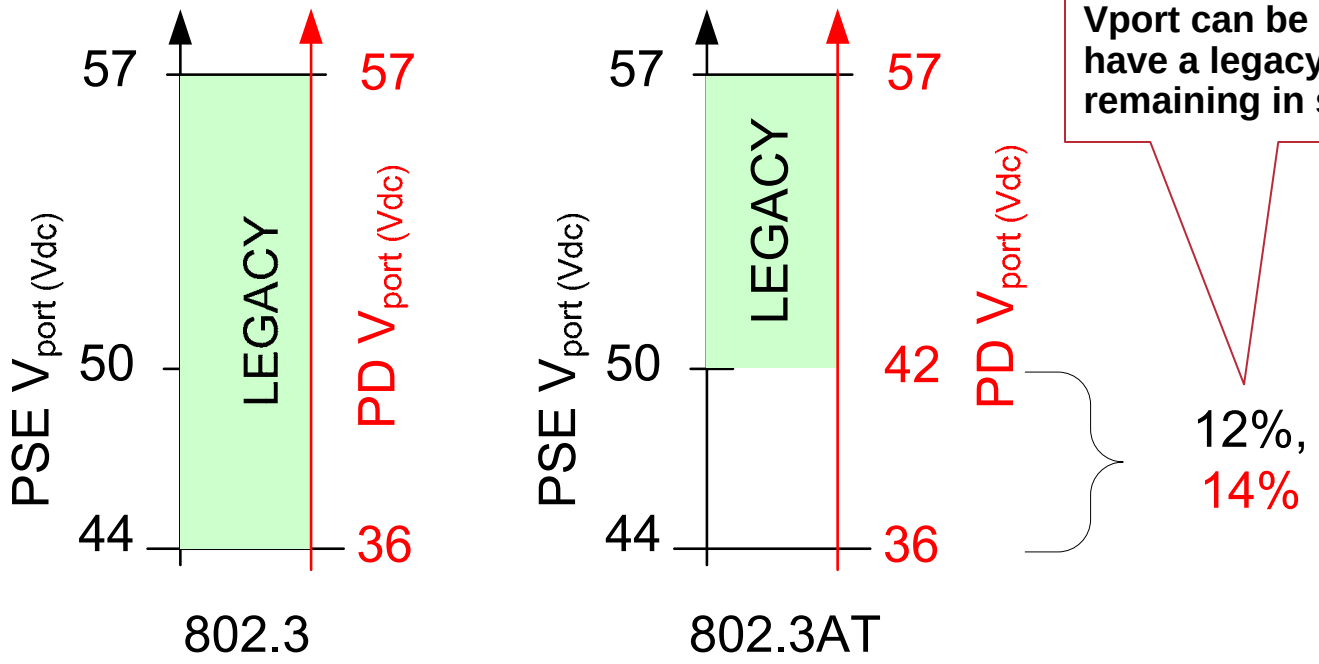
Highest PD di/dt from sample set.

Slow 0 to 100% load change.
160us transient.



The Knoxville XLS was correct,
The PPT was incorrect for this slide.

Legacy PD

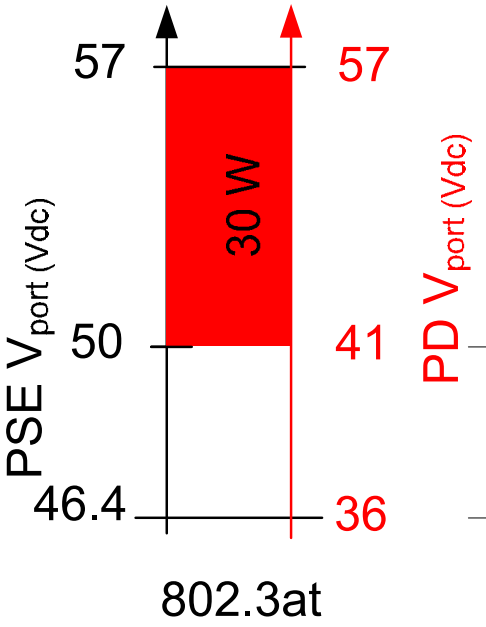


$$V_{PD} = V_{PSE} - I_{port}\,R$$

$$36 = 44 - I_{LIM\_MIN}\,20 \qquad 42 = 50 - I_{LIM\_MIN}\,20$$

I_{LIM_MIN} = 400 mA

30W PD



7.2%,
11.8%

VPSE (Vdc)	VPD (Vdc)	Icable (mA)	Ppd (W)	Ppse (W)
50	40.8	735	30	37
	36	1124	40	56
46.4	36	834	30	39
42.5	30	1000	30	43

This value is almost 2x the maximum average PD power demand.

It is determined using the same method as IEEE 802.3.

Do we want new PDs to operate at a lower port voltage than legacy devices?

The largest droop for the sample PSEs is 6%.

I_{CUT} and I_{LIM} thresholds

- None of the sample PDs cross the I_{cut} threshold.
- $I_{CUT} = P_{PSE\_MIN}/V_{port}$,(<5% duty cycle at the PD)
- I_{LIM} is a fix value not related to V_{port}.
- These current thresholds exist to permit the PD to draw more power than their reported average power.
- All sample PD current transients are less than 150 uS, while PSE voltage transients are less than 200 uS.
- TLIM and Tovld are approximately 250x larger than the largest transient.
- The current thresholds and the purpose of these currents need to be evaluated for this extension to PoE.

Next Step

- **Determine how to better convey PD di/dt rate limits.**
- **Determine what the PD di/dt limits should be.**
- **Collect more PD and PSE system input.**
- **Review current thresholds and their purpose.**
- **Adjust recommendations based on cable limit data.**
- **Determine what channel model the AF specification should use.**

Based on V11 Spreadsheet.