4x25 Gb/s SMF Optics:
Channel Spacing Considerations

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Outline

- *Application Overview*
- *Technology Choices*
  - *EML vs. DML TOSA*
  - *Cooled vs. Uncooled TOSA*
  - *LAN WDM vs. CWDM*
  - *Potential for integration*
- *Development Constraints*
- *Summary*

Application Overview

- Consensus view on 10 km reach objective
  - Enterprise applications < 10 km
  - 4 x 25 Gb/s channels centered at 1312nm (O-band)
  - EML or DML transmitter
  - PIN receiver
- Consensus view on 40 km reach objective
  - Metro applications < 40 km
  - 4 x 25 Gb/s channels on LAN WDM grid (400 or 800 GHz) centered at 1312nm (O-band)
  - Cooled EML transmitter
  - OA+PIN receiver
- Outstanding issues
  - Choice of LAN WDM or CWDM grid for 10 km objective

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Technology Choices: Link Budget

- LAN WDM is preferred for 40km due to lower CD, noise bandwidth and OA bandwidth
- DML chirp is too high for 40km links – requires EML
- Cooled CWDM DML will be challenging for 10km due to higher alpha and CD and lower MM compared to EML
- Link budgets are tight even for cooled transmitters
  - It will be challenging to develop uncooled DFB lasers with high enough output power for 4x25G PMD
  - Low cost uncooled solutions will likely be delayed
- 25G cooled EML is well developed and can support the dispersion tolerance of all proposed PMDs

Capability matrix

		Channel Spacing and Reach			
Source	**Un/Cooled**	**WDM 10km**	**WDM 40km**	**CWDM 10km**	**CWDM 40km**
25G DML	**Cooled**	Yes	High CD	Marginal CD	High CD
	Uncooled	NA	NA	Pout limited Marginal CD	High CD
25G EML	**Cooled**	Yes	Yes	Yes	High CD High OA noise
	Uncooled	NA	NA	Pout limited	High CD Pout limited

Cooled EML on LAN WDM grid is the only technology that supports both 10km and 40km reach objectives.

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Wavelength targeting capability

- *Typical DFB wavelength distribution for 50mm wafer*
  - *Intra-wafer σ ~ 0.6 nm, Inter-wafer σ ~ 0.7 nm, Total σ ~ 0.9 nm*
  - *Spacing between channels in phase-shifted DFB arrays is fairly uniform*
- *Temperature tuning capability*
  - *DFB laser: ~0.1 nm/°C for ± 0.5 nm with ± 5 °C*
  - *InP or SOI AWG: ~0.1 nm/°C for ± 0.5 nm with ± 5 °C*
  - *Silica AWG: ~0.01 nm/°C*
- *For CWDM, wavelength tolerance is ± 5 nm, so yield is close to 100% for wavelength alignment alone*

Wavelength yield for LAN WDM

- *Assume demux is aligned to channel grid*
  - *SOI AWG can be heated to align grid if needed*
- *Laser and demux AWG must align within ~ ± $\Delta\lambda/4$ for less than 1 dB excess loss*
  - *LAN WDM (800 GHz): tolerance for 1dB loss ~ ± 1.1 nm*
  - *Laser temperature tuning of ±7 °C allows laser wavelength range of ± 1.8 nm or ± 2σ of DFB capability (> 90% yield)*

- *LAN WDM wavelength spacing is feasible without significant yield hit due to wavelength registration*

Technology Choices: Integration

- *Integration is the key to long-term size, power dissipation and cost reduction*
  - *Established low-cost technologies like selective area growth and quantum well disordering are preferred*
- *LAN WDM enables simple, robust DFB and EAM integration*
  - *Bandgap range: 3 x 4.5nm + 40nm = 53.5 nm*
  - *This is well within the capability used for discrete EMLs today*
  - *Defects are correlated, so yield tends to be better than y^N estimates*
- *CWDM requires the integration of a much wider range of active materials*
  - *Bandgap range: 3 x 20nm + 40nm = 100 nm*
  - *Thickness, bandgap and effective index control become more difficult*
  - *Laser and modulator performance are more non-uniform*
  - *Gains in wavelength yield are partially offset by losses due to non-uniform device performance*

- *LAN WDM is preferred for low-cost integration and high performance*

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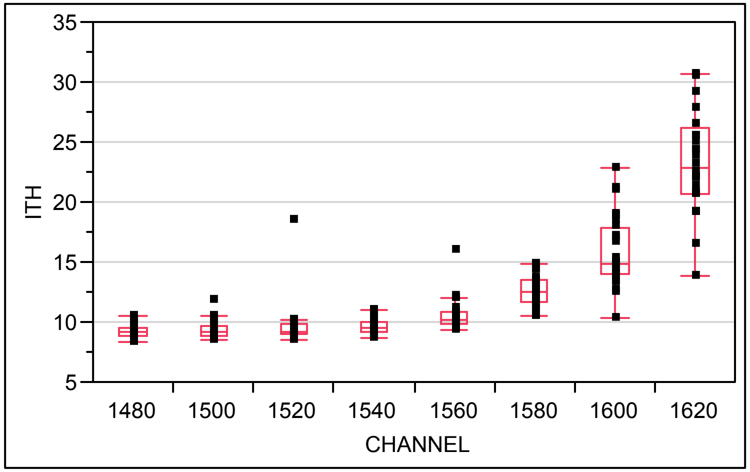
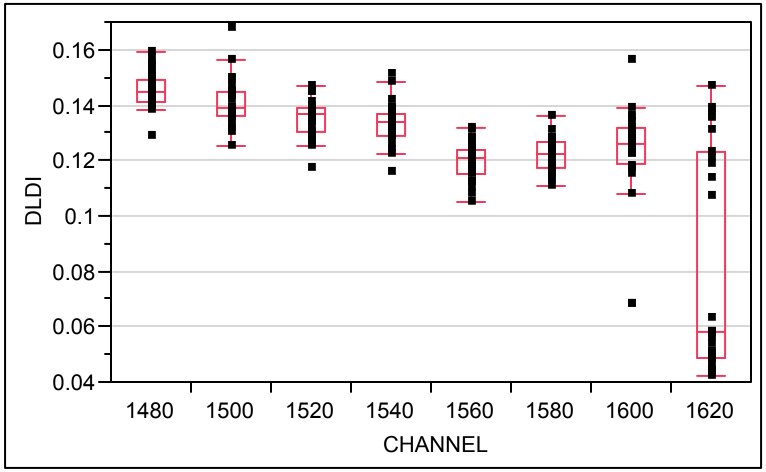
CWDM DFB array Ith and Slope





Monolithic 8λ array of 1550nm DFB lasers on 20nm grid fabricated by selective area growth (SAG)

Large SAG enhancement (>100nm) can result in yield loss due to non-ideal material properties, as well as worse reliability.

For EML integration, the lasers have the largest bandgap shifts.

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Integrated mux/demux options

- *Hybrid integration allows separate yielding of active and passive components and minimizes InP chip cost*
  - *Requires precise alignment (active or passive)*
  - *Laser input coupling loss with tolerances are typically > 3 dB*
  - *Detector coupling losses are low – hybrid is preferred for ROSA*
- *Monolithic integration reduces coupling losses but DFB array and combiner are yielded together*
  - *AWG minimizes mux insertion loss at the expense of additional mux yield, wavelength alignment yield and chip size*
  - *Power splitters have higher yield, smaller chip size (~50% of AWG) and no wavelength alignment yield at the expense of slightly higher insertion loss*

Integrated TOSA loss comparison

Multiplexer				Coupling Loss			Total Loss	
Type	**Rel. Chip Area**	**Insertion Loss**	**λ Reg. Loss**	**Hybrid Input**	**Mono Input**	**Output Fiber**	**Hybrid**	**Mono**
Splitter	1X	7.5	0	3	1	1	11.5	9.5
MMI	1X	6.5	0	3	1	1	10.5	8.5
AWG	2X	4	1	3	1	1	9	7

All losses in dB

DBF array + monolithic MMI combiner offers an interesting compromise between insertion loss, mux yield, wavelength yield and chip size/cost.

Product Development

- *Component vendors are under continual pressure due to provide ever lower cost solutions, which affects development capability*
  - *Development cost is an important part of the overall cost of a product, and can't be neglected in the analysis.*
  - *Development budgets and staff are limited, so it's more difficult to develop multiple products in parallel.*
- *Developing a single TOSA that can serve all reaches is critical to reducing unit cost and initial time to market.*
  - *Single product development reduces cost and time to market*
  - *Shared volume for all reaches reduces unit cost*

- *Cooled EML on LAN WDM grid is the only approach which meets the criteria*

Summary

- *Consensus is required on 100GE channel spacing before any investments in product development*
- *Due to the difficult economics of the component sector, a common configuration for both enterprise and metro reaches is needed to reduce unit cost, development cost and time to market*
- *4x25G cooled EML TOSA on 800 GHz grid is the lowest cost path short term and long term*
  - *Technically feasible based on existing 10G and 40G products*
  - *Provides link margin for all reaches up to 40km for high module yield*
  - *Acceptable wavelength tolerances for high transmitter chip yield*
  - *Enables monolithic integration using established technologies for future cost reduction*
- *To exclude a LAN WDM solution for 10km reach would unnecessarily delay product development and increase costs*
  - *CWDM will become important when breakthroughs are made in uncooled 25G DFB performance*

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Thank You!