Miscellaneous PCS Issues

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Agenda

- PCS State Machines
- MII and PCS Ordered Sets

PCS State Machines Background

- Today with 10GBASE-R, there are two state machines operating on the receive stream and looking at the sync bits
  - Lock state machine
    - Looks for 64 non-errored sync blocks in a row to declare in sync
    - Looks for 16 errored sync blocks out of 64 to declare out of sync
  - BER state machine
    - Looks for 16 errored sync blocks out in 125usec window to declare high BER
    - High BER ~ 10^{-4}

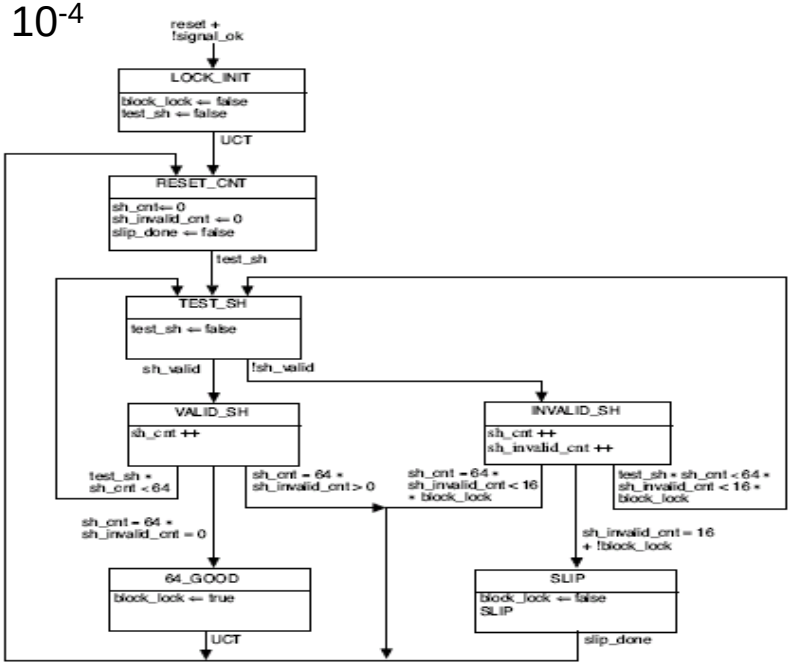


Figure 49–12—Lock state machine

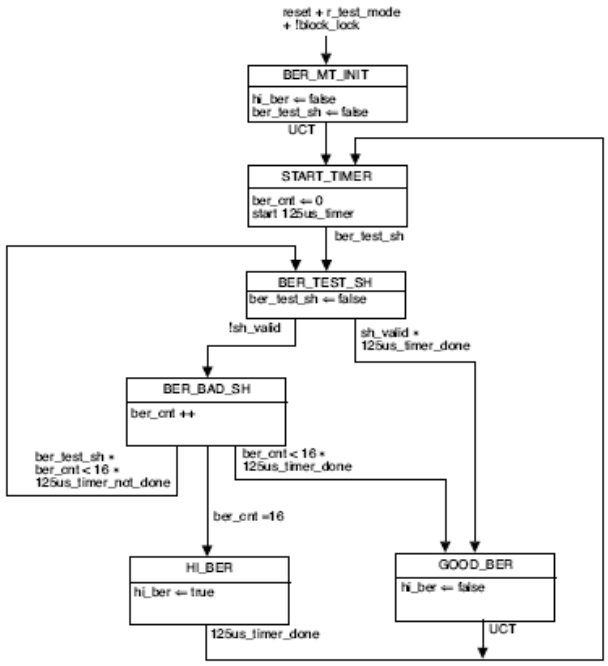


Figure 49–13—BER monitor state machine

Now for 100/40Ge

- We need SMs operating on each Virtual Lane instead of a single stream
- First we find 66b alignment, then we hunt for alignment markers
- Should we keep the same sync SM, just run 4 or 20 instances of them?

  I would assume yes…no need to also run it on the aggregate stream either

- Do we need the BER SM as is, just run 4 or 20 instances of them?

  Should be some value in identifying high BER VLs, though we can not always correlate that to a particular physical lane, but if just some are high BER, you could run test patterns to isolate a problem

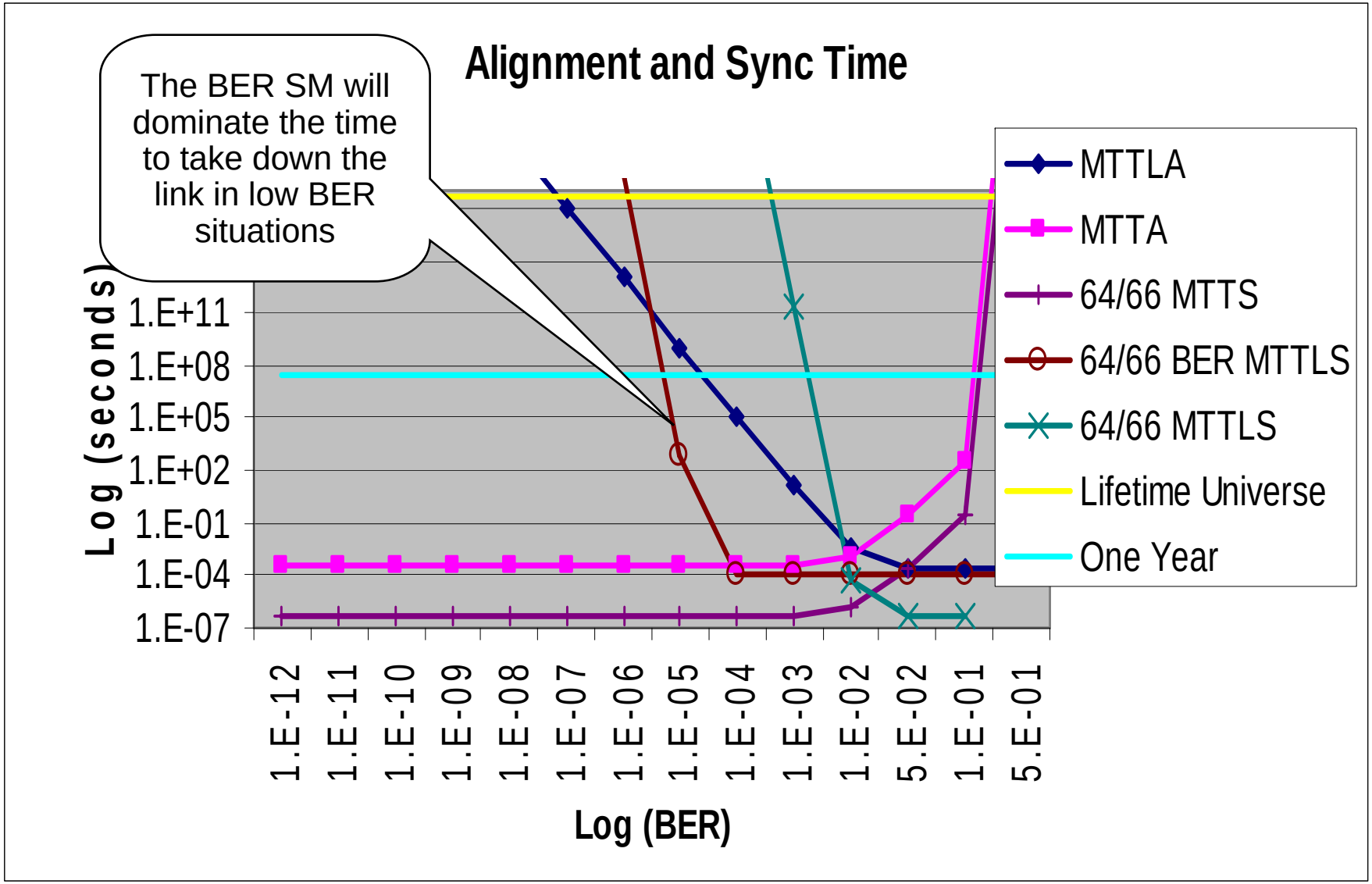
- Or we could run the BER SM on the aggregate stream?

  This makes sense if we don't care about identifying individual VLs that are misbehaving

100/40Ge Proposed SM Plan

1. The 66b lock SM runs on each Virtual Lane
2. Then an Alignment Marker SM runs on each Virtual Lane
3. The Virtual Lanes are De-skewed
4. Then the BER SM is run on the aggregate data stream

100/40Ge Proposed SM Plan



Ordered Sets

- In the 10GBASE-R PCS, two types of ordered sets are supported

  Sequence ordered sets: Local and remote faults

  Signal ordered sets: Reserved for future use (used by Fiber Channel)

- In XGMII, only sequence ordered sets are supported

  Sequence ordered sets: Local and remote faults

Options for Ordered Sets

- In XGMII the ordered sets are defined as follows:

Table 46–5—Sequence ordered_sets

Lane 0	Lane 1	Lane 2	Lane 3	Description
Sequence	0x00	0x00	0x00	Reserved
Sequence	0x00	0x00	0x01	Local Fault
Sequence	0x00	0x00	0x02	Remote Fault
Sequence	≥ 0x00	≥ 0x00	≥ 0x03	Reserved

NOTE—Values in Lane 1, Lane 2, and Lane 3 columns are in hexadecimal, most significant bit to least significant bit (i.e., <7:0>). The link fault signaling state machine allows future standardization of reserved Sequence ordered sets for functions other than link fault indications

Ordered Sets

- Proposed ordered set format for the XLGMII/CGMII
- With 8B alignment, ordered sets span 8B

Table 151–5—Sequence ordered_sets

Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7	Description
Sequence	0x00	0x00	0x00	0x00	0x00	0x00	0x00	Reserved
Sequence	0x00	0x00	0x01	0x00	0x00	0x00	0x00	Local Fault
Sequence	0x00	0x00	0x02	0x00	0x00	0x00	0x00	Remote Fault
Sequence	≥ 0x00	≥ 0x00	≥ 0x03	≥ 0x00	≥ 0x00	≥ 0x00	≥ 0x00	Reserved

NOTE—Values in Lane 1, Lane 2, and Lane 3 columns are in hexadecimal, most significant bit to least significant bit (i.e., <7:0>). The link fault signaling state diagram allows future standardization of reserved Sequence ordered sets for functions other than link fault indications

Ordered Sets

- With the 10GBASE-R PCS and 4B alignment, there are several block types that can carry ordered sets:

Input Data	Sync	Block Payload							
Bit Position: / Data Block Format:	0 1	2							65
$D_0 D_1 D_2 D_3/D_4 D_5 D_6 D_7$	01	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		Block Type Field							
$C_0 C_1 C_2 C_3/C_4 C_5 C_6 C_7$	10	0x1e	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$C_0 C_1 C_2 C_3/O_4 D_5 D_6 D_7$	10	0x2d	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
$C_0 C_1 C_2 C_3/S_4 D_5 D_6 D_7$	10	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
$O_0 D_1 D_2 D_3/S_4 D_5 D_6 D_7$	10	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
$O_0 D_1 D_2 D_3/O_4 D_5 D_6 D_7$	10	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
$S_0 D_1 D_2 D_3/D_4 D_5 D_6 D_7$	10	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7
$O_0 D_1 D_2 D_3/C_4 C_5 C_6 C_7$	10	0x4b	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
$T_0 C_1 C_2 C_3/C_4 C_5 C_6 C_7$	10	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0 T_1 C_2 C_3/C_4 C_5 C_6 C_7$	10	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0 D_1 T_2 C_3/C_4 C_5 C_6 C_7$	10	0xaa	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0 D_1 D_2 T_3/C_4 C_5 C_6 C_7$	10	0xb4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0 D_1 D_2 D_3/T_4 C_5 C_6 C_7$	10	0xcc	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0 D_1 D_2 D_3/D_4 T_5 C_6 C_7$	10	0xd2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0 D_1 D_2 D_3/D_4 D_5 T_6 C_7$	10	0xe1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0 D_1 D_2 D_3/D_4 D_5 D_6 T_7$	10	0xff	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

The ‘O’ codes denotes signal ordered set (0xF) vs. sequence ordered sets (0x0).

Though signal ordered sets are reserved.

Figure 49–7—64B/66B Block Formats

Ordered Sets

- For 100GBASE-R and 40GBASE-R, the proposal is:

Input Data	Sync	Block Payload							
Bit Position: / Data Block Format:	0 1	2							65
$D_0 D_1 D_2 D_3/D_4 D_5 D_6 D_7$	01	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		Block Type Field							
$C_0 C_1 C_2 C_3/C_4 C_5 C_6 C_7$	10	0x1e	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$S_0 D_1 D_2 D_3/D_4 D_5 D_6 D_7$	10	0x78	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$O_0 D_1 D_2 D_3/D_4 D_5 D_6 D_7$	10	0x4b	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$T_0 C_1 C_2 C_3/C_4 C_5 C_6 C_7$	10	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0 T_1 C_2 C_3/C_4 C_5 C_6 C_7$	10	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0 D_1 T_2 C_3/C_4 C_5 C_6 C_7$	10	0xaa	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0 D_1 D_2 T_3/C_4 C_5 C_6 C_7$	10	0xb4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0 D_1 D_2 D_3/T_4 C_5 C_6 C_7$	10	0xcc	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0 D_1 D_2 D_3/D_4 T_5 C_6 C_7$	10	0xd2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0 D_1 D_2 D_3/D_4 D_5 T_6 C_7$	10	0xe1	D_0	D_1	D_2	D_3	D_4	D_5	C_7
$D_0 D_1 D_2 D_3/D_4 D_5 D_6 T_7$	10	0xff	D_0	D_1	D_2	D_3	D_4	D_5	D_6

A single block type for sequence ordered sets (no ‘O’ code).

If we need to support signal ordered sets use a new block type (0x55).