85.8.4.2 Receiver interference tolerance test at TP3

The receiver interference tolerance tests shall be implemented using the receiver interference tolerance parameters summarized in Table 85–7. The tests are to be applied to all 10GBASE-CR4 or 10GBASE-CR10 lanes. The receiver interference tolerance test at TP3 is similar in basic principle to the test specified in Annex 69A.

Parameter	Test 1 Value	Test 2 Value	Units
Target BER	10^{-12}	10^{-12}	
Minimum fitted insertion loss coefficients	a_1=2.15 a_2=0.78 a_4=0.03	a_1=6.04 a_2=0.94 a_4=0.08	dB /root-GHz dB /GHz dB /GHz^2
Applied SJ[a] (min. peak-to-peak)	'0.115	'0.115	UI
Applied RJ[b] (min. peak-to-peak)	'0.130	'0.130	UI
Applied DCD (min. peak-to-peak)	'0.035	'0.035	UI
Calibrated far-end crosstalk (min. RMS)	'6.0	'2.2	mV
Calibrated ICN (min. RMS) - MDNEXT	'3.7	'3.7	mV

a Applied SJ frequency >15 MHz , specified at TP0
b Applied random jitter at TP0 is specified at 10–12

Notes to reviewer:
Test 1 Calibrated far-end Crosstalk RMS =9.6mV (from Equation 85-81) * 400mV/600mV (to because all Tx's should match amplitude) * .89 (from ratio of sigma nx to total, case G in healey_02_0709 RSSed with 2mV Tx noise from 85.8.3.2

Test 2 Calibrated far-end Crosstalk RMS =4.7mV (from Equation 85-81) * 400mV/600mV (to because all Tx's should match amplitude) * .625 (from ratio of sigma nx to total, case H in healey_02_0709 RSSed with 1mV Tx noise from 85.8.3.2

85.8.4.3 Test setup

The interference tolerance test is performed with the setup shown in Figure 85.X

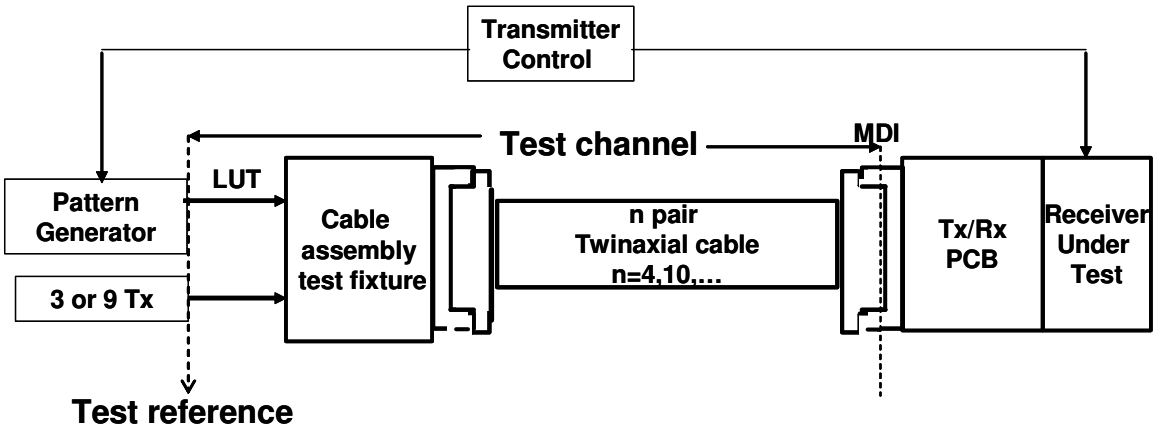

Figure 85.X interference tolerance test setup

85.8.4.4 Test channel

The test channel consists of:

1. A cable assembly
2. A cable assembly test fixture
3. A connecting path from the pattern generator to the cable assembly test fixture receiver lane under test.

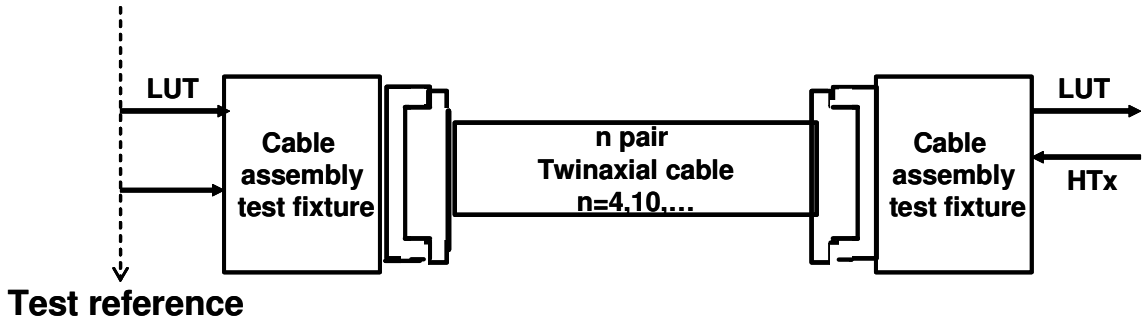

Figure 85.XX Test channel

85.8.4.4.1 Test channel calibration

The insertion loss, near-end integrated crosstalk noise, and far-end crosstalk of the test channels are characterized using the cable assembly test fixtures specified in 85.10.9 as illustrated in Figure-XX. The cable assembly test fixture lanes not under test are terminated in 100 ohms differentially.

The minimum fitted insertion loss coefficients of the lane under test (LUT), derived using the fitting procedure in 85.10.9, shall meet the test values in Table 85–7. It is recommended that the deviation between the insertion loss and the fitted insertion loss be as small as practical and that the fitting parameters be as close as practical to the values given in Table 85-7.

The MDNEXT is measured from points HTx to point LUT in Figure 85-XX. The RMS value of the integrated MDNEXT crosstalk noise, determined using Equation (85–29) through Equation (85–33), shall meet the test values in Table 85–7.

Note to reviewers: the number 3.7 mV =4.7mV (from Equation 85-81) * sqrt(1- .625^2 (from ratio of sigma nx to total, case H in healey_02_0709 RSSed with 1mV Tx noise from 85.8.3.2))

The far-end crosstalk disturbers consist of 40GBASE-CR4 or 100GBASE-CR10 transmitters. It is recommended that the transition time, equalization setting, and path from the far-end crosstalk disturbers to the cable assembly test fixture emulate the pattern generator as much as practical. . For 40GBASE-CR4 test channels, the crosstalk that is coupled into a receive lane is from three transmitters. For 100GBASE-CR10 test channels, the crosstalk that is coupled into a receiver lane is from nine transmitters. The disturber transmitters send either scrambled idle codes or PRBS31. The amplitudes of each the disturbers should not deviate more than 3 dB from the mean of the disturber amplitudes. The amplitudes of the disturbers should be such that the calibrated far-end crosstalk in Table 85-7 is met in the calibration setup at the lane under test (LUT) point with no signal applied at pattern generator connection (PGC), and host transmitter (HTx) and PGC terminated

85.8.4.5 Pattern generator

The Pattern generator transmits data to the device under test. Its output amplitude shall be no more than 800mV p-p differential when measured on an alternating one zero pattern. Its rise and fall times should be no less than 47ps. If the rise and fall times are less than 47ps the value of a_4 in Table 85-7 is increased by:

$$a_4 = 6.8 \times 10^{-6} \cdot (47^2 - Tr^2)$$

Tr in ps

The Pattern generator shall meet the jitter specification in Table 85-7.
The output waveform of the pattern generator shall comply to 72.7.1.11.

85.8.4.6 Transmitter control

For 40GBASE-CR4 or 100GBASE-CR10 testing, the pattern generator is controlled by transmitter control. Transmitter control responds to inputs from the receiver to adjust the equalization of the pattern generator. The receiver may communicate through its associated transmitter, using the protocol described in 72.6.10, or by other means.

85.8.4.7 Test procedure

For 40GBASE-CR4 or 100GBASE-CR10 testing, the pattern generator is first configured to transmit the training pattern defined in 72.6.10.2. During this initialization period, the device under test (DUT) configures the pattern generator equalizer, via transmitter control, to the coefficient settings it would select using the protocol described in 72.6.10 and the receiver will be tuned using its optimization method.

After the pattern generator equalizer has been configured and the receiver tuned, the pattern generator is set to transmit either test patterns 2 or 3 as defined in 52.9.1.1. The receiver under test shall meet the target BER listed in Table 85–7.

During the tests the disturbers transmit at their calibrated level and all of the transmitters in the host under test transmit either scrambled idle characters or PRBS31, with equalization turned off (preset condition) and largest compliant amplitude available under the test conditions.