CAUI-4 Ad hoc

Ryan Latchman, Mindspeed

Agenda

- Patent Policy: This meeting is an official IEEE ad hoc. Please review the patent policy at the following site prior to the meeting. http://www.ieee802.org/3/patent.html
- Chip-to-chip discussion
  - Slavick_01_121613_caui
  - anslow_01_121613_caui
  - gustlin_01_121613_caui
  - latchman_01_121613

20dB Informative channel update

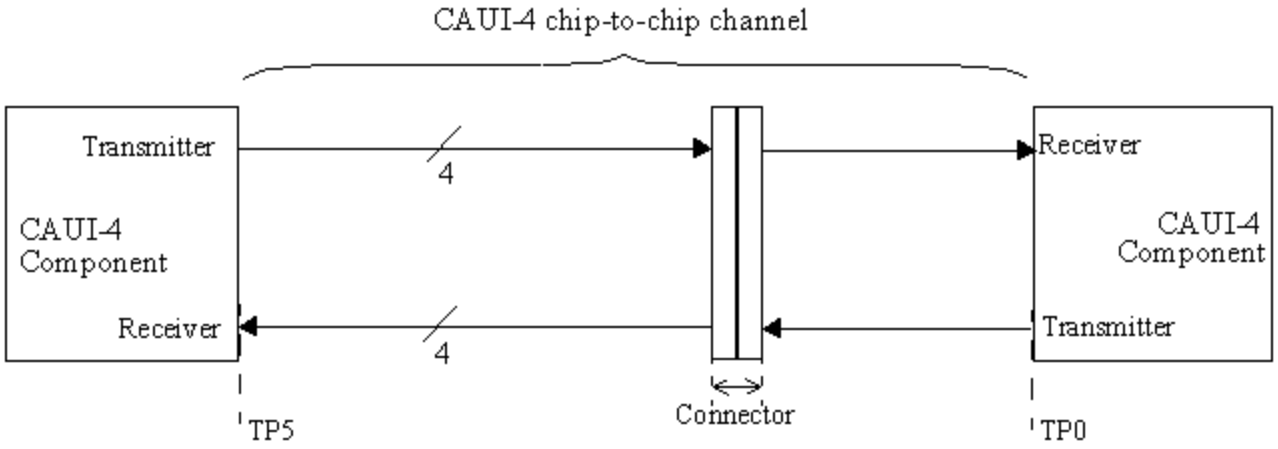

Figure 83D–2—Typical CAUI-4 chip-to-chip application

The normative channel compliance is through CAUI-4 COM as described in 83D.4. Actual channel loss could be higher or lower due to the channel ILD, return loss, and crosstalk.

$$Insertion\_loss(f) \le \begin{cases} 1.083 + 2.543\sqrt{f} + 0.761f & 0.01 \le f < 12.89 \\ -17.851 + 2.936f & 12.89 \le f < 25.78 \end{cases} \quad \text{(dB)} \qquad \text{(83D–1)}$$

Updated Insertion Loss Figure

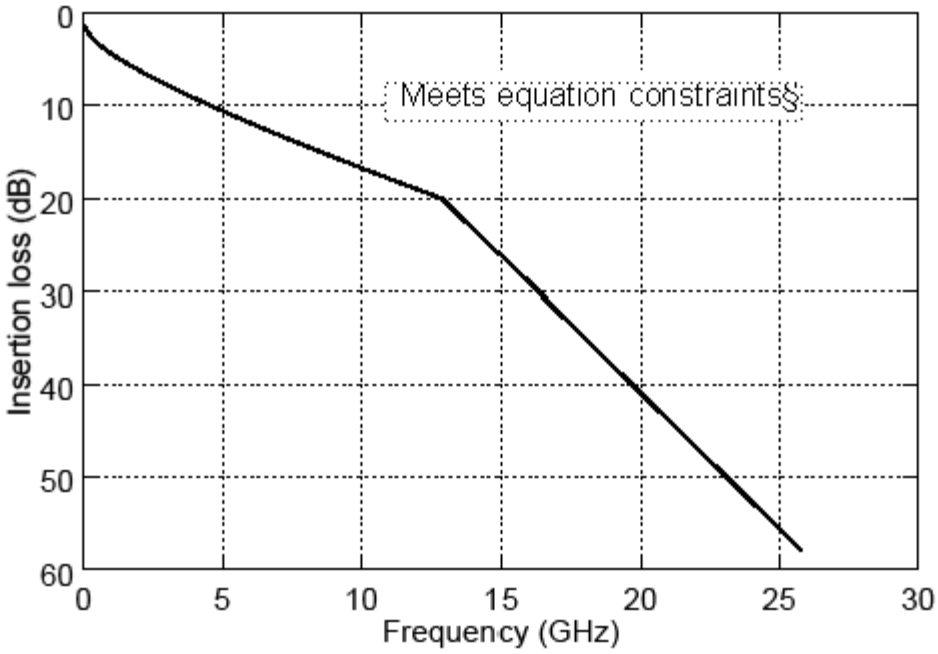

Figure 83D–3—TCAUI-4 chip-to-chip channel insertion loss§

Transmitter

- With addition of DFE, implementation can be more similar to CL93
  - Output waveform
  - Output jitter definition

Transmitter

83D.3 CAUI-4 chip-to-chip electrical characteristics

83D.3.1 CAUI-4 transmitter characteristics

A CAUI-4 chip-to-chip transmitter shall meet the specifications defined in Table 83D–1 when measured at TP0a. While the CAUI-4 chip-to-chip transmitter requirements are similar to those in Clause 93, they differ in that they do not assume transmitter training or a back-channel communications path. Also, the transmit output waveform is not manipulated via a PMD control function (see 93.7.12).

A test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for all transmitter signal measurements, unless otherwise specified.

83D.3.2 CAUI-4 receiver characteristics

A CAUI-4 chip-to-chip receiver shall meet the specifications defined in Table 83D–2 when measured at TP5a.

Transmitter

Table 83D–1—CAUI-4 transmitter characteristics at TP1a

Parameter	Subclause reference	Value	Units
Signaling rate per lane (range)	93.8.1.2	25.78125 ± 100 ppm	GBd
Differential peak-to-peak output voltage (max) Transmitter disabled Transmitter enabled	93.8.1.3	 30 1200	 mV mV
Common-mode voltage (max)	93.8.1.3	1.9	V
Common-mode voltage (min)	93.8.1.3	0	V
Common-mode AC output voltage (max, RMS)	93.8.1.3	12	mV
Differential output return loss (min)	93.8.1.4	Equation (93-3)	dB
Common-mode output return loss (min)	93.8.1.4	Equation (93-4)	dB
Output waveform[a] Steady state voltage v_f (max) Steady state voltage v_f (min) Linear fit pulse peak (min) Normalized coefficient step size (min) Normalized coefficient step size (max) Pre-cursor full scale range (min) Post-cursor full scale range (min)	93.8.1.5	 0.6 0.4 0.71 x v_{f1} 0.0083 0.05 1.54 4	 V V V — — — —
Signal-to-noise-and-distortion ratio (min)	93.8.1.6	27	dB
Output Jitter (max) Even-odd jitter Effective bounded uncorrelated jitter, peak-to-peak Effective random jitter, RMS	93.8.1.7	 0.035 0.1 0.01	 UI UI UI

[a]State of the transmit equalizer is controlled by management interface.

Interference Tolerance

Table 83D–2—CAUI-4 receiver characteristics at TP5a

Parameter	Subclause reference	Value	Units
Differential input return loss (min)		Equation (93-3)	dB
Differential to common mode input return loss		Equation (93-5)	dB
Interference tolerance	83D.3.2.1	Table 83D–3	—

83D.3.2.1 Receiver interference tolerance

The receiver shall satisfy the requirements for interference tolerance defined in Table 83D–3. The interference tolerance test leverages the test setup and method described in 93.8.1.7 using the parameters defined in Table 83D–3.

Table 83D–3—Receiver interference tolerance parameters

Parameter	Test 1 values		Test 2 values		Units
	Min	Max	Min	Max	
Bit error ratio[a]	—	10^{-15}	—	10^{-15}	—
Insertion loss at 12.89 GHz[b]	—	20	—	10	dB
Coefficients of fitted insertion loss[c] a_0 a_1 a_2 a_4	 -1 0 0 0	 2 14.914 41.228 19.728			 dB dB/GHz$^{1/2}$ dB/GHz dB/GHz^2
RSS_DFE	0.05	—	0.05	—	—
COM including effects of broadband noise	—	2	—	2	dB

[a] Bit error ratio replaces the RS symbol error ratio measurement in 93.8.1.7.
[b] Measured between TPt and TP5 (see Figure 93C-4).
[c] Coefficients are calculated from the insertion loss measured between TPt and TP5 (see Figure 93C-4) using the method in 93A.3 with f_{min} = 0.05 GHz and f_{max} = 25.78125 GHz, and maximum Δf = 0.01 GHz.

COM

83D.4 CAUI-4 chip-to-chip channel characteristics

The channel operating margin (COM) computed using the procedure in Annex 93A (with the exception that the continuous time filter (CTLE) is as defined in Equation (83D–2) and with coefficients given in Table 83D–7) and the parameters in Table 83D–4 shall be greater than or equal to 2 dB using any combination of discrete transmit equalizer and continuous time filter shown in Table 83D–4. This minimum value allocates margin for practical limitations on the receiver implementation as well as the allowed transmitter equalization settings.

Table 83D–4—Channel operating margin parameters

Parameter	Symbol	Value	Units
Signaling rate	f_b	25.78125	GBd
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Transmitter package model Single-ended device capacitance Transmission line length Single-ended board capacitance	 C_{dt} z_{pt} C_{bt}	 2.5×10^{-4} 12 1.8×10^{-4}	 nF mm nF
Receiver package model Single-ended device capacitance Transmission line length Single-ended board capacitance	 C_{dr} z_{pr} C_{br}	 2.5×10^{-4} 12 1.8×10^{-4}	 nF mm nF
Single-ended reference resistance	R_o	50	ohms
Single-ended termination resistance	R_d	55	ohms
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz

COM

Table 83D–4—Channel operating margin parameters (*continued*)

Parameter	Symbol	Value	Units
Transmitter equalizer, pre-cursor coefficient	$c(-1)$, $c(0)$, $c(1)$	Table 83D–5	
Transmitter equalizer, post-cursor coefficient	$c(-1)$, $c(0)$, $c(1)$	Table 83D–6	
Continuous time filter, DC gain	*CTLE*	Equation (83D–2) Table 83D–7	dB dB dB
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.4 0.4 0.6	 V V V
Number of signal levels	L	2	—
Level separation mismatch ratio	R_{LM}	1	
Transmitter signal to noise ratio	SNR_{TX}	27	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	5	UI
Normalized DFE coefficient magnitude limit	b_{max}	0.3	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.05	UI

COM

One-sided noise spectral density§	η_{0}§	5.2×10^{-4}§	V^2/GHz§
Target detector error ratio§	DER_{0}§	10^{-15}§	—§

¶

Table 83D–5—Transmit equalizer pre-cursor coefficients§

Pre-cursor equalization setting§	c(-1)§	c(0)§	c(1)§
0§	0§	1§	0§
1§	–0.05§	0.95§	0§
2§	–0.1§	0.9§	0§
3§	–0.15§	0.85§	0§

Table 83D–6—Transmit equalizer post-cursor coefficients§

Post-cursor equalization setting§	c(-1)§	c(0)§	c(1)§
0§	0§	1§	0§
1§	0§	0.95§	–0.05§
2§	0§	0.9§	–0.1§
3§	0§	0.85§	–0.15§
4§	0§	0.8§	–0.2§
5§	0§	0.75§	–0.25§

¶

$$H(f) = \frac{GP_1P_2}{Z_1} \times \frac{j2\pi f + Z_1}{(j2\pi f + P_1)(j2\pi f + P_2)} \quad (83D\text{–}2)$$

where

$H(f)$	is the CTLE transfer function
G	is the CTLE gain
P_1, P_2	are the CTLE poles in Grad/s
Z_1	is the CTLE zero in Grad/s
j	is the square root of –1
f	is the frequency in GHz

Table 83D–7—Reference CTLE coefficients

Peaking (dB)	G	$\frac{P_1}{2\pi}$	$\frac{P_2}{2\pi}$	$\frac{Z_1}{2\pi}$
1	0.89125	18.6	14.1	8.364
2	0.79433	18.6	14.1	7.099

COM

Table 83D–7—Reference CTLE coefficients§

Peaking (dB)§	G§	$\frac{f_{P1}}{2\pi}$§	$\frac{f_{P2}}{2\pi}$§	$\frac{f_{Z1}}{2\pi}$§
3§	0.70795§	15.6§	14.1§	5.676§
4§	0.63096§	15.6§	14.1§	4.9601§
5§	0.56234§	15.6§	14.1§	4.358§
6§	0.50119§	15.6§	14.1§	3.844§
7§	0.44668§	15.6§	14.1§	3.399§
8§	0.39811§	15.6§	14.1§	3.012§
9§	0.35481§	15.6§	14.1§	2.672§
10§	0.31623§	15.6§	14.1§	2.3728§
11§	0.28184§	15.6§	14.1§	2.109§
12§	0.25119§	15.6§	14.1§	1.8755§

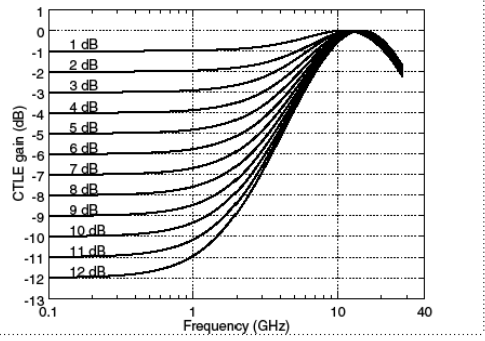

Figure 83D–4—Selectable continuous time linear equalizer (CTLE) characteristic§