

CAUI-4 Ad hoc January 6th Minutes

Minutes

- Patent Policy: This meeting is an official IEEE ad hoc. Please review the patent policy at the following site prior to the meeting.
<http://www.ieee802.org/3/patent.html>
- Chip-to-chip comment discussion
 - Comment 52 – 10dB channel support
 - Request commenter to present justification for two chip-chip interfaces
 - Comment 36 – Transmit Equalizer Values
 - Use current discrete settings
 - Comment 37 – Receiver characteristics
 - Add jitter tolerance
 - MTTFPA:
 - gustlin_01_010614_CAUI
 - ran_01_010614_CAUI4
 - slavick_01_010614_CAUI
- See next slide for straw poll and results

Straw Poll & Results

- 1) Straw Poll (Chicago Rules):
- I prefer the following solution to address MTTFPA in CAUI-4 chip-to-chip:
 - A) Note in the draft warning users about MTTFPA but not specifying the solution
 - Current note is: Maximum BER assumes errors are not correlated to ensure a sufficiently high mean time to false packet acceptance (MTTFPA) assuming 64B/66B coding. Actual implementation of the receiver is beyond the scope of this standard
 - I would consider Vinu's suggestion to be a modification of this note in relation to the burst error probability.
 - B) Block level muxing per gustlin_01_010614_CAUI
 - C) Modification to the 100G PCS.
 - D) Leverage SR FEC
 - E) Leverage low latency FEC per slavick_01_010614_CAUI
- 2) Straw Poll (one vote only):
- I prefer the following solution to address MTTFPA in CAUI-4 chip-to-chip:
 - A) Note in the draft warning users about MTTFPA but not specifying the solution
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Results

Chicago Rules	# of Votes
A) Note in the draft warning users about MTTFPA but not specifying the solution	16
B) Block level muxing per gustlin_01_010614_CAUI	12
C) Modification to the 100G PCS.	2
D) Leverage SR FEC	3
E) Leverage low latency FEC per slavick_01_010614_CAUI	5
Choose 1	# of Votes
A) Note in the draft warning users about MTTFPA but not specifying the solution	12
B) Block level muxing per gustlin_01_010614_CAUI	6
C) Modification to the 100G PCS.	0
D) Leverage SR FEC	3
E) Leverage low latency FEC per slavick_01_010614_CAUI	1