

# PSM4 Technology & Relative Cost Analysis Update

Jon Anderson, Oclaro  
Kiyoo Hiramoto, Oclaro

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# Introduction

- This presentation provides an update on the 4x 25 Gb/s parallel single mode (PSM4) technology identified in [anderson\\_01\\_0112](#) which is proposed as a PHY solution for the 500m single mode objective.
- Furthermore, an update on the PSM4 transceiver relative cost analysis given in [anderson\\_01\\_0112](#) is provided. This update is based on PSM4 optical baseline specifications given in [100G PSM4 Link Model Results Comparison, John Petrilla, Dec. 2012](#), presented at the Dec. 4, 2012 IEEE P802.3bm SMF Ad Hoc conference call.
- Conclusion: Our analysis indicates ~60% cost reduction in optical transceiver is achievable with the proposed PSM4 approach, compared with the current 100GBASE-LR4, for < 500m short reach SMF application.

# Outline

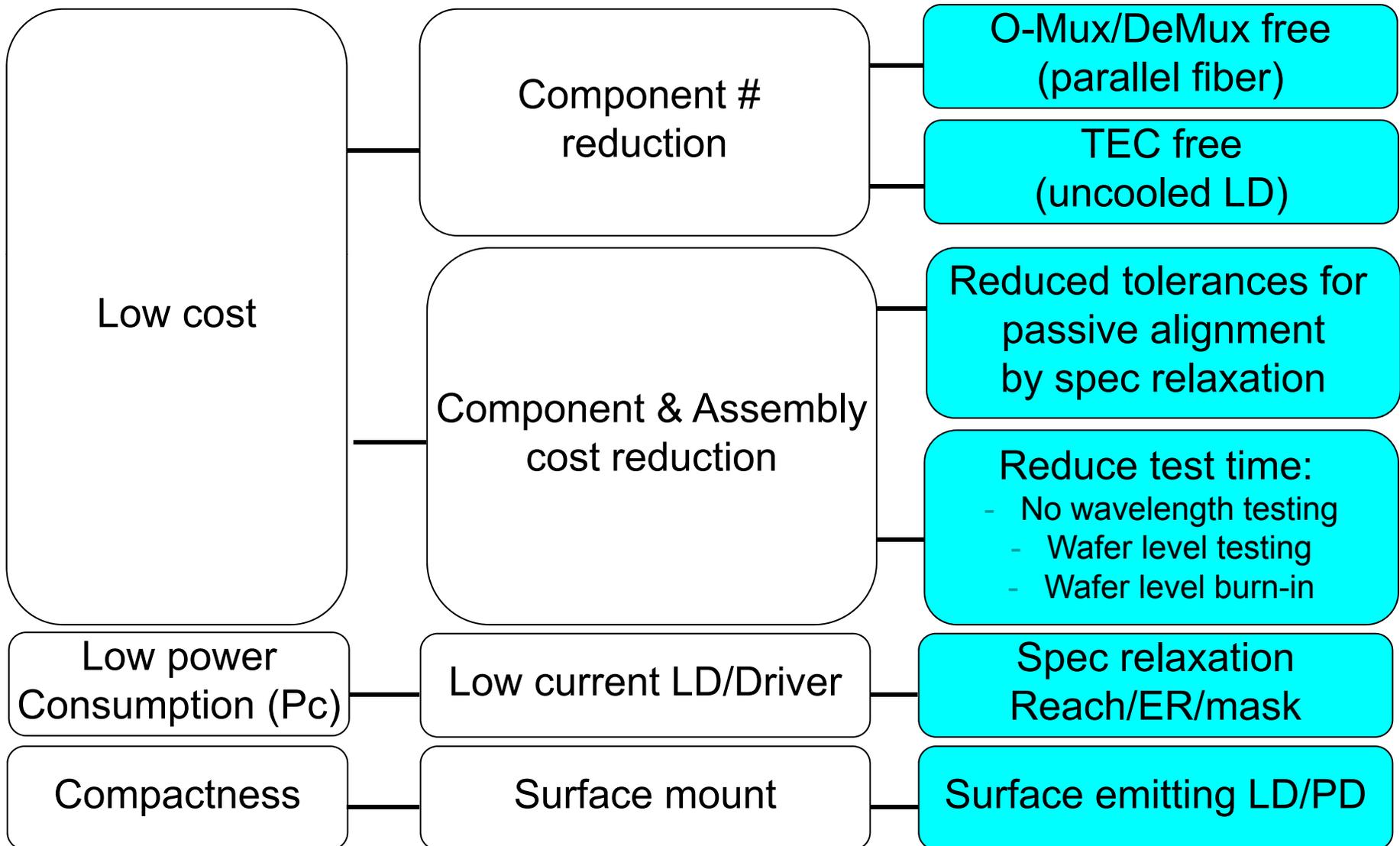
- PSM4 optical transmitter, receiver and transceiver technologies overview
- Key PSM4 technology, assembly and test factors providing cost reduction relative to 100GBASE-LR4 technology
- PSM4 transceiver relative cost analysis
- Summary

# Objectives and Approaches

## Objectives

## Challenges

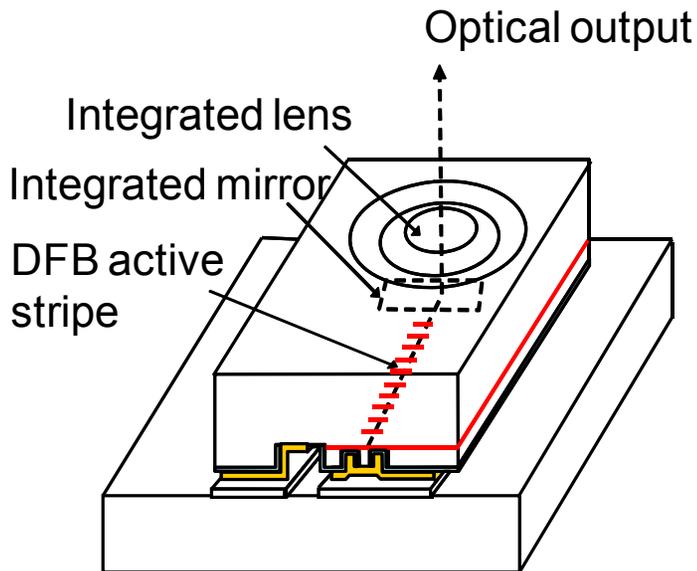
## Approaches



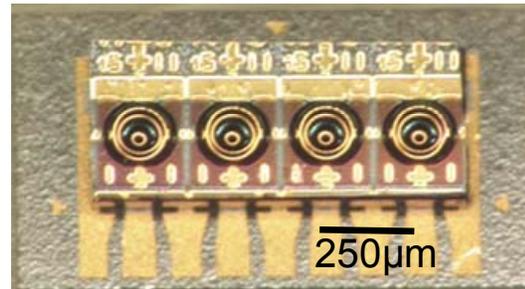
# Lens Integrated Surface Emitting Laser (LISEL)

- 1.3 $\mu\text{m}$  operation with low  $I_{th}$  ( $\sim 15 \text{ mA}$  @85 $^{\circ}\text{C}$ )
- High speed (25Gb/s) up to 100  $^{\circ}\text{C}$
- Surface emitting/ Flip-chip mount
- 2km error free transmission demonstrated

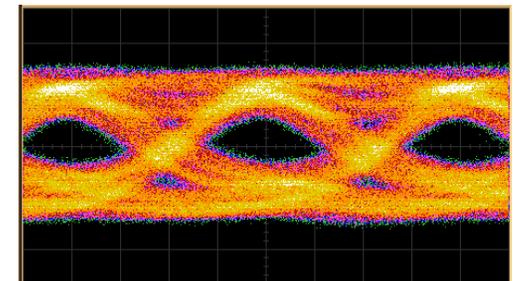
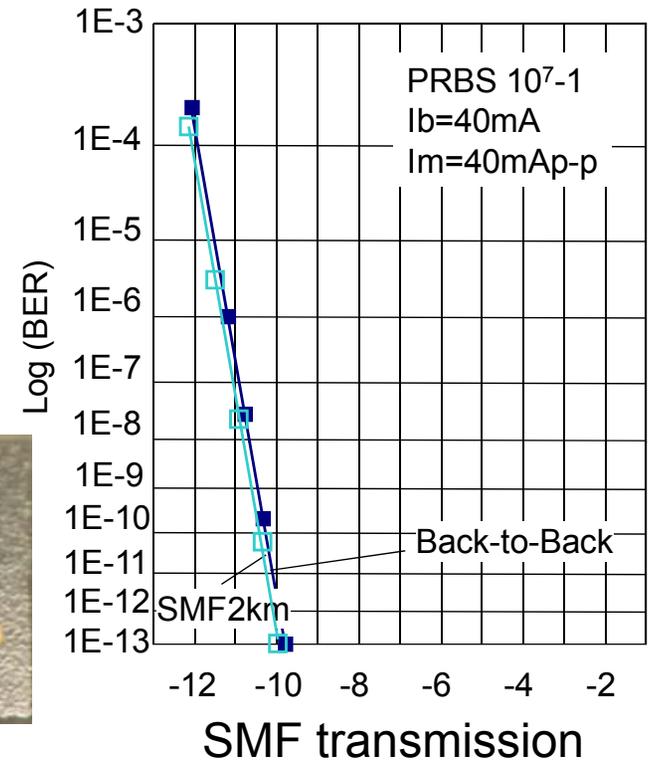
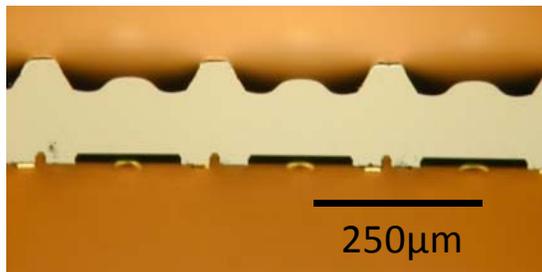
## Structure of LISEL



## 4ch-LISEL array



## Cross section



Eye pattern  
(Back-to-Back) 5

Ref: K. Adachi et al., J. Lightwave Tech. 29, 2899 (2011)  
 A part of this work was performed under management of the PETRA supported by NEDO.  
 18 Dec 2012  
 anderson\_01\_1212\_smf

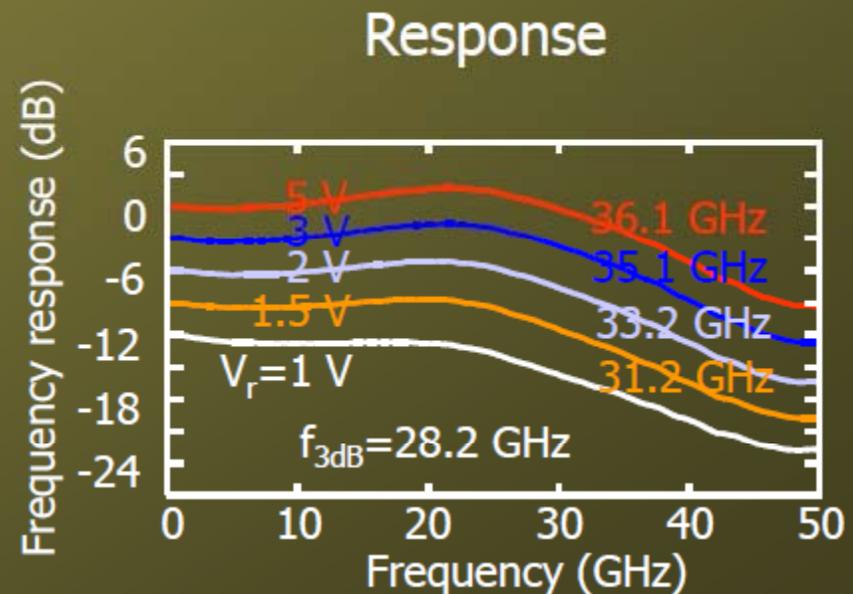
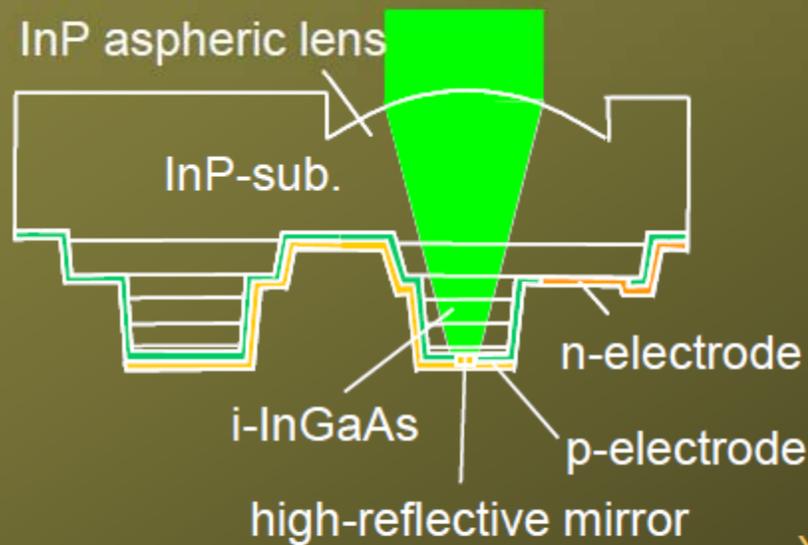
# Lens Integrated Photodiode (LIPD)

- High speed:  $\sim 35\text{GHz}$  ----- Small area p-i-n
- High responsivity:  $>0.8\text{A/W}$  --- High reflect. mirror
- Wide align. tolerance:  $>20\mu\text{m}$  -- Lens integration



(Bottom)

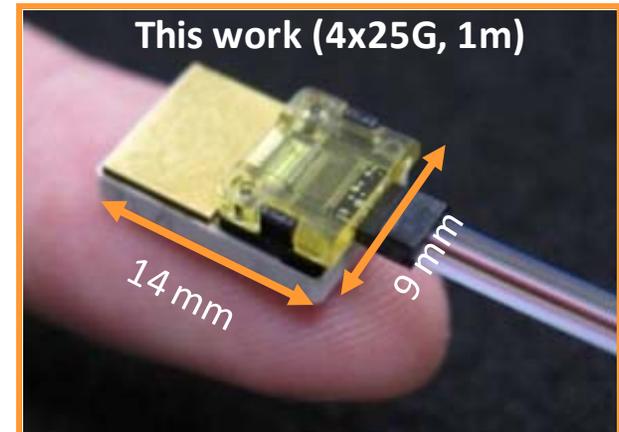
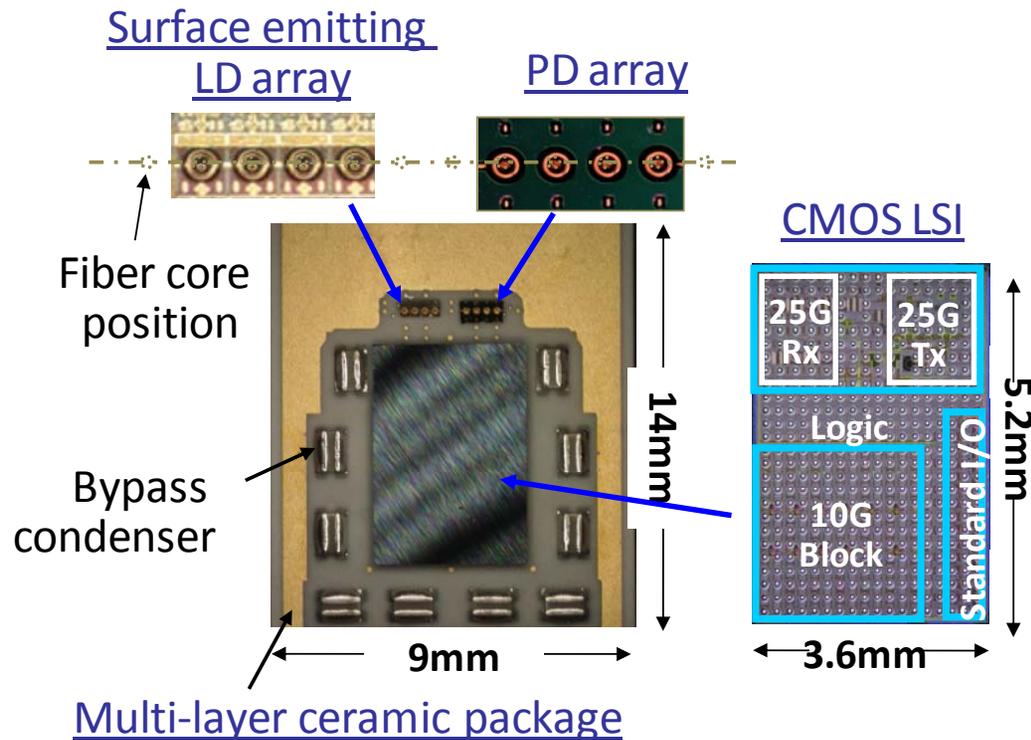
(Surface)



Y. Lee, et al., IEICE Trans. Electron. E94-C, p. 116 (2010)

# PSM4 transceiver

- Surface mount with passive alignment enables low cost module.
- Use of lens-integrated optical devices reduces components and assembly costs in transceiver design.



Foot print : 14 x 9 mm<sup>2</sup> (1/100)  
Power: 2W (1/15)

# Key factors in PSM4 technology for providing cost reduction relative to 100GBASE-LR4.

Factor	Key Differentiation
Reduced Component Count	<ul style="list-style-type: none"> <li>▪ <b>No O-Mux/DeMux</b></li> <li>▪ <b>No TEC</b></li> <li>▪ Integrated lens in LD, PD devices</li> <li>▪ Single chip LD array, PD array</li> </ul>
Reduced Component Cost	<ul style="list-style-type: none"> <li>▪ <b>Spec relaxation, increased yield</b></li> <li>▪ <b>Relaxed alignment tolerances</b></li> <li>▪ <b>1-chip CMOS quad CDR with laser driver array</b></li> <li>▪ <b>Wide spectral range increases LD array yield</b></li> <li>▪ <b>Small sized OSA package w/o O-Mux/DeMux</b></li> </ul>
Reduced Assembly Cost	<ul style="list-style-type: none"> <li>▪ <b>Relaxed tolerances enabling passive optical alignment</b></li> <li>▪ <b>Low assembly cost w/o O-Mux/DeMux</b></li> <li>▪ SMT for optical components</li> </ul>
Reduced Test Cost	<ul style="list-style-type: none"> <li>▪ <b>Wide spectral range eliminates wavelength test</b></li> <li>▪ On-wafer laser, PD testing and burn-in</li> </ul>

# PSM4 Transmitter Optical Sub-Assembly (TOSA) cost analysis, relative to 100G-LR4 and SR4.

100G PMD	Fiber Type	Reach	TOSA		LDD	O-mux	Optic Coupling	Total Rel. Cost
			LD	TEC				
LR4	SMF	10km	Cooled DML	Req	SiGe	Req	Active	1
PSM4	SMF	500m	Surface Emitting DML	NR	CMOS 1-chip CDR	NR	Passive*	0.2
SR4	MMF	100m	VCSEL	NR	CMOS	NR	Passive	<0.2

NR: Not Required

\* Design Target

# PSM4 Receiver Optical Sub-Assembly (ROSA) cost analysis, relative to 100G-LR4 and SR4.

100G PMD	Fiber Type	Reach	ROSA	TIA	O-demux	Optic Coupling	Total Rel. Cost
			PD				
LR4	SMF	10km	PIN	SiGe	Req	Active	1
PSM4	SMF	500m	PIN	CMOS 1-chip CDR	NR	Passive*	0.35
SR4	MMF	100m	PIN	CMOS	NR	Passive	<0.35

NR: Not Required

\* Design Target

# PSM4 transceiver cost analysis, relative to 100GBASE-LR4 and SR4.

<b>Component</b>	<b>100G-LR4</b>	<b>100G-PSM4</b>	<b>100G-SR4</b>
TOSA + LDD + O-mux	1	0.2*	< 0.2*
ROSA + TIA + O-demux	1	0.35	<0.35
CDR IC	1	1	1
MISC: DC-DC, uC, packaging	1	1	1
Assembly & Test	1	1	1
<b>Total</b>	<b>1</b>	<b>0.43</b>	<b>&lt; 0.43</b>

\* Decrease including results from reduced parameter set testing.

# Summary

- An update on the 4x 25 Gb/s parallel single mode (PSM4) technology and relative cost analysis has been presented.
- Relative cost analysis indicates ~60% optical transceiver cost reduction in a short reach 500m SMF link is achievable with the PSM4 approach, compared with the current 100GBASE-LR4.
- Relative link cost analysis is in progress.
- Seeking your:
  - feedback on this analysis,
  - any recommended next steps, and
  - Support!

End of Presentation

Thanks!