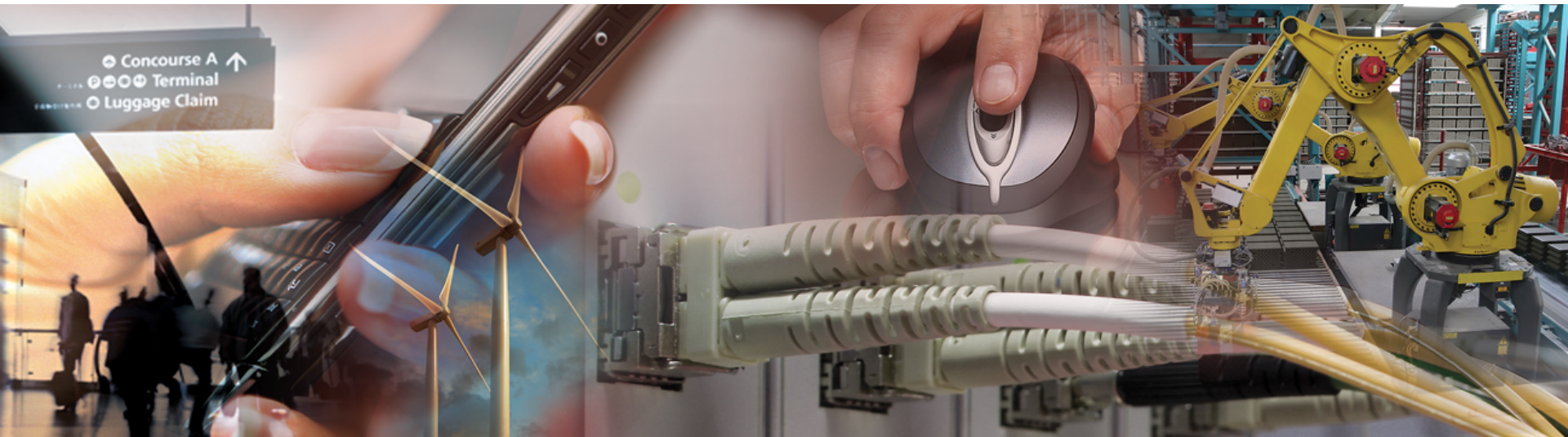


# PMA muxing considerations



**Jeff Slavick**

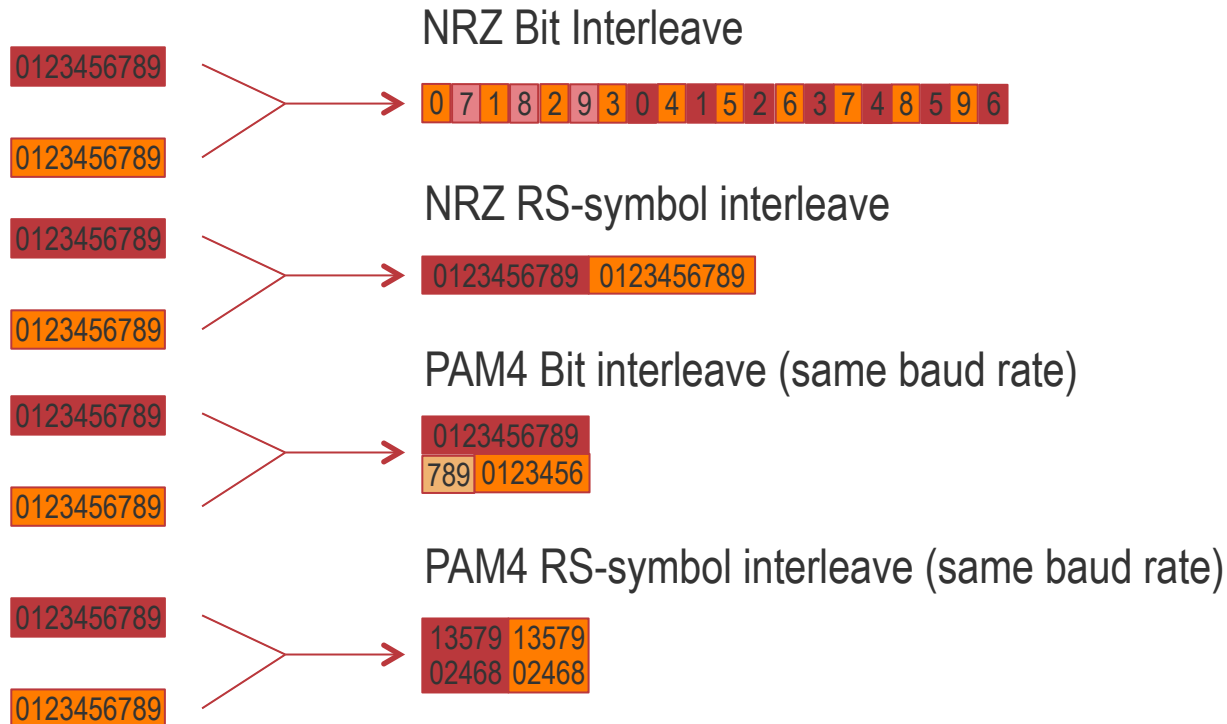
# Supporters

- **Tongtong Wang**
- **Xinyuan Wang**

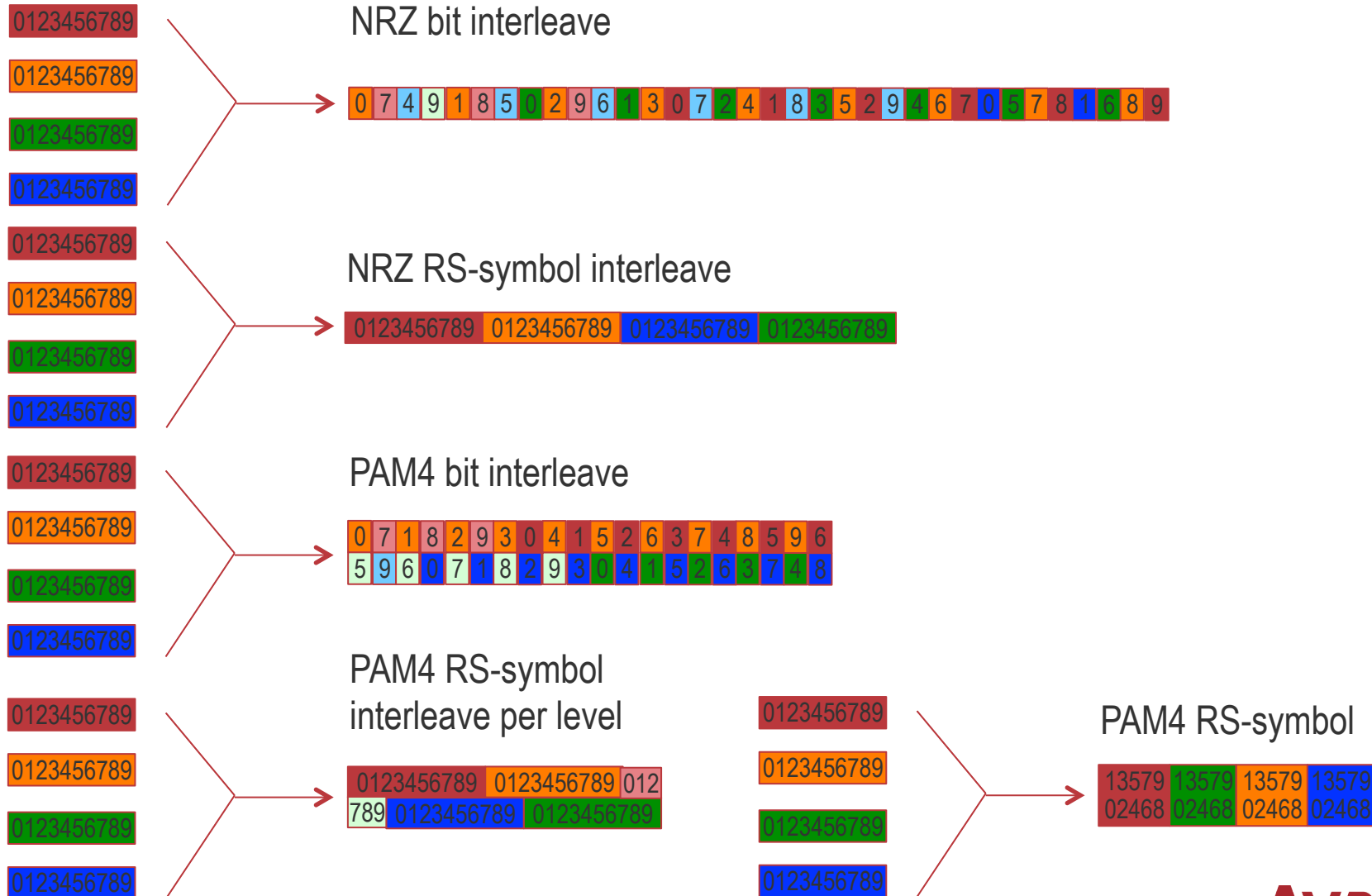
# Assumptions

- **RS-FEC is used (10b RS-symbol)**
- **Gray encoding is used for PAM4 modulations**
  - Single level miss incurs only a single bit error

# Double the data rate



# Quadruple data rate from NRZ



# Error Signatures

- **What do burst errors on a PAM4 link look like?**
  - Are they single level bursts
  - Do they toggle between levels
- **How does this affect the RS-FEC?**

## Single Level burst Error

#1 0 7 1 8 0 1 2 3 4 5 5 2 6

#2 012345678 0 12345 56789

#3 01234567 89  
78 012345 56#4 13579 13579  
01234 5 2468#5 0 7 1 8 2 9 3 0 4 1  
5 9 6 0 1 2 3 4 5 3#6 13579 13579 13579 13579  
02468 0123 45 468 02468

Pattern	Burst Length	Probability of RS FEC symbols in error due to single burst error				
		1	2	3	4	5
NRZ Bit (2 FEC lanes)	2b	100%	100%	-	-	-
	4b	100%	100%	19%	1%	-
	5b	100%	100%	28%	2%	-
	6b	100%	100%	36%	4%	-
NRZ RS (2 FEC lanes)	2b	100%	10%	-	-	-
	4b	100%	30%	-	-	-
	5b	100%	40%	-	-	-
	6b	100%	50%	-	-	-
PAM Bit (2 FEC lanes)	2b (1 level)	100%	10%	-	-	-
	4b (1 level)	100%	30%	-	-	-
	5b (1 level)	100%	40%	-	-	-
	6b (1 level)	100%	50%	-	-	-
PAM RS (2 FEC lanes)	2b (1 level)	100%	20%	-	-	-
	4b (1 level)	100%	60%	-	-	-
	5b (1 level)	100%	80%	-	-	-
	6b (1 level)	100%	100%	-	-	-
PAM Bit (4 FEC lanes)	2b (1 level)	100%	100%	-	-	-
	4b (1 level)	100%	100%	19%	1%	-
	5b (1 level)	100%	100%	28%	2%	-
	6b (1 level)	100%	100%	36%	4%	-
PAM RS (4 FEC lanes)	2b (1 level)	100%	20%	-	-	-
	4b (1 level)	100%	60%	-	-	-
	5b (1 level)	100%	80%	-	-	-
	6b (1 level)	100%	100%	-	-	-

## Burst Error toggling between PAM levels

#3

01234567 89  
78 012345 56

#4

13579 13579  
01234 5 2468

#7

012 23 56789  
78 0 01 345 56

#8

1357 9 23 579  
0246 0 02 345

#9

0 7 1 8 1 2 3 0 4 1  
5 9 6 0 7 1 3 4 5 3

#10

5 9 1 1 2 7 3 1 3 5  
6 8 0 2 4 3 4 5 2 3

Pattern	Burst Length*	Probability of RS FEC symbols in error due to single burst error				
		1	2	3	4	5
PAM Bit (2 FEC lanes)	4b (1 level)	100%	30%	-	-	-
	5b (1 level)	100%	40%	-	-	-
	6b (1 level)	100%	50%	-	-	-
PAM RS (2 FEC lanes)	4b (1 level)	100%	60%	-	-	-
	5b (1 level)	100%	80%	-	-	-
	6b (1 level)	100%	100%	-	-	-
PAM Bit (2 FEC lanes)	4b (2 level)	100%	100%	37%	3%	-
	5b (2 level)	100%	100%	46%	4%	-
	6b (2 level)	100%	100%	55%	5%	-
PAM RS (2 FEC lanes)	4b (2 level)	100%	60%	-	-	-
	5b (2 level)	100%	80%	-	-	-
	6b (2 level)	100%	100%	-	-	-
PAM Bit (4 FEC lanes)	4b (2 level)	100%	100%	100%	100%	-
	5b (2 level)	100%	100%	100%	100%	20%
	6b (2 level)	100%	100%	100%	100%	28%/ 2% (6)
PAM RS (4 FEC lanes)	4b (2 level)	100%	60%	-	-	-
	5b (2 level)	100%	80%	-	-	-
	6b (2 level)	100%	100%	-	-	-



# Error signatures affects

- **NRZ bit interleave has been shown to require a higher BER floor than NRZ RS-symbol interleave in previous presentations to the group.\***
- **PAM bit interleave has higher probabilities of needing 3 and 4 RS-symbols of correction (#7) compared to NRZ bit interleave (#1) when a PAM burst error occurs. This could imply an additional increase in the BER floor to support this type of bit interleave.**

# PMA option 1

- Bit mux always



- Pro – simple
- Con – RS-FEC performance is degraded, increasing required BER floor. Single RS-FEC solution not viable must use a FOM design.

## PMA option 2

- Bit mux when baud rate stays same. RS symbol mux when baud rate changes.



- PRO – simple for NRZ  $\leftrightarrow$  PAM4 transitions at same baud rate. RS-FEC performance degraded (magnitude depends on error signature)
- Con – When baud-rate changes must RS-FEC symbol align
  - I.e. 25G NRZ  $\rightarrow$  100G PAM4 requires alignment, 25G NRZ  $\rightarrow$  50G PAM does not.

# Option 3

- **RS-FEC symbol interleave always**



- **Pro – Best FEC performance, supports both FOM and Single FEC implementations.**
- **Con – All rate changes (data or baud) require alignment to RS-FEC symbols**

# Conclusion

- **Selection of PMA muxing scheme is a tradeoff between**
  - BER operating floor
  - Number of FEC engines
  - Error signature of links
  - RS-FEC symbol framing when lane counts change
- **Option 1 requires more FEC engines and higher BER floor**
- **Option 2 requires symbol framing in some situations with a reduced BER floor**
- **Option 3 requires symbol framing in all situations but the lowest BER floor**