

# 200GbE Logic Baseline proposal

**IEEE P802.3 Next Generation 100 Gb/s Ethernet &  
200 Gb/s Ethernet Study Group**

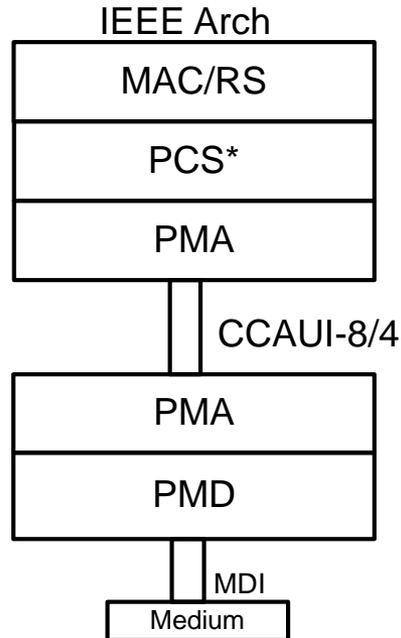
Work in progress  
for  
May 2016

# Introduction

- This looks at baseline proposal for the 200GbE logic layers
- The following assumes reusing the 802.3bs architecture, and that FEC is always required
- Supports 8/4 lanes (25G and 50G)

# PCS Architecture

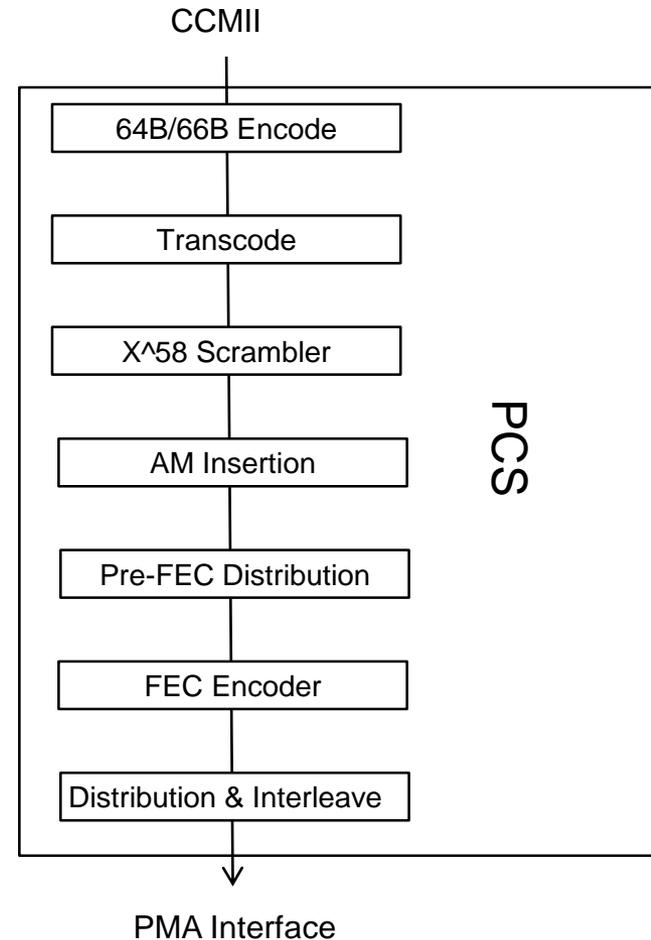
- Based on the current 802.3bs system architecture
- End to end FEC is used, across up to 5 interfaces (located in the PCS sublayer)
- CCMII is an optional interface that is not shown in these figures, but is already adopted and may be present in a given implementation



\*FEC is part of the PCS sublayer

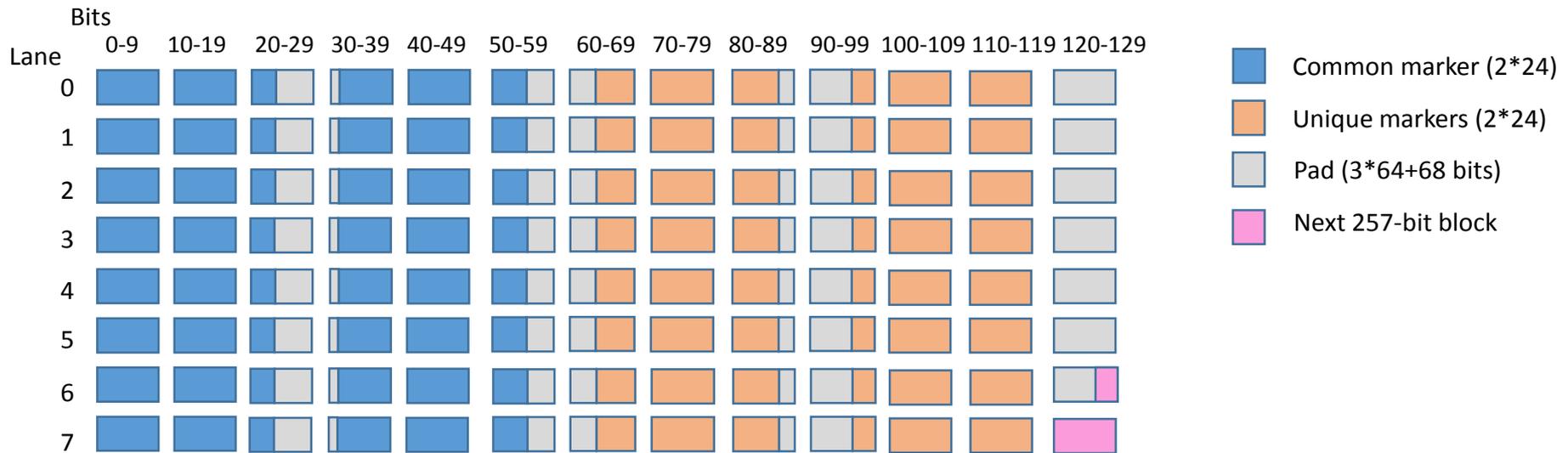
# Possible TX PCS Data Flow

- 64B/66B encode based on clause 82/119
- Transcode to 256B/257B based on clause 119
- Scrambler is located after the Transcoding to simplify the flow, standard X<sup>58</sup> scrambler
- Alignment Markers are the same format as clause 119
- FEC Encoder is RS(544,514,10)
  - Proposed that all FEC processing is as in clause 119, including data distribution and interleaving
- Support for any logical lane on any physical lane

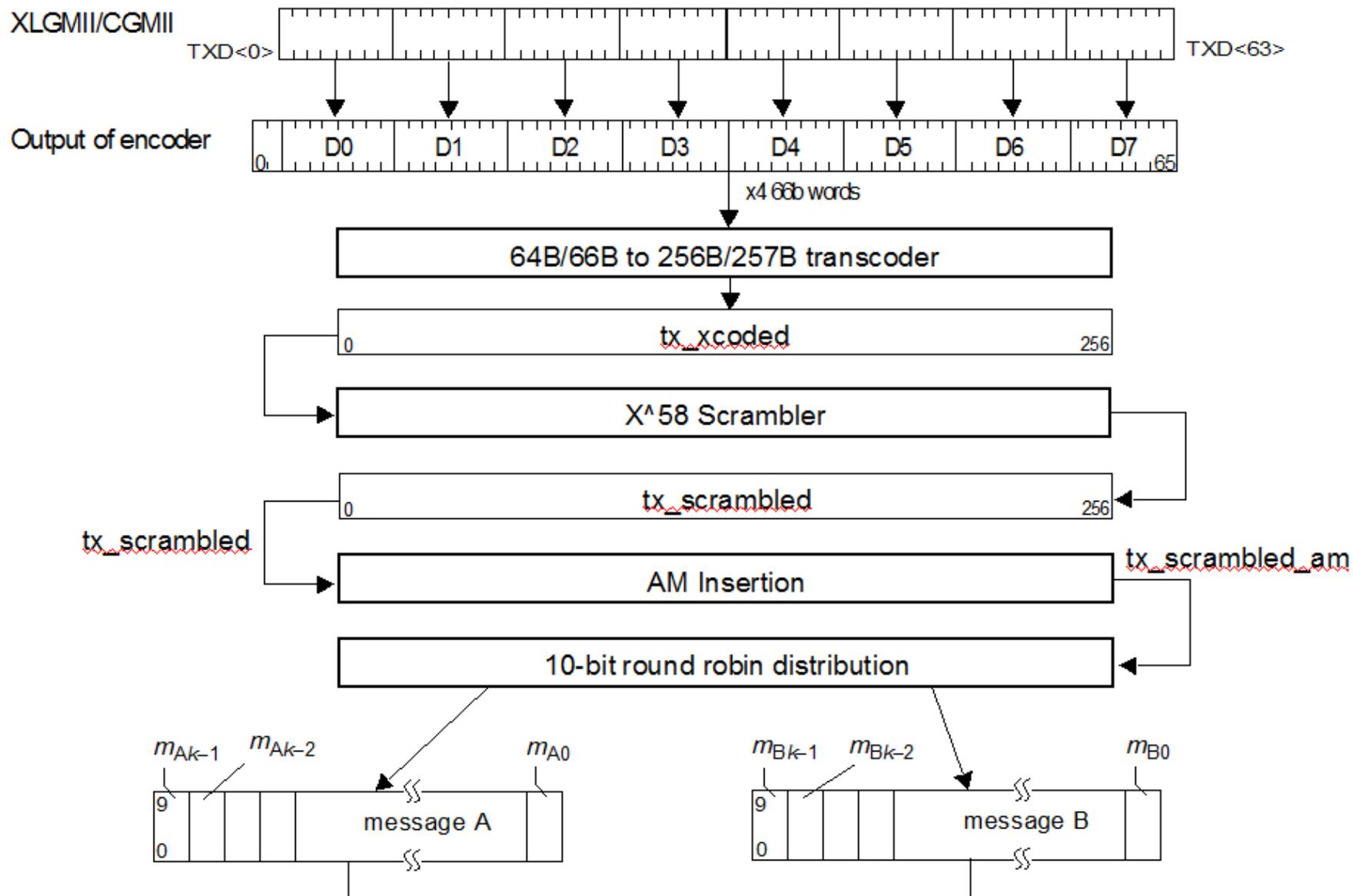


# AM Details

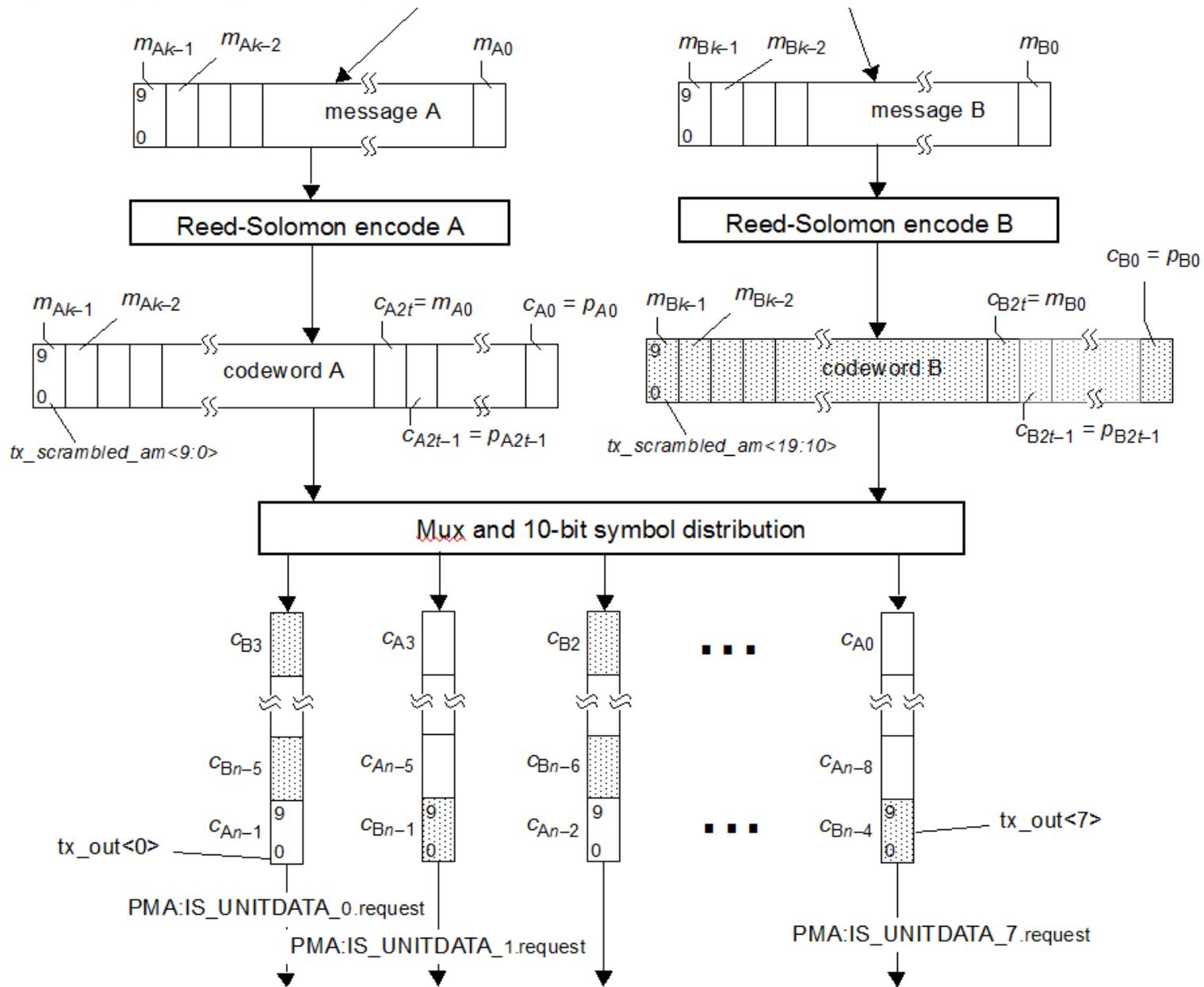
- Similar format to 400GbE
  - 120b AM field per lane with CM0-5 and UM0-5
  - For now use the first 8 AMs from 400GbE
- Distance is ½ that of 400GbE
  - 81920 × 257-bit blocks between AM insertions



# 200GbE Data Distribution Cont



# Distribution Cont



# PMA Functions

- Identical PMA functions as described in clause 120
- Support for bit muxing and any logical lane to any physical lane
- With KP4 FEC the per lane signaling rate is:
  - $544/514 * 257/256 * 25G = 26.5625G$
  - When running 8lanes
  - When running 4 lanes it is 53.125G per lane

# Misc Stuff

- All skew and delay budgets are identical to 400GbE

# Conclusion

- This presentation looks at a baseline PCS/PMA for the 200GbE architecture
- This architecture is feasible, it follows 802.3bs architecture which has been shown to be technically feasible
- Achievable latency is ~110ns with similar performance/gain as 400GbE

**Thanks!**