

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 99 SC P1 L 24 # 167
 Zimmerman, George CME Consulting

Comment Type ER Comment Status D Front Matter

(to minimize comments, all related front matter stuff is here)
 Page 1 line 24: Need to fill in purpose of amendment from PAR,
 Page 1 line 25: status as "Task Force Review".
 Page 2, abstract and keywords.
 Page 3, line 36, this is 802.3bt-20XX
 Page 4 line 27, this is 802.3bt-20XX
 Page 4 line 28, include a brief summary of the changes, generally aligned with the PAR.

SuggestedRemedy

See comment

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 33 SC 33.3.7.3 P 90 L 43 # 41
 Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Yair3

The following comment addresses linrush in Table 33-11 item 5a and PD Cport max to be supported by PSE linrush. Since both parameters are tied together, they are addressed at the same comment.
 See details in darshan_03_0915.pdf titled: Type 3 and 4 linrush for proposed solution that is a compromise for moving the standard forward.

SuggestedRemedy

See details in darshan_03_0915.pdf.

Proposed Response Response Status W

Wait for presentation.

Cl 1 SC 1.4.415 P 97 L 8 # 211
 Dwelley, David Linear Technology

Comment Type TR Comment Status D Definitions

Page number is from 802.3bx D3.2

The Type 1 PD definition in Clause 1 is broken:
 "1.4.415 Type 1 PD: A PD that does not provide a Class 4 signature during Physical Layer classification (see IEEE 802.3, Clause 33)."

Type 1 PSE and Type 2 definitions appear to be OK.

SuggestedRemedy

Change to:

"1.4.415 Type 1 PD: A PD that provides a Class 0, 1, 2 or 3 signature during Physical Layer classification (see IEEE 802.3, Clause 33)."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

This definition needs to be updated, but the suggested remedy can also describe a Type 3 PD.

Change to:

"1.4.415 Type 1 PD: A PD that provides a Class 0, 1, 2 or 3 signature during Physical Layer classification (see IEEE 802.3, Clause 33)."

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Cl 1 SC 1.4 P97 L 17 # 212
 Dwelley, David Linear Technology

Comment Type TR Comment Status D Definitions

Page number is from 802.3bx D3.2

Definitions for Type 3 and Type 4 PDs and PSEs are missing.

SuggestedRemedy

Add definitions:

Type 3 PD: A PD that provides a Class 6 or lower signature during Physical Layer classification, understands multiple-Event classification, and is capable of Data Link Layer classification (see IEEE 802.3, Clause 33).

Type 3 PSE: A PSE that supports PD Types 1-3 and supports Low MPS.

Type 4 PD: A PD that provides a Class 7 or 8 signature during Physical Layer classification, understands multiple-Event classification, and is capable of Data Link Layer classification (see IEEE 802.3, Clause 33).

Type 4 PSE: A PSE that supports PD Types 1-4 and supports 4-pair power and Low MPS.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

These definitions aren't perfect, but should be included so people can comment on them.

Add definitions:

Type 3 PD: A PD that provides a Class 6 or lower signature during Physical Layer classification, implements multiple-Event classification, and is capable of Data Link Layer classification (see IEEE 802.3, Clause 33).

Type 3 PSE: A PSE that supports PD Types 1-3 and supports Low MPS.

Type 4 PD: A PD that provides a Class 7 or 8 signature during Physical Layer classification, implements multiple-Event classification, and is capable of Data Link Layer classification (see IEEE 802.3, Clause 33).

Type 4 PSE: A PSE that supports PD Types 1-4 and supports 4-pair power and Low MPS.

Cl 1 SC 1.4.425 P97 L 40 # 213
 Dwelley, David Linear Technology

Comment Type TR Comment Status D Definitions

Page number is from 802.3bx D3.2

The Vpd and Vpse definitions in Clause 1 are 2-pair centric:

"1.4.425 VPD: The voltage at the PD PI measured between any conductor of one power pair and any conductor of the other power pair (see IEEE 802.3, Clause 33).

1.4.426 VPSE: The voltage at the PSE PI measured between any conductor of one power pair and any conductor of the other power pair (see IEEE 802.3, Clause 33)."

SuggestedRemedy

Adjust to support 4-pair operation:

"1.4.425 VPD: The voltage at the PD PI measured between any conductor of a positive power pair and any conductor of the matching negative power pair (see IEEE 802.3, Clause 33).

1.4.426 VPSE: The voltage at the PSE PI measured between any conductor of a positive power pair and any conductor of the matching negative power pair (see IEEE 802.3, Clause 33)."

Proposed Response Response Status W

PROPOSED ACCEPT.

Need to make sure these terms have not been changed to -2p.

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Cl 33 SC 33.1.4 P 198 L 8 # 228
 Schindler, Fred Seen Simply

Comment Type **TR** Comment Status **X** Cabling

Changes to the text,
 "A power system consists consisting of a single PSE, link segment, and a single PD, and the link section connecting them. "
 have changed legacy requirements.

1.4.241 link section: The portion of the link from the PSE to the PD.
 1.4.242 link segment: The point-to-point full-duplex medium connection between two and only two Medium Dependent Interfaces (MDIs).

We had a "link segment" that changed to "link section", which removes that requirement that a full-duplex medium be used.

SuggestedRemedy

The Task Force should discuss these implications. The preferred solution is to replace "link section" with "link segment".

Proposed Response Response Status **W**

Task Force to discuss.

Cl 33 SC 33.1.4 P 198 L 26 # 43
 Maguire, Valerie Siemon

Comment Type **ER** Comment Status **D** Cabling

Missing TIA reference in 4 locations in Table 33-1.

SuggestedRemedy

For Type 1, change,

"Class D recommended"

to,

"Class D or Category 5 recommended"

For Type 2, change,

"Class D (ISO/IEC 11801:1995)"

to,

"Class D (ISO/IEC 11801:1995) or Category 5 (ANSI/EIA/TIA-568-A:1995)"

For Type 3, change

"Class D (ISO/IEC 11801:2002)"

to,

"Class D (ISO/IEC 11801:2002) or Category 5e (ANSI/TIA-568-B.2:2001)"

For Type 4, change

"Class D (ISO/IEC 11801:2002)"

to,

"Class D (ISO/IEC 11801:2002) or Category 5e (ANSI/TIA-568-B.2:2001)"

Proposed Response Response Status **W**

PROPOSED ACCEPT.

See comment 30.

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Cl 33 SC 33.1.4 P 198 L 29 # 30
 Darshan, Yair Microsemi

Comment Type TR Comment Status D Cabling

Table 33-1, Cable Type for Type 3 and 4 systems.
 If we agree that we want to work with cable instalations that were specified for Type 2 with Type 3 and 4 systems then we need to use Class D (ISO/IEC 11801:1995) for Type 3 and 4 as well.

SuggestedRemedy

1. Change Minimum Cabling Type for Type 3 and 4 to Class D (ISO/IEC 11801:2002) or

Cabling experts to explain the differences between Class D (ISO/IEC 11801:2002) and Class D (ISO/IEC 11801:1995) for group to decide.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment 43

Cl 33 SC 33.1.4 P 198 L 32 # 268
 Jones, Chad Cisco

Comment Type T Comment Status X Cabling

Table 33-1, last row, last coulumn. We may need to adjust the cabling specs for Type 4 systems based on the regulations currently being drafted in the National Electric Code.

SuggestedRemedy

No change to suggest yet. Wanted a placeholder in the comment database to which to attach possible changes devised at the meeting.

Proposed Response Response Status W

Task Force to discuss

Cl 33 SC 33.1.4.1 P 199 L 5 # 19
 Darshan, Yair Microsemi

Comment Type T Comment Status X Cabling

This is my response to comment #4 in D1.1 per Maintenance Request #1271, on behalf of GEOFF THOMPSON, GRACASI S.A./LINEAR TECHNOLOGY.
 I was asked to review it and submit my response.
 Due to the fact that part of the requested is already implemented in clause 33.1.4, I will address only the comment part that addresses clasue 33.1.4.1

SuggestedRemedy

Replace lines 5-12 in page 199 clause 33.1.4.1 from:
 "Type 1 power levels may be transmitted over all specified premises cabling that meets the requirements specified in Table 33-1. Type 2 operation requires Class D, or better, cabling as specified in ISO/IEC 11801:1995, with the additional requirement that channel DC loop resistance shall be 25 .. or less.
 These requirements are also met by Category 5e or better cable and components as specified in ANSI/TIA-568-C.2; or Category 5 cable and components as specified in ANSI/TIA/EIA-568-A. Type 3 and Type 4 operation requires Class D or better cabling as specified in ISO/IEC 11801:2002. These requirements are also met by Category 5e or better cable and components as specified in ANSI/TIA-568-C.2."

To:

The supply of power over the data connection is intended to operate with no additional requirements to the cabling that is normally installed for data usage. This is approximately true but may require some further attention. Power at Type 1 power levels may be transmitted over all specified premises cabling without further restrictions. Higher power levels may require heavier gauge conductors than are found in Class C/Category 3 cabling and (more uncommonly) in some lighter gauge Class D or better cable. The requirements for Type 2 are met by Category 5 or better cable and components as specified in ANSI/TIA/EIA-568-A."

Proposed Response Response Status W

Task Force to discuss.

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Cl 33 SC 33.2.0a P 200 L 28 # 118
 Yseboodt, Lennart Philips

Comment Type T Comment Status D Types

In Table 33-1a we have a column "Number of Pairs used to deliver Power".
 What we really want here is to indicate if the PSE shall, may, or may not support 4P
 powering.
 The difference is in *support* versus *used*.

SuggestedRemedy

- Replace column title by "Support 4-pair power".
- Change content to "No, No, Allowed, Allowed, Yes, Yes"
- Remove note 4 as this clarification is then no longer needed.

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 33 SC 33.2.0a P 200 L 30 # 185
 Johnson, Peter Sifos Technologies

Comment Type E Comment Status D Types

Under the Table 33-1a heading "Number of Pairs use to deliver Power" are values "2-Pair
 Only", etc. Seems like these values need only be "2", "2 or 4", or "4" to be meaningful.

SuggestedRemedy

Change values to "2", "2 or 4", or "4". Furthermore, because footnote 4 uses the term
 "pairsets", and because pairset is now defined in Definitions, it might be even better to
 change column header to "Number of pairsets used to deliver power" and adjust the values
 to "1", "1 or 2", or "2".

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Possible OBE by comment 118.

Cl 33 SC 33.2 P 200 L 34 # 201
 Dwelley, David Linear Technology

Comment Type E Comment Status D Editorial

We changed "2-Event" Classification to "Multiple-Event" Classification a while ago - now "1-
 Event" and "Multiple-Event" don't match well. "Single-Event" fits better.

I recognize that this is changing a long-standing parameter name, but I think the additional
 clarity this change would bring is worth it.

SuggestedRemedy

Change "1-Event" to "Single-Event" throughout the document (first instance at p200 line
 34).

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 33 SC 33.2.0a P 200 L 45 # 269
 Jones, Chad Cisco

Comment Type T Comment Status X Types

Table 3301a. Comment #72 in D1.1 made some unintended changes that cause problems.
 The second column simply states "maximum class supported" and states Class 8. Join this
 with the information in Table 33-3 on page 214 that states Type 4 can have
 class_num_events, of 1,2,4,5 and this implies that we can make a Type 4 Class 0-3
 system. The desire to bring the new features invented for 802.3bt to legacy systems is
 handled by allowing Type 3 systems class_num_events of 1,2,4. extending this to Type 4
 causes a couple of problems:

1. we now have two OPTIONS for new Class 0-3 systems and three total OPTIONS for
 Classes 0-3 systems. to quote Geoff: options bad, standards good.
2. allowing a Type 4 Class 0-3 system implies that you can extend the 'improvements'
 made to T4 to these lower power systems; for instance, a single polarity PSE. We are
 already aware of some problems with legacy devices.

The improvements for Type 4 are easily defended for a high power, engineered system but
 not so easily defended for the low power systems, (see MDI/MDIX addition required in AF
 to gain WG approval).

SuggestedRemedy

Undo the changes made from comment #72 in D1.1. At a minimum, change Table 33-3 on
 page 214, line 39, Type 4 class_num_events from "1,2,4,5" to "5"

Proposed Response Response Status W

Task Force to discuss.

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Cl 33 SC 33.2.0a P 200 L 50 # 136
 Yseboodt, Lennart Philips
 Comment Type **TR** Comment Status **D** Types
 "Type 1 or 2 PDs may be powered using one pairset."
 Any PD may be powered over 2P, not just Type 1 or Type 2 PDs.
 SuggestedRemedy
 Remove sentence.
 Proposed Response Response Status **W**
 PROPOSED ACCEPT.

Cl 33 SC 33.2.0a P 200 L 50 # 189
 Johnson, Peter Sifos Technologies
 Comment Type **T** Comment Status **D** Types
 Footnote 4 should apply to ALL Type-3 PSE's that provide 4-pair powering including those in rows 3 and 4 of the table. Secondly, assuming that we are allowing for Type-3 PSE's that only power 2 pair (to Class 3/4 limit), then Section 33.2.5.6 (4-Pair ID) needs to specify 4-pair PSE's only. Finally, there is a caveat that a Type-3 or Type-4 PSE that is restricted to 1 or 2 event classification by power management will not be able to resolve if a PD is Type-2 versus Type-3 / 4.
 SuggestedRemedy
 Add footnote 4 to wherever "4-Pair" (or 2 pairsets) appears in the table.
 Then modify 33.2.5.6 to start with "Type 3 and Type 4 PSEs that will deliver power on both pairsets shall determine...."
 Change 2nd line of footnote: "Type 1 PDs and Type 2 PDs that have been clearly identified as Type 1 or Type 2 may be powered using one pairset."
 Proposed Response Response Status **W**
 PROPOSED ACCEPT IN PRINCIPLE.
 AIP this part (possible obe by 118):
 Add footnote 4 to wherever "4-Pair" (or 2 pairsets) appears in the table.

 Accept this part:
 Then modify 33.2.5.6 to start with "Type 3 and Type 4 PSEs that will deliver power on both pairsets shall determine...."

 Reject this part as unneeded (Any PD that presents a class signature in the valid range for a Type 1/2 PD may be 2-pair powered):
 Change 2nd line of footnote: "Type 1 PDs and Type 2 PDs that have been clearly identified as Type 1 or Type 2 may be powered using one pairset."

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Cl 33 SC 33.2.4.3 P 209 L 23 # 251
 Dove, Daniel Dove Networking Solut
 Comment Type **TR** Comment Status **X** Pres: SD
 Type 3 and Type 4 PSEs will use Pairset Controllers and this should be identified early in the constant descriptions.
 SuggestedRemedy
 Modify as follows; "The PSE and Pairset Control state diagrams use the following constants. For Type 3 and Type 4 PSEs, each pairset controller will maintain a local copy of each constant"
 Proposed Response Response Status **W**
 Wait for PSE State Diagram Presentations

Cl 33 SC 33.2.3 P 209 L 27 # 184
 Johnson, Peter Sifos Technologies
 Comment Type **TR** Comment Status **D** Types
 "Type 3 and Type 4 PSEs may operate simultaneously on both Alternatives" reads like this is optional when it is not in many cases (Class 5 and above PSE's powering Type 3 and Type 4 PD's) as specified in Table 33-1a.
 SuggestedRemedy
 Change to:
 Type 3 and Type 4 PSEs shall operate both Alternatives simultaneously when powering at Class 5 and above and may operate both Alternatives simultaneously when powering PDs capable of receiving power on both Alternatives.
 Proposed Response Response Status **W**
 PROPOSED ACCEPT IN PRINCIPLE.
 We need to be careful about our desire to put every requirement in every sentence. This sentence is obviously not as specific as later requirements, but the shalls in later requirements would override this may.
 Task Force to discuss.

Cl 33 SC 33.2.3 P 209 L 27 # 138
 Yseboodt, Lennart Philips
 Comment Type **TR** Comment Status **X** Types
 "Type 3 and Type 4 PSEs may operate simultaneously on both Alternatives."
 Conditions apply, this statement is not always true.
 SuggestedRemedy
 "Type 3 and Type 4 PSEs may operate simultaneously on both Alternatives, when the requirements of Section 33.2.5.6 are met."
 Proposed Response Response Status **W**
 See comment 184.

Cl 33 SC 33.2.4.4 P 209 L 36 # 253
 Dove, Daniel Dove Networking Solut
 Comment Type **TR** Comment Status **X** Pres: SD
 New variables to be added
 SuggestedRemedy
 Insert the following; "PS_Det_Fail_A This variable provides an indication from the Pairset A controller that a failure to detect has occurred. PS_Det_Fail_B This variable provides an indication from the Pairset B controller that a failure to detect has occurred.Values: True: The pairset controller has timed out when attempting detection.False: The pairset controller has not timed out when attempting detection."
 Proposed Response Response Status **W**
 Wait for presentation

Cl 33 SC 33.2.4.4 P 209 L 44 # 250
 Dove, Daniel Dove Networking Solut
 Comment Type **ER** Comment Status **X** Pres: SD
 Additional Text required
 SuggestedRemedy
 Insert the following; "For Type 3 and Type 4 PSEs, the PI will consist of either an Alt-A pairset, an Alt-B pairset, or both Alt-A and Alt-B pairsets being controlled by pairset controllers. The pairset controller will utilize timers, variables and functions defined in this subclause as either a single controller, or as two controllers using local instances of each timer, variable and/or function."
 Proposed Response Response Status **W**
 Wait for presentation

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Cl 33 SC 33.2.4.4 P 209 L 49 # 254
 Dove, Daniel Dove Networking Solut

Comment Type TR Comment Status X Pres: SD

PD_4pair_candidate no longer required

SuggestedRemedy

Replace PD_4pair_Candidate with PD_Alt, replace the sentence "This variable is a function of the results of detection, connection_check and an additional 4PID method" with "This variable is a result of the function do_PD_Check." Under Values, delete the text for False and True, and insert the following; "A: The PD is a candidate for accepting power on Alt-A B: The PD is a candidate for accepting power on Alt-B Both: The PD is a candidate for accepting power on both Alt-A and Alt-B simultaneously"

Proposed Response Response Status W

wait for presentation

Cl 33 SC 33.2.4.1 P 210 L 5 # 62
 Yseboodt, Lennart Philips

Comment Type E Comment Status D Editorial

"If a PSE performs detection using Alternative B see 33.2.5.5."

SuggestedRemedy

"If a PSE performs detection using Alternative B see Section 33.2.5.5."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment 202.

Cl 33 SC 33.2.4.1 P 210 L 5 # 270
 Jones, Chad Cisco

Comment Type E Comment Status D Editorial

"If a PSE performs detection using Alternative B (see 33.2.5.5)" This sentence looks lonely, and a lot of unnecessary text. Perhaps it's hard to see all this stuff without the version of the draft that doesn't show the change bars (I will request a clean version of the draft for D1.3 in addition to change bars).

SuggestedRemedy

add "(see 33.2.5.5)" to the end of the previous paragraph and delete this sentence.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment 202.

Cl 33 SC 33.2.4.1 P 210 L 5 # 202
 Dwelley, David Linear Technology

Comment Type E Comment Status D Editorial

We were either too aggressive or not quite aggressive enough cutting text last time: "If a PSE performs detection using Alternative B see 33.2.5.5."

SuggestedRemedy

Either restore the original sentence from D1.1, or kill this sentence entirely and add (see 33.2.5.5) to the end of the previous sentence.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

We removed the sentence in order to not have the same requirement in two places.

Change sentence to:

"If a PSE performs detection using Alternative B see 33.2.5.5. for more information on detection backoff requirements."

Cl 33 SC 33.2.4.1 P 210 L 5 # 187
 Johnson, Peter Sifos Technologies

Comment Type E Comment Status D Editorial

Partially deleted sentence regarding Alt B backoff in presence of open circuit. Was this done as maintenance? (If not, it should have been a maintenance task.) Also, moving to the new clause 33.2.5.5 seems a bit out of place since the topic is clearly about back-off behavior.

SuggestedRemedy

Either delete the sentence in 33.2.4.1 entirely or re-locate 33.2.5.5 clause back to its prior location.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment 202.

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 33 SC 33.2.4.1 P 210 L 5 # 247
 Picard, Jean Texas Instruments
 Comment Type ER Comment Status D Editorial
 Sentence seems imcomplete
 SuggestedRemedy
 Remove parentheses around "see 33.2.5.5"
 Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 OBE by comment 202.

Cl 33 SC 33.2.4.4 P 211 L 41 # 219
 Schindler, Fred Seen Simply
 Comment Type ER Comment Status D Editorial
 Fix typo "Tyep".
 SuggestedRemedy
 Use "Type".
 Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 OBE by comment 96.

Cl 33 SC 33.2.4.4 P 212 L 52 # 255
 Dove, Daniel Dove Networking Solut
 Comment Type TR Comment Status X Pres: SD
 Need to add variables to address pairset operation as independent for each pairset controller.
 SuggestedRemedy
 Add: mr_ps_enable:
 A control variable that selects Pairset operation and test functions. This variable is provided by a management interface that may be mapped to the PSE Control register PS Enable A, or PS Enable B bits (11.9 and 11.8 respectively), as described below, or other equivalent functions.
 Values: True - The pairset function is defined by PSE Control register bits 1:0
 False - The pairset function is disabled
 Proposed Response Response Status W
 Wait for presentation

Cl 33 SC 33.2.4.4 P 213 L 4 # 256
 Dove, Daniel Dove Networking Solut
 Comment Type TR Comment Status X Pres: SD
 pi_powered should either be a local PS_Controller variable, or we need to have one for each pairset. For instance, one pairset may be unpowered, while the other is powered.
 SuggestedRemedy
 replace "PSE" with "pairset controller". I believe that this (replacing PSE with pairset controller) is going to be needed in multiple locations.
 Proposed Response Response Status W
 Wait for presentation

Cl 33 SC 33.2.4.4 P 214 L 52 # 139
 Yseboodt, Lennart Philips
 Comment Type TR Comment Status X Types
 Topic: Type 4 classrange
 "Type 3 and Type 4 PSEs shall issue no more class events than the class they are capable of supporting. For example, this would apply to a PSE that is oversubscribed and in power management mode or a Type 3 PSE that has a hardware limitation."
 Also applies to Type 4.
 SuggestedRemedy
 "Type 3 and Type 4 PSEs shall issue no more class events than the class they are capable of supporting. For example, this would apply to a PSE that is oversubscribed and in power management mode or a Type 3 or Type 4 PSE that has a hardware limitation."
 Proposed Response Response Status W
 Need outcome of comment 269.

Cl 33 SC 33.2.4.5 P 215 L 2 # 257
 Dove, Daniel Dove Networking Solut
 Comment Type TR Comment Status X Pres: SD
 We need to add tcc2det_timer into this subclause.
 SuggestedRemedy
 Add tcc2det_timer for state diagram to start, stop and/or identify when the timer is done.
 Defined as:
 Add tcc2det_timer for state diagram to start, stop and/or identify when the timer is done.
 Defined as:
 tcc2det_timer - A timer used to limit the duration from connection_check function being performed until detection function is started
 Proposed Response Response Status W
 Wait for Presentation.

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Cl 33 SC 33.2.4.6 P 216 L 18 # 55
Lukacs, Miklos Silicon Labs

Comment Type TR Comment Status X Definitions

This is the first place where the single and dual signature PD is mentioned, but these terms are not described.

SuggestedRemedy

Insert a chapter into section 33.1. describing the PD interface variants (single and dual signature)

Proposed Response Response Status W

We created definitions last time, they are in the definition section (1.4). Should we include a pointer here?

Cl 33 SC 33.2.4.6 P 216 L 29 # 141
Yseboodt, Lennart Philips

Comment Type TR Comment Status X Editorial

"pd_requested_power: This variable indicates the power class requested by the PD. A Type 1 PSE that measures a Class 4 signature assigns that PD to Class 0. When a PD requests a higher class than a Type 3 or Type 4 PSE can support, the PSE shall assign the PD class 3, 4, or 6, whichever is the highest that it can support."

This exact same 'shall' statement is in 33.2.6.2, page 237, line 4-5.

SuggestedRemedy

Remove "When a PD requests a higher class than a Type 3 or Type 4 PSE can support, the PSE shall assign the PD class 3, 4, or 6, whichever is the highest that it can support."

Proposed Response Response Status W

Task Force to discuss.

The Type 1 requirement was also repeated here. This text mirrors that...

Cl 33 SC 33.2.4.6 P 216 L 36 # 190
Johnson, Peter Sifos Technologies

Comment Type T Comment Status D PSE State Diagram

The value descriptions, for example Class 5, do not account for Dual Signature classifications described in Table 33-16a.

SuggestedRemedy

Either update this to reflect Dual Signature classification processing or add editor's note that do_classification function must eventually take into account Dual Signature handling.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Add editor's note: "DS PD classification must be taken into account here."

Cl 33 SC 33.2.4.6 P 217 L 10 # 258
Dove, Daniel Dove Networking Solut

Comment Type TR Comment Status X Pres: SD

The values for the do_detection function don't align with my proposed pair-set control approach. Each detection is done by the pairset controller, thus only a single pairset is under consideration. This returns the function results to their original values.

SuggestedRemedy

delete Valid_A, Valid_B and Valid_AB references.

Proposed Response Response Status W

Wait for presentation.

Cl 33 SC 33.2.4.6 P 218 L 1 # 224
Schindler, Fred Seen Simply

Comment Type ER Comment Status X Editorial

Editor's note,
"Editor's Note: "Mutual identification not complete" in above paragraph needs to be clear. Team to pay close attention to above paragraph during reviews."

I do not understand why this note exists.

SuggestedRemedy

Briefly discuss if anyone has a concern with the reference section and remove the Editor's note if no concern remains. Otherwise add some specifics to the Editor's note.

Proposed Response Response Status W

Task force to discuss

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Cl 33 SC 33.2.4.6 P 218 L 5 # 97
 Yseboodt, Lennart Philips

Comment Type ER Comment Status D Editorial

"... for which the PSE shall select to meet the requirements of its Type or a less Type such that, Type PD <= PSE Type <= Type PSE."

Can be more compact/clear + fix spelling mistake.

SuggestedRemedy

"... for which the PSE shall select to meet the requirements of any Type such that, Type_PD <= applied Type <= Type_PSE."

Request to editor: the paragraph has so many strikeouts, readability is poor. Delete paragraph and insert a fresh one.

Proposed Response Response Status W
 PROPOSED ACCEPT.

Cl 33 SC 33.2.4.6 P 218 L 5 # 114
 Yseboodt, Lennart Philips

Comment Type T Comment Status D Types

"... except for I Con-2P, I LIM-2P, T LIM-2P, and P Type (see Table 33-11), for which the PSE shall select to meet ..."

Type 3/4 PSEs are (currently, D1.2) required to support "360uF" worth of inrush unconditionally when powering over 4P. We are likely to adopt that this will become
 - "180uF" for Type 3
 - "360uF" for Type 4

It makes sense to give Type 4 PSEs (which may be restricted to lower classes) the option to support the lower inrush if they are powering (or are only capable of) lower Type PDs.

SuggestedRemedy

"... except for I Con-2P, I LIM-2P, linrush, linrush-2P, T LIM-2P, and P Type (see Table 33-11), for which the PSE shall select to meet ..."

Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.

Cl 33 SC 33.2.4.6 P 218 L 104 # 259
 Dove, Daniel Dove Networking Solut

Comment Type TR Comment Status X Pres: SD

Based on the latest proposal for the state diagram, we need to add a function called do_PD_check.

SuggestedRemedy

Insert the following; do_PD_check_
 This function initiates the PD_check in Section 33.2.5.0b. This function returns the following variable:

PD_Alt: This variable indicates which pairsets are to be considered a candidate for accepting power from the PSE.

Values:

A - The PD is a candidate for receiving power on the Alt-A pairset.

B - The PD is a candidate for receiving power on the Alt-B pairset.

Both - The PD is a candidate for receiving power on both the Alt-A and Alt-B pairsets simultaneously.

Proposed Response Response Status W
 Wait for presentation

Cl 33 SC 33.2.4.7 P 221 L 1 # 260
 Dove, Daniel Dove Networking Solut

Comment Type TR Comment Status X Pres: SD

The latest proposal for the Type 3 and Type 4 PSE State Diagram includes a higher-level hierarchical drawing, and an approach where each pairset is controlled independently for the case of a dual-signature PD, and/or a single pair-set controller (with both pairsets controlled by it).

SuggestedRemedy

Insert the attached state diagrams with appropriate color changes and removal of comments as shown in T3T4PSEStateDiagramV1.3a.pptx.

Proposed Response Response Status W
 Wait for presentaiton

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 33 SC 33.2.4.7 P 223 L 13 # 115
 Yseboodt, Lennart Philips

Comment Type T Comment Status X PSE State Diagram

Autoclass missing from state diagrams, eg: "Figure 33-9c Type 3 and Type 4 PSE delivering power state diagram" and "Figure 33-9g Type 3 and Type 4 PSE classification state diagram".

SuggestedRemedy

Insert editors note: "Autoclass to be added to state machine".

Proposed Response Response Status W

Autoclass is an optional behavior. Do these go into the SD? I didn't think so...

Cl 33 SC 33.2.4.7 P 226 L 1 # 129
 Yseboodt, Lennart Philips

Comment Type TR Comment Status X PSE State Diagram

This is part of the Type 3 and Type 4 state diagram, and as such the states CLASS_EV1 and 1-EVENT_CLASS do not apply and can be removed.

SuggestedRemedy

Remove mentioned states and incoming and outgoing arrows.
 See yseboodt_state_diagram_0915.pdf

Proposed Response Response Status W

Waiting for document.

Cl 33 SC 33.2.5 P 227 L 35 # 225
 Schindler, Fred Seen Simply

Comment Type TR Comment Status D PSE Power

The existing sentence,
 "In any operational state, the PSE shall not apply operating power to a pairset until the PSE has successfully detected a valid signature over that pairset."
 may be improved by permitting allowed specific system implementations.

SuggestedRemedy

Replace with,
 "In any operational state, the PSE shall not apply operating power to a pairset until the PSE has successfully detected a valid signature over that pairset. A PSE powering a single-signature PD with less than or equal to class 4 power levels may toggle between 2-pair and 4-pair power."

Proposed Response Response Status W

PROPOSED REJECT.

This is not the place for the 2/4-pair power transition. Additionally, that sentence exists in the appropriate section.

Cl 33 SC 33.2.5 P 227 L 37 # 35
 Darshan, Yair Microsemi

Comment Type TR Comment Status D PSE Powering

Addressing the text and the Editor Note following this text:
 In any operational state, the PSE shall not apply operating power to the PI a pairset until the PSE has successfully detected a valid signature over that pairset.

Editor's Note: The above sentence needs to be addressed as it forbids turning off and on a single pairset when connected to a SS class 0-4 PD.

 We need to allow turning on and off a single pairset when connected to single signature PD for all classes.

SuggestedRemedy

1. To add the following text after line 38:
 Type 3 and Type 4 PSE that successfully detected valid signature over each pairset of a single signature PD, may turn off one of the pairsets and turn it on gain during POWER_UP or POWER_ON states.
2. If this comment accepted, to remove editor note in lines 38-40.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Remove editor's note.

.....
 The power on part is covered in section 33.2.7.1. The power up part should be addressed in the appropriate section.

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 33 SC 33.2.5 P 227 L 38 # 92
 Yseboodt, Lennart Philips

Comment Type ER Comment Status D PSE Powering

"In any operational state, the PSE shall not apply operating power to the PI a pairset until the PSE has successfully detected a valid signature over that pairset."

"Editor's Note: The above sentence needs to be addressed as it forbids turning off and on a single pairset when connected to a SS class 0-4 PD."

This has been addressed by in 33.2.7.1:
 "A Type 3 or Type 4 PSE that is connected to a class 0-4 single-signature PD and is in the POWER_ON state may transition between 2-pair and 4-pair power at any time, including after the expiration of T pon."

SuggestedRemedy

Remove editors note.
 Possibly amend the sentence:
 "In any operational state, the PSE shall not apply operating power to the PI a pairset until the PSE has successfully detected a valid signature over that pairset. See 33.2.7.1 for transitions between 2-pair and 4-pair mode."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment 35.

Cl 33 SC 33.2.5 P 227 L 39 # 261
 Dove, Daniel Dove Networking Solut

Comment Type TR Comment Status D PSE Powering

Regarding this Editor's Note: I believe that unless its imperative to support, having a SS Type 3 or Type 4 PD precludes powering off one pairset. The relevant issue is that the PSE State Diagram does not allow a single signature process to have different power states on the different pair-sets. Adding such would substantially increase complexity. Example; What state would a Type 3 PSE with single PS Control state machine, powering a single-signature PD be in if it removed power on one pairset while keeping power on the other?

SuggestedRemedy

Remove the Editor's note and leave text as is.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment 35.

Cl 33 SC 33.2.5 P 227 L 39 # 21
 Darshan, Yair Microsemi

Comment Type T Comment Status D PSE Powering

Per the Editor Note we need to allow at POWER-UP or POWER_ON state to turn OFF and back to ON a sigle pairset.

SuggestedRemedy

1. Add the following text after line 39:
 Type 3 and Type 4 PSE that successfully detected valid signature over each pairset and powered up a Single Signature PD, may turn off one of the pairsets and turn it on gain during POWER_UP or POWER_ON states.
2. Remove Editor Note in lines 39-40.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment 35.

Cl 33 SC 33.2.5 P 227 L 40 # 93
 Yseboodt, Lennart Philips

Comment Type ER Comment Status D PSE Powering

Topic: Class 0 / Type 3 removal
 "Editor's Note: The above sentence needs to be addressed as it forbids turning off and on a single pairset when connected to a SS class 0-4 PD."

SuggestedRemedy

"Editor's Note: The above sentence needs to be addressed as it forbids turning off and on a single pairset when connected to a SS class 1-4 PD."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment 35. (note removed)

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 33 SC 33.2.5 P 227 L 42 # 214
Schindler, Fred Seen Simply

Comment Type **TR** Comment Status **X** PSE Detection

A previous comment filed indicated why changing link segment to link section changes requirements. This same concern exists for all of these changes.

SuggestedRemedy

The Task Force should discuss the implications of restoring IEEE 802.3-2012 values. When I review the specification I see link section and link segment values used interchangeably. The text in this section lines 42 and 43 are an example of this. The group should decide what is required and change all occurrences of these words to a consistent usage and technical implications.

Proposed Response Response Status **W**

Task Force to discuss.

Cl 33 SC 33.2.5 P 228 L 5 # 262
Dove, Daniel Dove Networking Solut

Comment Type **ER** Comment Status **D** Connection Check

The words "that will deliver" suggest that power WILL be delivered on both pairsets.

SuggestedRemedy

Replace "that will deliver" with "capable of delivering".

Proposed Response Response Status **W**

PROPOSED REJECT.

"that will deliver" is the intent of the sentence. If a type 3/4 PSE will only deliver power over 1 pairset, it does not need to do a connection check.

Cl 33 SC 33.2.5.01 P 228 L 36 # 218
Schindler, Fred Seen Simply

Comment Type **E** Comment Status **D**

The sentence,
"The connection check shall be rerun if power up fails to meet the timing requirements or anytime power is removed from both pairsets at the same time after reaching the POWER_UP state." may be improved.

SuggestedRemedy

Replace the text with,
"The connection check shall be rerun if power up fails to meet the timing requirements or when power is removed from both pairsets after reaching the POWER_UP state."

Proposed Response Response Status **W**

PROPOSED ACCEPT IN PRINCIPLE.

Replace with:

"The connection check shall be rerun before applying power if power up fails to meet the timing requirements or anytime power is not present on at least one pairset after reaching the POWER_UP state."

Cl 33 SC 33.2.5.2 P 229 L 50 # 98
Yseboodt, Lennart Philips

Comment Type **E** Comment Status **D** Editorial

'voltage/current' can be read as 'or', should be 'and'

SuggestedRemedy

Replace 'voltage/current' by 'voltage and current'

Proposed Response Response Status **W**

PROPOSED REJECT.

The PSE is only required to measure the voltage or current. The other one is supplied by the PSE.

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 33 SC 33.2.5 P 232 L 2 # 263
 Dove, Daniel Dove Networking Solut

Comment Type **TR** Comment Status **X** Pres: SD

4PID has been deprecated (in my proposal) by PD_Check.

SuggestedRemedy

Replace "4PID" with "PD_Check" in all instances of text using search/replace, remove the TBD, delete "the detection state" and replace with "measurements on" and delete "mutual identification". Replace PD_4pair_candidate" with "PD_Alt".

Proposed Response Response Status **W**

Wait for presentation.

Cl 33 SC 33.2.6 P 232 L 12 # 116
 Yseboodt, Lennart Philips

Comment Type **T** Comment Status **X** PSE classification

Section 3.2.6 describes classification. Classification has become significantly more complicated compared to Type 2 classification:

- single & dual signature
- Autoclass
- power demotion
- long finger vs short finger

The text alone + the state machine are sufficient to (eventually) figure out how it works, but providing a simple overview would help the reader.

SuggestedRemedy

See yseboodt_classification_overview_0915.pdf

Proposed Response Response Status **W**

Waiting for document

Cl 33 SC 33.2.6 P 232 L 31 # 130
 Yseboodt, Lennart Philips

Comment Type **TR** Comment Status **D** PSE Classification

"Based on the response of the PD, the minimum power level at the output of the PSE is P Class as shown in Equation (33-3)."

This seems like an appropriate place to explain the Pclass nuance between SS and DS PDs.

SuggestedRemedy

"Based on the response of a single-signature PD, the minimum power level at the output of the PSE is P Class as shown in Equation (33-3). For dual-signature PDs P Class applies to each pairset independently."

Proposed Response Response Status **W**

PROPOSED ACCEPT.

Cl 33 SC 33.2.6 P 233 L 10 # 191
 Johnson, Peter Sifos Technologies

Comment Type **T** Comment Status **X** Editorial

In Table 33-7, the column header "Minimum supported power levels at output of PSE (Pclass)" is not accurate. Pclass is defined in equation 33-3. Text above refers to "over-margined values..." - that is a more accurate depiction of this column. Also, for Classes 4 - 7, phrases such as "30W or Ptype as defined in Table 33-11, whichever is lower" is unusual because as presented in Table 33-11, Ptype cannot be lower than 30W.

SuggestedRemedy

Change column header "Minimum PSE output power (Pclass) See NOTE 1" and modify NOTE 1 to "This is the minimum required power at the PSE PI calculated using minimum Vport_pse and maximum Rchan. Use equation 33-3 for other values of Vport_pse and Rchan. For maximum power available to PDs, see Table 33-18."

Utilize numeric values as is done for class 0-3, namely 30 Watts, 45 Watts, 60 Watts, 75 Watts, and 90 Watts.

Proposed Response Response Status **W**

Task Force to Discuss.

We cannot just leave numbers for classes 4 and above as a lower Type PSE cannot supply that amount of power and thus Ptype is the power required.

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 33 SC 33.2.6 P 233 L 22 # 226
Schindler, Fred Seen Simply

Comment Type **TR** Comment Status **D** PSE Classification

PSEs may indicate that they are not capable of providing more than class-4 power by ending classification after 2 or 3 events. Table 33-7 indicates 2 or 3 events but Table 33-3, omit 3 events, which is confusing.

SuggestedRemedy

Indicate that 3 events may be provided by Type-3 and Type-4 PSEs in Table 33-3 on page 214.

Proposed Response Response Status **W**

PROPOSED REJECT.

Class_num_events in Table 33-3 is a maximum. Table 33-7 is not the maximum, it is the number of events required for that power.

Cl 33 SC 33.2.6 P 234 L 35 # 131
Yseboodt, Lennart Philips

Comment Type **TR** Comment Status **X** PSE Classification

Topic: Type 4 classrange
"A Type 3 PSE that will provide class 3 or lower power levels may opt to use 1-event Physical Layer classification."

SuggestedRemedy

"A Type 3 or Type 4 PSE that will provide class 3 or lower power levels may opt to use 1-event Physical Layer classification."

Proposed Response Response Status **W**

See comment 192.

Cl 33 SC 33.2.6 P 234 L 35 # 192
Johnson, Peter Sifos Technologies

Comment Type **T** Comment Status **X** PSE Classification

Footnote 1 to Table 33-8 says "A Type 3 PSE that will provide class 3 or lower power levels may opt to use 1-event Physical Layer classification". Is this really an option? Para. 33.2.6.2 mandates that a Type-3 or Type-4 PSE powering a Class 0 to 3 PD provides one-event classification with no mark events. Para. 33.3.2.4.4 (under Table 33-3) says Type-3 and Type-4 PSEs shall issue no more class events than the class they are capable of supporting..."

SuggestedRemedy

Replace "may opt to" with "is required to". (Any 'shall' here seems redundant with other paragraphs referenced above.)

Proposed Response Response Status **W**

Actually, do the long first finger requirement, I think it would be better to make TYPE 3/4 PSEs do multiple-event class (even if its only one finger) so that they then go to mark and the PD "remembers" that it saw a long finger.

Task force to discuss.

Cl 33 SC 33.2.6 P 235 L 5 # 193
Johnson, Peter Sifos Technologies

Comment Type **T** Comment Status **D** PSE Classification

Present text: "When a dual-signature PD is detected, the PSE shall supply at least the requested power over a pairset per the class code detected over that pairset". This statement, as written, demands that full requested power be provided to any dual-signature PD by any PSE detecting it. Not sure about the term "class code" - is that used anywhere else?

SuggestedRemedy

Revise this to:

A Type 3 or Type 4 PSE detecting a dual-signature PD shall not power any pairset with a classification exceeding the power available on that pairset at the PSE.

Proposed Response Response Status **W**

PROPOSED ACCEPT IN PRINCIPLE.

Possible OBE by 132

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 33 SC 33.2.6 P 235 L 5 # 132
 Yseboodt, Lennart Philips

Comment Type **TR** Comment Status **D** PSE Classification

"When a dual-signature PD is detected, the PSE shall supply at least the requested power over a pairset per the class code detected over that pairset."

Seems to force a PSE to delivered requested power, thereby breaking power demotion. Also mis-uses the word 'detection'.

SuggestedRemedy

"When connected to a dual-signature PD, the PSE shall treat the requested power over each pairset independently."

Proposed Response Response Status **W**

PROPOSED ACCEPT.

Cl 33 SC 33.2.6.2 P 236 L 27 # 194
 Johnson, Peter Sifos Technologies

Comment Type **T** Comment Status **D** PSE Classification

"PSEs that implement CLASS_EV1_LCF, when connected to single-signature PD's, shall transition directly from CLASS_EV1_LCF to MARK_EV_LAST if they implement only one class event."

First, why not say "Type 3 and Type 4 PSE's" ?

Second, the Figure 33-9g does not include this transition possibility. Figure 33-9g will need this transition if we want Type 3 and Type 4 PD's to "remember" that the PSE is Type 3 or Type 4.

Third, why is this limited to single signature PD's?

SuggestedRemedy

Figure 33-9g, the Classification State Diagram, probably needs a transition from CLASS_EV1_LCF to MARK_EV_LAST in place of transitioning to node "C".

(This could be an editor note now...)

Replace "PSEs that implement CLASS_EV1_LCF" with "Type 3 and Type 4 PSEs".

May need an editor note to review this phrase once all the details for Dual Signature classification are worked out.

Proposed Response Response Status **W**

PROPOSED ACCEPT IN PRINCIPLE.

Change text to "Type 3 and type 4 PSEs connected to single-signature PDs shall transition directly from..."

Update to Figure 33-9g to be presented.

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

CI 33 SC 33.2.6.2 P 236 L 52 # 133
 Yseboodt, Lennart Philips

Comment Type TR Comment Status D PSE Classification

"If the result of the first class event is any of Classes 0, 1, 2, or 3, a Type 3 or Type 4 PSE treats a single-signature PD as a Type 1 PD and shall omit the subsequent mark and class events and classify the PD according to the result of the first class event."

The PSE should visit MARK_EV_LAST in this case.

SuggestedRemedy

"If the result of the first class event is any of Classes 0, 1, 2, or 3, a Type 3 or Type 4 PSE treats a single-signature PD as a Type 1 PD and shall skip all subsequent class events, transition directly to MARK_EV_LAST, and classify the PD according to the result of the first class event."

Add editors note on page 226 below Figure 33-9g "TODO: add arrow from CLASS_EV1_LCF to MARK_EV_LAST".

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Change text as shown in suggested remedy.

Update to Figure 33-9g to be presented.

CI 33 SC 33.2.6.2 P 237 L 10 # 195
 Johnson, Peter Sifos Technologies

Comment Type T Comment Status D PSE Classification

"...A Type 3 or Type 4 PSE connected to a dual-signature PD shall skip all subsequent class events and transition directly to MARK_EV_LAST if the class signature during CLASS_EV3 is 0, 1, 2, or 4."

This transition option is not currently available in Figure 33-9g, the classification state diagram. Only exit from CLASS_EV3 requires PD Class =4.

Also, if a PSE uses at least 3 events to resolve Type 1 Class 3 from Type 3 Class 3, then the only option is to move onto CLASS_EV4 after measuring Class 3 on the 3rd event. Is this a problem if the PSE will not support Class 5 on that pairset? (Would CLASS_EVAL just reject the power-up?)

SuggestedRemedy

Editor note indicating this deficiency in the state diagram Fig 33-9g.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Update to Figure 33-9g to be presented.

CI 33 SC 33.2.6.2 P 238 L 41 # 240
 Picard, Jean Texas Instruments

Comment Type TR Comment Status D PSE Classification

The PSE TLCF spec needs to readjusted to align with the PD proposed changes on TACS and TLCF_PD.

SuggestedRemedy

Change the TLCF range from 85-100 ms to 88-105 ms.

Proposed Response Response Status W

PROPOSED ACCEPT.

See comments 53, 52, 54, 238, 239

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 33 SC 33.2.6.3 P 238 L 42 # 53
 Beia, Christian STMicroelectronics

Comment Type **TR** Comment Status **D** PSE Classification

Table 33-10
 The long first class Event timing for the PSE can be easily set to a tighter range with no impact on PSE complexity, since the accuracy of PSE clock already allows it. This is helpful for the PD timings which can be relaxed, since this is the more restrictive timing requirement for the PD.

SuggestedRemedy

Change Table 33-10 item 12 T_LCF to 87.5 Min
 Leave 100 as Max

Proposed Response Response Status **W**

PROPOSED ACCEPT IN PRINCIPLE.

See comment 240.

Make min 88. Max ?

Cl 33 SC 33.2.6.3 P 239 L 1 # 134
 Yseboodt, Lennart Philips

Comment Type **TR** Comment Status **D** PSE Classification

Autoclass Table 33-10a is missing values for T_auto_pse1(max) and T_auto_pse2(min).

SuggestedRemedy

Add to Table 33-10a:
 T_auto_pse1 max = 1.55
 T_auto_pse2 min = 3.1

Proposed Response Response Status **W**

PROPOSED ACCEPT IN PRINCIPLE.

These numbers are WAY TOO tight. The accuracy required to get an timer to stop between 3.1 and 3.2 seconds is +/- 1.59 %

Use:

T_auto_pse1 max = 1.65
 T_auto_pse2 min = 2.8

They both equal to 6.X% accuracies.

Cl 33 SC 33.2.6.3 P 239 L 19 # 135
 Yseboodt, Lennart Philips

Comment Type **TR** Comment Status **X** Pres: Autoclass

An improved calculation for Autoclass margin is described in yseboodt_1_0915.pdf

SuggestedRemedy

See changes in yseboodt_1_0915.pdf

Proposed Response Response Status **W**

Wait for presentation.

Cl 33 SC 33.2.7 P 239 L 25 # 227
 Schindler, Fred Seen Simply

Comment Type **TR** Comment Status **X** PSE Power

Legacy text,
 "PSE behavior conforms to the state diagrams in Figure 33-9, Figure 33-9 continued, and Figure 33-10.
 When the PSE provides power to the PI, it shall conform with Table 33-11."
 that states a requirement has been stricken from the spec.

SuggestedRemedy

Restore the text with the following TBD or replace with reference to the appropriate state diagrams.
 "PSE behavior conforms to the state diagrams in Figure 33-9, Figure 33-9 continued, Figure TBD, and Figure 33-10. When the PSE provides power to the PI, it shall conform with Table 33-11."

Proposed Response Response Status **W**

Task Force to discuss.

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 33 SC 33.2.7 P 240 L 21 # 22
 Darshan, Yair Microsemi

Comment Type T Comment Status D PSE Power

Table 33-11 item 1a, Vport_PSE_diff (PSE Vdiff).
 Background:
 We have shown that PSE Vdiff max for a single port is 0.2mV maximum calculated at worst case and the spec were set to 2mV.
 After additional research on multi-port systems we have found that the PSE Vdiff may reach to 6-8mV due to cross regulation effect of ports using shared power leads.
 Two solutions were analyzed:
 a) To specify PSE Vdiff=2mV as is today for a single port and let system designer to figure out how to make sure that in multiport operation the spec will still be met.
 This solution was rejected by few system vendors.
 b) To specify PSE Vdiff=10mV while keeping system Vdiff=60mV as it was before which move some burden on PD to use 50mV maximum when diodes are used in the PD, instead of 58mV as it is today.
 This solution looks better.
 -It will keep the same maximum pair current.
 -It will not affect PSE MPS solutions.
 -It will add tolerable burden on PD by making sure that diode Vdiff is 50mV max and not 58mV.
 - The total system E2EP2P_lunb stays the same

SuggestedRemedy

- To change Table 33-11 item 1a from 2mV to 10mV.
- To update all relevant PSE PI and PD PI numbers that will be affected by this change.

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 33 SC 33.2.7 P 240 L 39 # 13
 Darshan, Yair Microsemi

Comment Type T Comment Status D PSE Power

1.To update TBDs for Icon-2P_unb min in Table 33-11 item 4a for classes 5 and 7.
 2. To update class 8 value from 0.931A to 0.926A due to the change of Pclass PD from 71.3W to 71W.
 See details on page 2 of darshan_04_0915.pdf.

SuggestedRemedy

Replace TBDs in Table 33-11 item 4a, Icon-2P_unb minimum value column:
 Class 5: Replace TBD with 0.536A
 Class 7: Replace TBD with 0.778A
 Class 8: Change from 0.931A to 0.926A

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 33 SC 33.2.7 P 240 L 42 # 3
 Darshan, Yair Microsemi

Comment Type E Comment Status D PSE Power

Table 33-11 item 4a, additional information.
 1. It is 33.2.7.4.1 and not 33.2.7.4a
 2. The additional information do not cover all the information needed for item 4a. It is 33.2.7.4 and 33.2.7.4.1

SuggestedRemedy

Table 33-11 item 4a, additional information.
 Replace See 33.2.7.4a with: See 33.2.7.4 and 33.2.7.4.1

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 33 SC 33.2.7 P 240 L 44 # 206
 Dwelley, David Linear Technology

Comment Type ER Comment Status X Editorial

Table 33-11, item 4a: The Icon-2p-unb label makes less sense than before because of the change made in the D1.1 comment cycle that changed Icon-2p to Icon. The -unb suffix made sense when there was a standalone Icon-2p parameter but not now.

SuggestedRemedy

Change Icon-2p-unb to Icon-2p throughout: I count 6 locations on pages 240, 245, 246, and 276, and two more with _unb on pages 198 and 245.

Also change the existing Icon-2p to Icon on p245 line 23 to be consistent.

Proposed Response Response Status W

Task Force to Discuss (Yair...)

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 33 SC 33.2.7 P 241 L 17 # 152
 Yseboodt, Lennart Philips

Comment Type TR Comment Status D PSE Power

Table 33-11, Item 7, Icut-2P.

Icut-2p is the range in which the PSE may optionally cut power. The lowerbound was defined by Icon in 802.3-2012. The correct lowerbound now would be Icon-2P-unb. The calculation in D1.2 also results in Icon-2P-unb values.

Issues:

- Rather than a calculation, we can refer to Icon-2P-unb
- In its current form it is defined per Type, which results in Icut-2P being smaller than Icon-2P-unb for Class 5 and 7
- It is too high in 2P mode

SuggestedRemedy

Replace the 'min' value of Icut-2p for Type 3 and Type 4 by 'Icon-2P-unb'. Add editors note below Table 33-11 "Icut-2P min should be equal to the relevant section of the lowerbound template which is currently TBD. "

Note: somewhat less broken, needs further work (does not work for dual-signature, have not fixed 2P mode)

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

This parameter should be fixed, but the min values you suggest are not correct. For example, if the PSE uses active current balancing, it could use the values listed currently.

Task Force to Discuss

Cl 33 SC 33.2.7 P 241 L 20 # 18
 Darshan, Yair Microsemi

Comment Type T Comment Status X Pres: Unbalance

Table 33-11 item 7.

We need to update Kicut3 and Kicut4 to include the constants for class 5 and 7 otherwise they will create errors resulted with Icont-2P_unb doesnt equal to Icut_min. See details in Darshan_07_0915.pdf.

SuggestedRemedy

See details in Darshan_07_0915.pdf for updating Table 33-11 item 7.

Proposed Response Response Status W

Wait for presentation

Cl 33 SC 33.2.7 P 241 L 34 # 14
 Darshan, Yair Microsemi

Comment Type T Comment Status X Pres: Yair6

- To update TBDs for ILIM-2P min in Table 33-11 item 9 classes 5 and 7. See derivation in darshan_06_0915.pdf.

SuggestedRemedy

Table 33-11 item 9, ILIM-2P minimum value column:
 Class 5: Replace TBD in ILIM-2P min with 0.551A
 Class 7: Replace TBD in ILIM-2P min with 0.829A

Proposed Response Response Status W

Wait for presentation.

Cl 33 SC 33.2.7 P 241 L 38 # 242
 Picard, Jean Texas Instruments

Comment Type TR Comment Status X PSE Power

there is too much margin for ILIM-2P

Table 33-11

SuggestedRemedy

Reduce ILIM-2P class 6 to a value slightly below 0.7A

Proposed Response Response Status W

What is the reason behind this? Yair do you agree?

Cl 33 SC 33.2.7 P 241 L 38 # 17
 Darshan, Yair Microsemi

Comment Type T Comment Status X Pres: Yair6

To update ILIM-2P min in Table 33-11 item 9 classes 6 and 8. It reduces currents by about 15% due margins reduction that can be left to designer decision.

Reason for update:

In order to reduce currents, we utilized the fact that Ppeak_PD is lower now and we dont force Icut_max/Icon-2P_unb= about 1.15 as in 802.3at. See derivation in darshan_06_0915.pdf.

SuggestedRemedy

Table 33-11 item 9, ILIM-2P minimum value column:
 Class 6: Change from 0.817A to 0.691A.
 Class 8: Change from 1.162A to 0.990A.

Proposed Response Response Status W

Wait for presentation

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 33 SC 33.2.7 P 241 L 43 # 241
 Picard, Jean Texas Instruments
 Comment Type **TR** Comment Status **X** PSE Power
 there is too much margin for ILIM-2P
 SuggestedRemedy
 Reduce ILIM-2P class 8 to a value slightly below 1A
 Proposed Response Response Status **W**
 What is the reason behind this? Yair do you agree?

Cl 33 SC 33.2.7 P 243 L 45 # 42
 Darshan, Yair Microsemi
 Comment Type **ER** Comment Status **X** Pres: Yair4
 There are list of editor notes on page 243-244 that need to be updated per the progress made in D1.1 and the possible acceptance of comments in D1.2.
 See the proposed updates for Editor Notes in page 243-244 in darshan_04_0915.pdf page 5.
 SuggestedRemedy
 In case updates proposed by darshan_04_0915.pdf pages 1-4 will be accepted, to update Editor's Notes in page 243-244 per darshan_04_0915.pdf page 5.
 Proposed Response Response Status **W**
 Wait for presentation

Cl 33 SC 33.2.7 P 243 L 45 # 5
 Darshan, Yair Microsemi
 Comment Type **E** Comment Status **X** Pres: Yair4
 Editor Notes on Page 243 lines 44-47 and page 244 lines 1-21 to change per page 5 of darshan_04_0915.pdf due to addressing the issues in D1.1 and D1.2.
 SuggestedRemedy
 Editor Notes on Page 243 lines 44-47 and page 244 lines 1-21 to change per page 5 per darshan_04_0915.pdf.
 Proposed Response Response Status **W**
 Wait for presentation

Cl 33 SC 33.2.7.1 P 244 L 43 # 264
 Dove, Daniel Dove Networking Solut
 Comment Type **TR** Comment Status **D** PSE Power
 If we are going to allow this, we need to address the stability issues and potential interoperability problems that may occur if a PSE suddenly removes power from one pair-set, and also how to deal with applying power to that pairset without creating stability problems.
 SuggestedRemedy
 Remove the added text on lines 43 and 44.
 Proposed Response Response Status **W**
 PROPOSED REJECT.
 Do you know of any stability or interoperability problems that may occur.
 There are many systems that already do this...

Cl 33 SC 33.2.7.4 P 245 L 18 # 153
 Yseboodt, Lennart Philips
 Comment Type **TR** Comment Status **X** Icon
 "PSEs shall meet I Con as specified in Table 33-11. Type 3 and Type 4 PSEs when connected to a single-signature PD shall meet I Con-2P as specified in Table 33-11 item 4a."
 Problems:
 - Does not address dual signature
 - I Con-2P no longer exists
 SuggestedRemedy
 "PSEs connected to a single-signature PD shall meet Icon and Icon-2P_unb as specified in Table 33-11.
 PSEs connected to a dual-signature PD shall meet Icon on each pairset as specified in Table 33-11."
 (Note: this works, because Pclass is defined to be independent for dual-signature PDs.)
 (Note: we need to specify that Icon, in the context of dual-signature, refers to the pairset current (what used to be Icon-2P), see other comment).
 Proposed Response Response Status **W**
 Task force to discuss.
 Do PSEs really need to meet Icon-2P_unb? Or do they only need to meet that if they don't control unbalance somehow?

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 33 SC 33.2.7.4 P 245 L 19 # 200
 Dwelley, David Linear Technology

Comment Type E Comment Status D Icon

Hierarchy of "shalls" is not as clear as it could be:
 "PSEs shall meet ICon as specified in Table 33-11. Type 3 and Type 4 PSEs when connected to a single signature PD shall meet ICon-2P as specified in Table 33-11 item 4a."

SuggestedRemedy

Add an "also":
 "PSEs shall meet ICon as specified in Table 33-11. Type 3 and Type 4 PSEs when connected to a single signature PD shall also meet ICon-2P as specified in Table 33-11 item 4a."

Proposed Response Response Status W

PROPOSED ACCEPT.

See comment 153

Cl 33 SC 33.2.7.4 P 245 L 19 # 2
 Darshan, Yair Microsemi

Comment Type E Comment Status D Icon

"single-signature PD shall meet ICon-2P as specified in Table 33-11 item 4a."

Typo: It is Icont-2P_unb and not Icont-2P

SuggestedRemedy

Change to:
 single-signature PD shall meet ICon-2P-UNB as specified in Table 33-11 item 4a.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Change to:
 single-signature PD shall meet ICon-2P-unb as specified in Table 33-11 item 4a.

Cl 33 SC 33.2.7.4 P 245 L 21 # 154
 Yseboodt, Lennart Philips

Comment Type TR Comment Status D Icon

"I Con is the total current of both pairs with the same polarity that a PSE has to support. I Con-2P_unb is the maximum current the PSE is required to support over one of the pairs of same polarity under E2EP2PRunb condition in the POWER_ON state."

Only applies to single-signature.
 Replace E2EP2PRunb by defined terminology.

SuggestedRemedy

"When connected to single-signature PDs, I Con is the total current of both pairs with the same polarity that a PSE has to support. I Con-2P_unb is the maximum current the PSE is required to support over one of the pairs of same polarity at maximum current unbalance condition in the POWER_ON state."

When connected to a dual-signature PD, I Con is the current of a pairset that a PSE has to support."

Note: by removing -2P, things fit better for single-signature, but now we have to shoehorn things for dual-signature.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Cl 33 SC 33.2.7.4 P 245 L 22 # 49
 Bennett, Ken Sifos Technologies, In

Comment Type T Comment Status D Icon

The statement:
 "ICon-2P_unb is the maximum current the PSE is required to support..."
 should say:
 "ICon-2P_unb is the minimum current the PSE is required to support..."

SuggestedRemedy

Change the word "maximum" to "minimum".

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

CI 33 SC 33.2.7.4 P 245 L 22 # 198
 Dwelley, David Linear Technology

Comment Type E Comment Status D Icon

The E2EP2PRunb section of this sentence is awkward, and E2EP2PRunb is used before it is defined:

"ICon-2P_unb is the maximum current the PSE is required to support over one of the pairs of same polarity under E2EP2PRunb condition in the POWER_ON state."

SuggestedRemedy

Replace with:

"ICon-2P_unb is the maximum current the PSE is required to support over any pair in the POWER_ON state when unbalance effects are included."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

CI 33 SC 33.2.7.4 P 245 L 23 # 4
 Darshan, Yair Microsemi

Comment Type E Comment Status D Icon

"In addition to ICon-2P and ICon-2P-UNB as specified in Table 33-11, the..."

Typo: It is Icont and not Icont-2P

SuggestedRemedy

Change from:

"In addition to ICon-2P and ICon-2P-UNB as specified in Table 33-11, the..."

To:

"In addition to ICon and ICon-2P-UNB as specified in Table 33-11, the..."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

CI 33 SC 33.2.7.4 P 245 L 40 # 155
 Yseboodt, Lennart Philips

Comment Type TR Comment Status D Editorial

"K is the ratio between I Peak-2P due to system end to end pair-to-pair current unbalance effect..."

"K=0 for two pair systems (Type 1 and Type 2 systems). The value of K which is based on curve fit and is dimensionless, for a Type 3 and Type 4 system that operates as 4-pair system is given by Equation (33-4a)."

Main issue: K=0 also for dual-signature PDs.

SuggestedRemedy

Reword & fix:

Replace

"K=0 for two pair systems (Type 1 and Type 2 systems). The value of K which is based on curve fit and is dimensionless, for a Type 3 and Type 4 system that operates as 4-pair system is given by Equation (33-4a)."

By

"The value of K is based on a curve fit and is dimensionless. For Type 3 and Type 4 PSEs, operating in 4-pair mode and connected to single-signature PDs, the value of K is given by Equation 33-4a. In all other cases the value of K is 0."

Proposed Response Response Status W

PROPOSED ACCEPT.

CI 33 SC 33.2.7.4 P 245 L 49 # 33
 Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Yair 4

Equation 33-4a (the equation that describes K) need to be updated per class 5 and 7 and not just class 6 and 8 as it is now.

It is in line with all updates made for PSE/PD P2P_Runb for better accuracy due to the fact that unbalance parameters are changed as function of current.

SuggestedRemedy

Implement the changes proposed in page 4 of darshan_04_09.pdf

Proposed Response Response Status W

Wait for presentation

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 33 SC 33.2.7.4.1 P 246 L 6 # 199
 Dwelley, David Linear Technology

Comment Type E Comment Status D Icon

The PSE_P2PRunb and E2EP2PRunb acronyms are unnecessarily complicated. The descriptions and analysis in 33.2.7.4.1 make the nature of the unbalance clear - the acronym doesn't need to carry all the details.

SuggestedRemedy

Replace with PSEunb and E2Eunb throughout this section and in section 33A.6.

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 33 SC 33.2.7.4.1 P 246 L 10 # 209
 Dwelley, David Linear Technology

Comment Type T Comment Status D Icon

Leftover Icon-2p reference and some awkward language:
 "The PSE_P2PRunb determined by RPair_max and RPair_min ensures that along with any other parts of the system - i.e. channel (cables and connectors) and the PD, the maximum pair current due to E2EP2PRunb, is not exceeding Icon-2P-unb as defined in Table 33-11 during normal operating conditions. Icon-2P-unb maximum is the average pair current due to E2EP2PRunb that is higher than Icon-2P specified in Table 33-11."

SuggestedRemedy

Fix first sentence:
 "The PSE_P2PRunb parameter is chosen to ensure that unbalance in other parts of the system (cables, connectors and PD) will not cause the maximum pair current to exceed Icon-2P-unb (as defined in Table 33-11) during normal operating conditions."

Strike the second sentence.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Suggested remedy for first sentence is good.

Still need definition of Icon-2p-unb (or whatever we choose to call it now).

Cl 33 SC 33.2.7.4.1 P 246 L 11 # 156
 Yseboodt, Lennart Philips

Comment Type TR Comment Status D Icon

"I con-2P-unb maximum is the average pair current due to E2EP2PRunb that is higher than I con-2P specified in Table 33-11."

There is no I con-2P-unb maximum. Icon-2P no longer exists.

SuggestedRemedy

"I con-2P-unb is the pairset current in case of maximum unbalance and will be higher than half of Icon."

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 33 SC 33.2.7.4.1 P 246 L 11 # 112
 Yseboodt, Lennart Philips

Comment Type ER Comment Status D Icon

"... the maximum pair current due to E2EP2PRunb, is not exceeding I con-2P-unb as defined in Table 33-11 during normal operating conditions."

SuggestedRemedy

"... the maximum pair current due to E2EP2PRunb, does not exceed I con-2P-unb as defined in Table 33-11 during normal operating conditions."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by 209.

Cl 33 SC 33.2.7.4.1 P 246 L 14 # 113
 Yseboodt, Lennart Philips

Comment Type ER Comment Status D Icon

"I con-2P-unb maximum is specified for total channel common mode pair resistance from 0.1 to 12.5."

There is no I con-2P-unb maximum. Possible to use Rch rather than constant.

SuggestedRemedy

"I con-2P-unb is specified for total channel common mode pair resistance from 0.1 to Rch."

Proposed Response Response Status W

PROPOSED ACCEPT.

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 33 SC 33.2.7.4.1 P 246 L 15 # 32
 Darshan, Yair Microsemi

Comment Type TR Comment Status D Editorial

See related comment YD_002_PSEP2P.
 "For channels with common mode pair resistance lower than 0.1 ..., see guidelines in Annex 33A."

The relevant material in Annex 33A (from 33A.6 to 33A.10) is NORMATIVE and it was originally named Annex 33B. see separate comment on Annex 33B ((MARKED FOR REFERENCE AS YD_002_PSEP2P) that was not implement correctly per the approved documents from July 2015)

Therefore:

1. the word guidelines not to be used.
2. Replace reference from Annex 33A to Annex 33B.

SuggestedRemedy

replace:

For channels with common mode pair resistance lower than 0.1 ..., see guidelines in Annex 33A."

With:

For channels with common mode pair resistance lower than 0.1 ..., see Annex 33B."

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 33 SC 33.2.7.4.1 P 246 L 21 # 16
 Darshan, Yair Microsemi

Comment Type T Comment Status X Pres: Yair4

To update equation 33-4b to include classes 5 and 7.
 See details in page 1 of darshan_04_0915.pdf.

SuggestedRemedy

1. Implement updates per page 1 of darshan_04_0915.pdf.
2. Remove Editor Note in page 246 line 37

Proposed Response Response Status W

Wait for presentation

Cl 33 SC 33.2.7.5 P 246 L 49 # 157
 Yseboodt, Lennart Philips

Comment Type TR Comment Status D PSE Inrush

"POWER_UP mode occurs on each pairset between the PSE's transition to the POWER_UP state on that pairset and either the expiration of T Inrush-2P or the conclusion of PD inrush currents on that pairset (see 33.3.7.3)."

For Type 3 and Type 4 PSEs, the conclusion of the PD inrush current is not cause to transition to POWER_ON.

SuggestedRemedy

"POWER_UP mode occurs on each pairset between the PSE's transition to the POWER_UP state on that pairset and either the expiration of T Inrush-2P or, for Type 1 and Type 2 PSEs that make use of legacy inrush, the conclusion of PD inrush currents on that pairset (see 33.3.7.3)."

Proposed Response Response Status W

PROPOSED ACCEPT.

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 33 SC 33.2.7.5 P 247 L 14 # 26
 Darshan, Yair Microsemi

Comment Type T Comment Status D PSE Inrush

Addressing the text:
 For Type 1 PSE, measurement of minimum Inrush-2P requirement to be taken after 1 ms to allow startup transients. A Type 2 PSE that uses 1-Event Physical Layer classification, and requires the 1ms settling time, shall power up a class 4 PD as if it used 2Multiple-Event Physical Layer classification.

- 1. Measuring after 1msec to account for transients is true for:
 a) all PSE Types and not just Type 1.
 b) Not clear how the rest of the text addressing classification is related to the inrush requirements.

SuggestedRemedy

1. Change the first sentence from:
 For Type 1 PSE, measurement of minimum Inrush-2P requirement to be taken after 1 ms to allow startup transients.

To:
 Measurement of minimum Inrush-2P requirement to be taken after 1 ms to allow startup transients.

2. Delete:
 A Type 2 PSE that uses 1-Event Physical Layer classification, and requires the 1ms settling time, shall power up a class 4 PD as if it used 2Multiple-Event Physical Layer classification. OR explain why we need it. As it is worded and combined with the first sentence, it is not clear the intent and the need.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

We need to extend this to all PSEs that use single event.

Task Force to discuss.

Cl 33 SC 33.2.7.6 P 248 L 18 # 23
 Darshan, Yair Microsemi

Comment Type T Comment Status D PSE Power

Referring to the text:
 The ICUT-2P threshold may equal the IPeak-2P value determined by Equation (33-4).

 When we changed Ppeak_PD/Pclass_PD ratio from 1.11 to 1.05 to reduce maximum ipeak current, it caused lpeak-2P to be close to lcont-2P_unb which required tighter accuracy for setting lcut-2P threshold.

As a result, for allowing design flexibility and cost effective solutions we can allow lcut-2P threshold to be equal or higher that lpeak-2P due to the fact that removing power due to crossing lcut-2P is not mandatory.

As a result we need to explicitly clarify and allow the following:

- a) The ICUT-2P threshold may equal or greater (not just equal) the IPeak-2P value determined by Equation (33-4).
- b) ICUT-2P threshold must be below ILIM_MIN (as usual).
- c) The value of lcut_2P_max shall not exceed 1.15*Icon-2P_unb
- d) Any combinations of the above will not cause violating PSE maximum power allowed.

SuggestedRemedy

To change:
 The ICUT-2P threshold may equal the IPeak-2P value determined by Equation (33-4).

To:
 The ICUT-2P threshold may equal or greater than the IPeak-2P value determined by Equation (33-4). The lcut-2P threshold needs to be below ILIM_MIN as described by Figure 33-14.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

To change:
 The ICUT-2P threshold may equal the IPeak-2P value determined by Equation (33-4).
 To:
 The ICUT-2P threshold shall be equal to or greater than the lpeak-2P value determined by Equation (33-4). The lcut-2P threshold shall be below ILIM_MIN as described by Figure 33-14.

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 33 SC 33.2.7.6 P 248 L 26 # 221
 Schindler, Fred Seen Simply

Comment Type ER Comment Status X PSE Power

The existing text,
 " When connected to a single signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset."
 provides unnecessary guidance. The prior sentence,
 "Power shall be removed from a pairset of a PSE before the pairset current exceeds the "PSE upperbound template" in Figure 33-14."
 provides requirement. On pages 239 to 240,
 "Power may be removed from both pairsets any time power is removed from one pairset.
 Editor's Note: All other instances of the above statement to be removed from draft. If commentators find any please comment against them." The first sentence called out in this comment is fits the concern expressed in the Editor's note.

The requirement in this section prevents one or both of the pairsets from crossing the PSE upperbound template. Concerns about delays in turning off one pairset then a second pairset may not warranted because the device connected to the PSE is no longer considered a PD. Having the ability to control pairsets individually permits system providers to build systems capable of removing power from a fault while still providing power on a nonfaulting pairset.

SuggestedRemedy

Strike the sentence,
 " When connected to a single signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset."

Proposed Response Response Status W

Task Force to discuss.

Cl 33 SC 33.2.7.7 P 248 L 26 # 36
 Darshan, Yair Microsemi

Comment Type TR Comment Status X PSE Power

Referring to the text:
 When connected to a single signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset.

The above text meant to protect single signature classes 6 and up PDs from having all the current flowing over one pairset when the other pairset is about to cross the upperbound template of figure 33-14.
 The TBD need to be replaced with text that reflects it.

SuggestedRemedy

Alternative 1:
 Change from:
 When connected to a single signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset.

To:
 When connected to above class 5 single signature PD, a Type 3 or Type 4 PSE should should remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset.

Alternative 2:
 Remove the above text ("When connected to a single signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset.")

Due to the fact that the text in lines 24-26 covers already what we want and shown here below for reference :

"A PSE may remove power from the PI if the PI current meets or exceeds the "PSE lowerbound template" in Figure 33-14. Power shall be removed from the a pairset PI of a PSE before the pairset PI current exceeds the "PSE upperbound template" in Figure 33-14."

So if the current over a pairset is about to cross the upperbound and as a result power was disconnected from that pair, the other pair will be overloaded and disconnected as well due its own protections.

Proposed Response Response Status W

Task Force to discuss.

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 33 SC 33.2.7.7 P 248 L 27 # 127
 Yseboodt, Lennart Philips

Comment Type T Comment Status X PSE Power

"When connected to a single signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset."

TF to discuss if we can lose the TBD.

SuggestedRemedy

Remove TBD.

Proposed Response Response Status W

Task Force to discuss.

Cl 33 SC 33.2.7.7 P 248 L 33 # 25
 Darshan, Yair Microsemi

Comment Type T Comment Status D PSE Power

After line 33 which is the end of:
 "The maximum value of ILIM-2P is the PSE upperbound template described by Equation (33-6) and Figure 33-14."

We need to mention that ILIM-2P minimum in Table 33-11 item 9 include the effects of end to end pair to pair current/resistance unbalance.

SuggestedRemedy

1. Add after the above text:
 ILIM-2P minimum value in Table 33-11 item 9 for class 5 and above includes E2EP2PRunb effect.
2. Remove note #5 at the Editor Note section in page 244 line 13.

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 33 SC 33.2.7.7 P 249 L 1 # 160
 Yseboodt, Lennart Philips

Comment Type TR Comment Status X Pres: Lennart2

Figure 33-14.
 In contrast to 802.3-2012, the parameter Ilim(min) went from being Type dependent to being Class dependent.
 The reason is that we do not want Type 3/4 PSEs that are restricted to low power, to have to support comparatively enormous currents up to Tlim(min) in the lowerbound template.

Fig 33-14 also uses Ilim(min) in the upperbound template, for $t > T_{cut}(max)$.
 The side effect is that that upperbound limit is no longer Type-constant, but moves with Class.

See comment #94 against D1.1:
 "Comment is rejected because this is not necessary behavior and is a feature rather than a requirement. This allows PSEs to use a single current limit and not dynamically change it."

SuggestedRemedy

Solution is to have this section of the upperbound template defined by another parameter. This could be any of: something new, Ilim(max), Icut(max), ...

I am suggesting Icut(max) in the presentation.

See presentation yseboodt_2_0915.pdf on Figure 33-14 for replacement figures.

Proposed Response Response Status W

Wait for presentation.

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 33 SC 33.2.7.7 P 249 L 1 # 159
 Yseboodt, Lennart Philips

Comment Type TR Comment Status X Pres: Lennart2

This Figure 33-14 now works on a per pairset basis, rather than a PI basis.
 This has the effect to double all the constants in the Figure when the PSE operates in 4P mode.
 The issue is with the 1.75A constant in the upperbound template.

In 802.3-2012 this was chosen as $100W / 57V = 1.75A$.
 IEC 60950 lists a maximum Isc for Class 2 power sources as $150W / Vmax = 150W / 57V = 2.63A$ or 1.3A per pairset.

TF to discuss if we need to change 1.75A to 1.3A.

Note:
 - Adopting 1.3A limit introduces a margin challenge for Class 7-8 PSEs
 - Discussion with IEC experts still ongoing to see how to interpret this specification

SuggestedRemedy
 See presentation yseboodt_2_0915.pdf on Figure 33-14 for replacement figures.

Proposed Response Response Status W
 Wait for presentation.

Cl 33 SC 33.2.7.7 P 249 L 1 # 161
 Yseboodt, Lennart Philips

Comment Type TR Comment Status X Pres: Lennart2

Figure 33-14 still has a TBD. It is there because this is a very tricky to define value with our current set of parameters.

SuggestedRemedy
 The lowerbound TBD is Icon - 'the current in the other pairset'.
 It is probably helpful for the reader to also show the effect of unbalance in this Figure.

See presentation yseboodt_2_0915.pdf on Figure 33-14 for replacement figures.

Proposed Response Response Status W
 Wait for presentation

Cl 33 SC 33.2.7.7. P 249 L 15 # 24
 Darshan, Yair Microsemi

Comment Type T Comment Status X Pres: Yair2

Figure 33-14.
 We need to capture Type 1cand Type 2 requirements and Type 3 and Type 4 requirements.
 See proposed solution in darshan_02_0915.pdf

SuggestedRemedy
 To implement darshan_02_0915.pdf.

Proposed Response Response Status W
 Wait for presentation

Cl 33 SC 33.2.7.7 P 249 L 28 # 158
 Yseboodt, Lennart Philips

Comment Type TR Comment Status X Pres: Lennart2

In Figure 33-14, x axis, there is a marked time with value of 8.2ms.
 Followed by a marked time with value T_LIM-2P(min).
 For Type 4, T_LIM-2P(min)=6ms, which is less than 8.2ms.

SuggestedRemedy
 See presentation yseboodt_2_0915.pdf on Figure 33-14 for replacement figures.

Proposed Response Response Status W
 Wait for presentation.

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 33 SC 33.2.7.7 P 249 L 43 # 37
 Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Lennart2

In Equation 33-7 there is a TBD that can be replaced with parametric values.
 This part addresses the lowerbound template for the time point $t \geq T_{cut-2P}$ min.
 The value of this it has to be the value of 2P current without the effect of unbalance and up to $I_{cont-2P_unb}$ which is the maximum possible DC current over the pair including E2EP2P_{Runb} effect.
 In other words:
 For Type 3 and 4 classes 5-8: The value is $0.5 * P_{class} / V_{port_PSE}$ to I_{con-2P_unb} .

SuggestedRemedy

1. Replace the entire row of the TBD in equation 33-7 to two separate rows:
 Row #3: $0.5 * P_{class} / V_{port_PSE} - 2P$ to I_{con-2P_unb} for $t \geq T_{cut-2Pmin}$ and for classes 5-8 operating over four pairs.
 Row #4: $0.5 * P_{class} / V_{port_PSE} - 2P$ for $t \geq T_{cut-2Pmin}$ and for classes 0-4 operating over two pairs.
2. Add after line 3 page 50:
 I_{con-2P_unb} is specified in Table 33-11.

Proposed Response Response Status W

Wait for Lennart's presentations

Cl 33 SC 33.2.7.11a P 251 L 3 # 230
 Schindler, Fred Seen Simply

Comment Type TR Comment Status X Types

The added section and choices made related to Type power may confuse the market place. Previously we had Types that indicated abilities, one of which was maximum expected power. Type 3 and 4 introduce devices that no longer guaranty a specific power level. These choices require new terms to be used and explained.

Before we had a Type-X system that indicated cabling, connectors, power source, and power acceptance ability.

Now we have Type-X PSE that cannot provide full power to a Type-X PD and the system cabling infrastructure needs to meet the Type-X PSE needs. If I change the Type-X PSE to a PSE that supports the maximum class possible for Type-X the cabling infrastructure needs to be changed.

Using the suggested solution removes many corner-cases and footnotes, which makes the specification easier to understand.

SuggestedRemedy

The Task Force should discuss these implications and the need for so many variants of the same Type to determine how to proceed.

The preferred solution is to require a PSE of Type-X to provide $P_{type(min)}$ for that type.

Proposed Response Response Status W

Task Force to discuss.

Cl 33 SC 33.2.7.11a P 251 L 13 # 27
 Darshan, Yair Microsemi

Comment Type T Comment Status D PSE Power

The text:
 Type 4 PSEs shall not source more power than $P_{Type\ max}$ as specified in Table 33-11 calculated with any sliding window with a width of 1 (TBD) second.

 For design flexibility we can allow 1sec window to 5sec which is much less than 60sec and get rid of the TBD

SuggestedRemedy

Replace TBD with 1 to 5 seconds.

Proposed Response Response Status W

PROPOSED ACCEPT.

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 33 SC 33.2.8 P 251 L 36 # 128
 Yseboodt, Lennart Philips

Comment Type T Comment Status X PSE Power

"A PSE does not initiate power provision to a link if the PSE is unable to provide the maximum power level requested by the PD based on the PD's class." (As in 802.3at)

"A PSE shall not initiate power provision to a link if the PSE is unable to provide the maximum power level requested by the PD based on the PD's class." (As in 802.3af)

In .at the shall was changed to 'does not', which is no longer normative, but also not correct.

SuggestedRemedy

"A PSE shall not initiate power provision to a link if, based on the number of classification events produced by the PSE, the PD is unable to ascertain the available amount of power based on the PDs advertised class."

Proposed Response Response Status W

I don't understand the suggested remedy. How can the PSE know what the PD is able to ascertain or not?

This is handled in .3at by a Type 1 PSE classifying a class 4 PD as class 0 (or 3). We could handle it in a similar way or we can change this sentence to reflect power demotion.

Cl 33 SC 33.3.1 P 255 L 51 # 271
 Jones, Chad Cisco

Comment Type T Comment Status X 57V

Still looking for the proper wording for the understood implied specification: "The PD shall withstand any voltage from 0 V to 57 V at the PI indefinitely without permanent damage."

SuggestedRemedy

Type 1 and Type 2 PDs shall withstand any voltage from 0V to 57V at the PI indefinitely without permanent damage.

Type 3 and Type 4 PDs shall withstand any voltage or combination of voltages from 0V to 57V across any polarity combination of the Mode A pairset, the Mode B pairset, and both Mode A and Mode B pairsets (defined in Table 33-13) indefinitely without permanent damage.

These tests shall be run with the two conductors of each tested pair at the same voltage potential.

Proposed Response Response Status W

Task Force to discuss.

This language would cause problems for the "half active bridge" implementation that is commonly used.

Cl 33 SC 33.3.1 P 255 L 51 # 229
 Schindler, Fred Seen Simply

Comment Type TR Comment Status X 57V

New PD Types will need to accept up to 57V on each pair set. Fix text, "The PD shall withstand any voltage from 0 V to 57 V at the PI indefinitely without permanent damage."

SuggestedRemedy

Replace the Draft text with,

Solution-1:

Type 1 and Type 2 PDs shall withstand any voltage from 0 V to 57 V at the powered pairset indefinitely without permanent damage. Type 3 and Type 4 PDs shall withstand any voltage from 0 V to 57 V on both pair sets indefinitely without permanent damage.

Solution-2:

Type 1 and Type 2 PDs shall withstand any voltage from 0 V to 57 V at the powered pairset indefinitely without permanent damage. Type 3 and Type 4 PDs shall withstand any voltage from 0 V to 57 V on both pair sets or between pairsets indefinitely without permanent damage.

Proposed Response Response Status W

Task Force to discuss.

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 33 SC 33.3.2 P 256 L 17 # 176
 Zimmerman, George CME Consulting

Comment Type **TR** Comment Status **D** Types

Table 33-13a is entitled "Permissible PD Types" as such, it should list the types, 1 row per type. There are two entries for "Type 3/SS", differentiated by their class, not their type. They differ in the physical layer class events and whether data link layer classification is required. These differences should just be noted in a single row since the PDs are of the same type, or, are they really a different type? (the first is preferable, since a PD really shouldn't change it's type, but might under some circumstances operate say as class 3, and others as class 4)

SuggestedRemedy

Either: a) Define Type 3/SS Class 1-3 and Type 3/SS Class 4-6 as separate types (i.e., rename them e.g., Type 3a/SS and Type 3b/SS) or, preferably
 b) merge the two rows showing the 2 class ranges under physical layer class and data link layer class.

Proposed Response Response Status **W**

PROPOSED ACCEPT IN PRINCIPLE.

These rows could be combined if the class 1-3 row still uses multiple-event (I think it should). Then only a note would be needed for DLL support.

Cl 33 SC 33.3.2 P 256 L 36 # 178
 Zimmerman, George CME Consulting

Comment Type **TR** Comment Status **D** Types

There are two major informative distinctions in the table, which are puzzling, but left out of the discussion. Without pointing these out, the reader is likely to think it a typographical error.

- 1) Class 6 is not permitted for any Type 4 PDs
- 2) Class 0 is not permitted for any PDs other than Type 1.

SuggestedRemedy

Insert: "Class 0 is not permitted for any PDs other than Type 1." on line 36, after the end of the sentence (same paragraph as Type 1 PDs).
 Insert: "Class 6 is not permitted for Type 4 PDs." as a new paragraph after line 52.

Proposed Response Response Status **W**

PROPOSED ACCEPT.

Cl 33 SC 33.3.2 P 257 L 1 # 170
 Zimmerman, George CME Consulting

Comment Type **ER** Comment Status **X** Editorial

Most all of Section 33.3.2 appears to be informative - summarizing requirements and allowed type/classification/LLDP requirements where the normative requirements are elsewhere (if they aren't then the section is missing the 'shall' statements and any PICs). However, at the end of the section there are two requirements (PD5 (underpowered PDs) and PD6 (25.4.5 compliance) which seem misplaced. These make the informative nature of the new text unclear (hence why this isn't a maintenance request), and the informative text needs to be separated from the normative text

SuggestedRemedy

Add (informative) to the title of the section.
 (note the two normative requirements are moved elsewhere)

Proposed Response Response Status **W**

Task Force to discuss.

Are all of these informative? Are they all stated elsewhere?

Cl 33 SC 33.3.2 P 257 L 6 # 177
 Zimmerman, George CME Consulting

Comment Type **TR** Comment Status **D** Editorial

"Type 2, Type 3 and Type 4 PDs shall meet the requirements of 25.4.5 in the presence of (Iunb / 2)." , but the requirement of 25.4.5 specifically only applies to Type 2 devices.
 "A receiver in a Type 2 Endpoint PSE or Type 2 PD (see Clause 33) shall meet the requirements of 25.4.7. A transmitter in a Type 2 Endpoint PSE or Type 2 PD delivering or accepting more than 13.0W average power shall meet either the Open Circuit Inductance (OCL) requirement in 9.1.7 of TP-PMD, or meet the requirements of 25.4.5.1."
 Additionally, the requirement here requires ALL TType 2, 3 and 4 PDs whether or not they include 100BASE-TX, to meet the clause 25 requirement, which would make magnetics more expensive if, in the future, 100BASE-TX support were dropped.
 I believe the purpose of the requirement here is to add Iunb to the clause 25 test, so, which might benefit from some descriptive text as to the purpose.

SuggestedRemedy

Insert after "PDs", "implementing 100BASE-TX (Clause 25) PHYs"
 Add a note after line 6 stating: "NOTE - For PDs implementing both Clause 25 and Clause 33, this adds the unbalance current to the requirements in Clause 25."
 Add Clause 25 to the 802.3bt amendment, and modify 25.4.5 to say "Type 2 or greater Endpoint PSE or Type 2 or greater PD" (2 places).

Proposed Response Response Status **W**

PROPOSED ACCEPT.

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Cl 33 SC 33.3.3.5 P 260 L 14 # 120
 Yseboodt, Lennart Philips
 Comment Type T Comment Status X PD State Diagram
 original text: ""
 "Figure 33-16 PD state diagram" does not yet include Autoclass partial
 finger support.
 SuggestedRemedy
 Insert editors note: "PD state diagram needs to be updated for Autoclass."
 Proposed Response Response Status W
 Do optional behaviors go in the State Diagram?

Cl 33 SC 33.3.4 P 261 L 50 # 121
 Yseboodt, Lennart Philips
 Comment Type T Comment Status X PD Detection
 "A Type 2 PD presents a non-valid detection signature when in a mark event state per
 Figure 33-16."
 Applies to any PD which supports Multiple event classification.
 Shall missing?
 SuggestedRemedy
 "A Type2, Type 3, or Type 4 PD shall present a non-valid detection signature when in a
 mark event state per Figure 33-16."
 Proposed Response Response Status W
 I don't believe there is a PICS associated with this line, but there should be...
 any objection to adding a shall?

Cl 33 SC 33.3.4 P 262 L 6 # 48
 Bennett, Ken Sifos Technologies, In
 Comment Type E Comment Status D LLDP
 "LLDP variable PD 4P-ID" should be "LLDPDU variable.." or "TLV variable..".
 SuggestedRemedy
 Change "LLDP" to "TLV".
 Proposed Response Response Status W
 PROPOSED ACCEPT.

Cl 33 SC 33.3.4 P 262 L 13 # 68
 Yseboodt, Lennart Philips
 Comment Type E Comment Status X PD Detection
 "two voltage/current" can be read as 'or'
 SuggestedRemedy
 change to "two voltage and current"
 Proposed Response Response Status W
 PSEs don't measure both. They force one and measure the other. "and" can be
 misleading...

Cl 33 SC 33.3.4 P 262 L 33 # 69
 Yseboodt, Lennart Philips
 Comment Type E Comment Status D Editorial
 "PD input connector" is not consistent with rest of document
 SuggestedRemedy
 change to "PD PI"
 Proposed Response Response Status W
 PROPOSED ACCEPT.
 Does this change requirements? I don't think so.

Cl 33 SC 33.3.4 P 263 L 1 # 70
 Yseboodt, Lennart Philips
 Comment Type E Comment Status D Editorial
 "PD input connector" is not consistent with rest of document
 SuggestedRemedy
 change to "PD PI"
 Proposed Response Response Status W
 PROPOSED ACCEPT.
 Does this change requirements? I don't think so.

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CI 33 SC 33.3.5 P 264 L 36 # 181
 Zimmerman, George CME Consulting

Comment Type **TR** Comment Status **D** PD Classification

(Note 1 to Table 33-15a)
 "Any PD that is limited to class 0-3 power levels may omit DLL support."
 and P264 L43
 "Type 2, Type 3 and Type 4 PDs shall implement both Multiple-Event class signature (see 33.3.5.2) and Data Link Layer classification (see 33.6)."

Are in conflict. L43 would be read that any Type 3 Class 1-3 PD would have to implement DLL (which is also in conflict with table 33-13a's PD summary, which also says that Type 1-3 Type 3 PDs only have to do 1-Event class).

SuggestedRemedy

Change P264 L43 to read:
 "Type 2, Type 3 and Type 4 PDs at class 4 or greater power levels shall implement both Multiple-Event class signature (see 33.3.5.2) and Data Link Layer classification (see 33.6)."
 Add after the above sentence.
 "PD's of all Types at class 3 or lower power levels are not required to implement Multiple-Event class signature (see 33.3.5.2) and Data Link Layer classification (see 33.6)."

Proposed Response Response Status **W**
 PROPOSED ACCEPT.

CI 33 SC 33.3.5 P 264 L 43 # 231
 Schindler, Fred Seen Simply

Comment Type **TR** Comment Status **D** PD Classification

The footnote on Table 33-15a and text below the table may confuse the reader. If a PD already supports DLL them it should continue to support DLL whether is it consuming less than class-4 power or not.

SuggestedRemedy

Replace footnote 1 with,
 "Any PD not capable of drawing more than class-3 power levels may omit DLL support."

Proposed Response Response Status **W**
 PROPOSED ACCEPT.

CI 33 SC 33.3.5 P 264 L 43 # 243
 Picard, Jean Texas Instruments

Comment Type **TR** Comment Status **D** PD Classification

The statement about Type 3 does not align with table 33-13 for class 1-3

SuggestedRemedy

Restate the sentence to Indicate that for class 1-3 SS, LLDP is optional

Proposed Response Response Status **W**
 PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment 181

CI 33 SC 33.3.5.1 P 264 L 52 # 174
 Zimmerman, George CME Consulting

Comment Type **T** Comment Status **D** PD Classification

"Class 0 is the default for PDs".
 Now that we have Type 3 and Type 4, which are required to present at least 1-event classification class signatures, as described all over the place and summarized in Table 33-13a, Class 0 is NOT the default for PDs. Class 0 is the default that a PSE assumes. this clause specifies the PD. Class 0 appears to be only allowed for Type 1 PDs. This statement needs to be clarified.
 Additionally, Table 33-16a appears to allow class 0 for Type 3 PDs. Without a class sig, how is the PD a type 3?

SuggestedRemedy

Clarify the sentence as either applying only to Type 1 PDs or as applying to Type 1 and Type 3/SS PDs, and editor to search and align other references to class 0 Type 3 PDs in document (some of which I have commented on elsewhere).

Proposed Response Response Status **W**
 PROPOSED ACCEPT IN PRINCIPLE.

Change to: Class 0 is the default for Type 1 PDs."

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Cl 33 SC 33.3.5.1 P 265 L 4 # 223
Schindler, Fred Seen Simply

Comment Type ER Comment Status D PD Classification

The text,
"PDs implementing a Multiple-Event class signature shall return Class 4 in accordance with the maximum power draw, PClass_PD, as specified in Table 33-18."
may confuse the reader.

SuggestedRemedy

Replace the sentence with,
PDs implementing a Multiple-Event class signature shall return Class 4 in accordance with the maximum power draw, PClass_PD, as specified in Table 33-18 and the responses specified in Table 33-16a."

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 33 SC 33.3.5.1 P 265 L 7 # 104
Yseboodt, Lennart Philips

Comment Type ER Comment Status D PD Classification

"Since 1-Event classification is a subset of Multiple-Event classification, Type 2, and Type 3 PDs operating with a maximum power draw corresponding to class 4 or higher, as well as Type 4 PDs respond to 1-Event classification with a Class 4 signature."

Why list Type 4 separately ? Can be shorter.

SuggestedRemedy

"Since 1-Event classification is a subset of Multiple-Event classification, Type 2, Type 3, and Type 4 PDs operating with a maximum power draw corresponding to class 4 or higher respond to 1-Event classification with a Class 4 signature."

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 33 SC 33.3.5.2 P 266 L 3 # 196
Johnson, Peter Sifos Technologies

Comment Type T Comment Status D PD Classification

The terms "class_sig_A" and "class_sig_B" are just a problem waiting to happen in Table 33-16a and in the PD State Diagram (and associated variable definitions). Will get confused with classifying on Alt-A and Alt-B pairs when these really mean something else.

SuggestedRemedy

What about "search and replace" with "class_sig_A" with "class_sig_ev12" and "class_sig_B" with "class_sig_ev35" or something like this?

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

That is a fair point, but the suggestion may be even worse. Any other ideas?

Cl 33 SC 33.3.5.2 P 266 L 23 # 182
Zimmerman, George CME Consulting

Comment Type TR Comment Status D PD Classification

Table 33-16a shows no entries for dual signature class 0 PDs and text on line 38 indicates "Dual-signature PDs shall use only class 0 to 5 power level..."

Which is it? Table 33-13a suggests DS PDs don't have class 0

SuggestedRemedy

change "class 0 to 5" to "class 1 to 5"

Proposed Response Response Status W

PROPOSED ACCEPT.

OBE by 147.

Cl 33 SC 33.3.5.2 P 266 L 26 # 197
Johnson, Peter Sifos Technologies

Comment Type T Comment Status D PD Classification

In Table 33-16a, since class signatures are per-pairset in a Dual Signature PD, perhaps it would be beneficial to highlight this fact.

SuggestedRemedy

Beneath Dual-Signature under PD Type 3 and PD Type 4, add (per pairset)

Proposed Response Response Status W

PROPOSED REJECT.

This idea is captured in the text below the table.

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CI 33 SC 33.3.5.2 P 266 L 38 # 145
 Yseboodt, Lennart Philips
 Comment Type **TR** Comment Status **D** PD Classification
 Topic: Class 0 / Type 3 removal
 "Dual-signature PDs shall use only class 0 to 5 power level over each pairset."
 SuggestedRemedy
 "Dual-signature PDs shall use only class 1 to 5 power levels over each pairset."
 Proposed Response Response Status **W**
 PROPOSED ACCEPT IN PRINCIPLE.
 OBE by 147.

CI 33 SC 33.3.5.2 P 266 L 38 # 147
 Yseboodt, Lennart Philips
 Comment Type **TR** Comment Status **D** PD Classification
 "Dual-signature PDs shall use only class 0 to 5 power level over each pairset. The class advertised over each pairset is the power requested by the PD over that pairset. Dual-signature PDs may use different classsignature per pairset. It is not recommended to use different class signatures with single load dual-signature PDs."
 Remove Class 0 + Grammer improvement needed.
 SuggestedRemedy
 "Dual-signature PDs shall advertise a class signature of 1, 2, 3, 4 or 5 on each pairset. The class advertised on each pairset is the power requested by the PD on that pairset. Dual-signature PDs may advertise a different class signature on each pairset. It is not recommended to use different class signatures if the dual-signature PD powers a single electrical load."
 Proposed Response Response Status **W**
 PROPOSED ACCEPT.

CI 33 SC 33.3.5.2 P 266 L 39 # 105
 Yseboodt, Lennart Philips
 Comment Type **ER** Comment Status **D** PD Classification
 "Dual-signature PDs may use different class signature per pairset."
 Better wording.
 SuggestedRemedy
 "Dual-signature PDs may use a different class signature on each pairset."
 Proposed Response Response Status **W**
 PROPOSED ACCEPT IN PRINCIPLE.
 OBE by 147.

CI 33 SC 33.3.5.2.1 P 267 L 15 # 239
 Picard, Jean Texas Instruments
 Comment Type **TR** Comment Status **D** PD Classification
 The PD needs more margin for TLCF_PD to keep complexity down.
 SuggestedRemedy
 Increase the maximum value from 84.5 ms to 87.5 ms.
 Proposed Response Response Status **W**
 PROPOSED ACCEPT.

CI 33 SC 33.3.5.2.1 P 267 L 15 # 52
 Beia, Christian STMicroelectronics
 Comment Type **TR** Comment Status **D** PD Classification
 Table 33-17
 The PD long first class event spec introduces a big burden for PD timing accuracy, which can be relaxed if the PSE was able to better control the lenght of the long first class event. This should not add complexity to the PSE since its clock is typically more accurate than the PD one.
 SuggestedRemedy
 Change Table 33-17 item7, TLCF_PD max to 86.5
 Leave 75.5 as min
 Proposed Response Response Status **W**
 PROPOSED ACCEPT IN PRINCIPLE.
 OBE by 239

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CI 33 SC 33.3.5.3 P 267 L 37 # 244
 Picard, Jean Texas Instruments

Comment Type TR Comment Status D PD Classification

To indicate Autoclass, same requirement as indicated in table 33-16 needs to apply.

SuggestedRemedy

Replace with "a PD implementing Autoclass shall reduce its classification current at TACS (as defined in Table 33-17a), resulting in a classification signature of '0' (as shown in table 33-16 for type 3) for the remainder of CLASS_EV1."

Proposed Response Response Status W

PROPOSED ACCEPT.

This means PDs need to draw at least 1mA during the TACS period so that the PI discharges.

CI 33 SC 33.3.5.3 P 267 L 40 # 123
 Yseboodt, Lennart Philips

Comment Type T Comment Status D PD Classification

"The PD shall not draw more power than the power consumed during the time from T AUTO_PD1 to T AUTO_PD2 (as defined in Table 33-17a) at any point until V Port_PD falls below V Reset_th."

This precludes re-negotiating through DLL.

SuggestedRemedy

"The PD shall not draw more power than the power consumed during the time from T AUTO_PD1 to T AUTO_PD2 (as defined in Table 33-17a) at any point until V Port_PD falls below V Reset_th, unless the PD successfully negotiates a higher power level through Data Link Layer classification as defined in section 33.6."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by 148 (the exact same comment.)

CI 33 SC 33.3.5.3 P 267 L 40 # 148
 Yseboodt, Lennart Philips

Comment Type TR Comment Status D PD Classification

"The PD shall not draw more power than the power consumed during the time from T AUTO_PD1 to T AUTO_PD2 (as defined in Table 33-17a) at any point until V Port_PD falls below V Reset_th."

This precludes re-negotiating through DLL.

SuggestedRemedy

"The PD shall not draw more power than the power consumed during the time from T AUTO_PD1 to T AUTO_PD2 (as defined in Table 33-17a) at any point until V Port_PD falls below V Reset_th, unless the PD successfully negotiates a higher power level through Data Link Layer classification as defined in section 33.6."

Proposed Response Response Status W

PROPOSED ACCEPT.

CI 33 SC 33.3.5.3 P 268 L 5 # 238
 Picard, Jean Texas Instruments

Comment Type TR Comment Status D PD Classification

The PD needs more margin for TACS to keep complexity down.

SuggestedRemedy

Increase the maximum value from 84.5 ms to 87.5 ms.

Proposed Response Response Status W

PROPOSED ACCEPT.

See comment 239.

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Cl 33 SC 33.3.6 P 268 L 5 # 54
 Beia, Christian STMicroelectronics

Comment Type TR Comment Status D PD Classification

Table 33-17a
 The autotimer timing, as well as T_LCF_PD, introduces a big burden for PD timing accuracy, which can be relaxed if the PSE was able to better control the length of the first long finger.

SuggestedRemedy

Change Table 33-17 item7, TACS max to 86.5
 Leave 75.5 as min

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by 239.

Cl 33 SC 33.3.7 P 269 L 35 # 51
 Bennett, Ken Sifos Technologies, Inc

Comment Type TR Comment Status X PD Power

In item 4 of table 33-18 the PClass_PD parameter description has changed from "input average power" to "input available average power". The values for it are in the MAX column. It seems like the values for it should be in the MIN column, because it is a minimum "available" power under worst case conditions.

The pre-existing text in the item 4 info reference, 33.3.7.2, defines PClass_PD as the "maximum input power", which does not match either the pre-existing nor the modified PClass_PD parameter description in table 33-18.

There is an underlying problem, which is that PClass_PD, which is a power classification level, is shown as a Parameter in table 33-18, with a range within each class.

It would be much clearer to present this using the same method that's used in the PSE section for PClass, which specifies values for each class in a separate table (33-7), and uses "PClass" in the MIN/MAX columns of table 33-11.

The suggested remedy would not change the content or intent of the pre-existing information text in 33.3.7.2.

SuggestedRemedy

- 1) Incorporate PClass_PD levels into table 33-16a.
- 2) Change item 4 to a single row with the following items: Parameter="Input Average Power"; Symbol="Pport_PD"; and MAX="PClass_PD".
- 3) Adjust references as necessary

(See bennett_PClass_PD.pdf)

Proposed Response Response Status W

Task Force to discuss

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Cl 33 SC 33.3.7 P 269 L 35 # 50
 Bennett, Ken Sifos Technologies, In

Comment Type T Comment Status X PD Classification

PClass is defined as a total port power and is described in Equation 33-3 using the PD Classification PClass_PD and the channel loss.

The descriptions for dual-signature PD's use PClass_PD per pairset, and different classes are allowed per pairset.

The suggestion is one possible approach to remedy this problem.

SuggestedRemedy

Create new dual signature parameters PClassDS_alta and PClassDS_altb, where PClass_PD = PClassDS_alta + PClassDS_altb. Add text in 33.3.7.2 stating that single-signature rules shall apply to each pairset in dual signature PDs.

Proposed Response Response Status W

Task Force to discuss.

Cl 33 SC 33.3.7 P 270 L 13 # 246
 Picard, Jean Texas Instruments

Comment Type TR Comment Status D PD Power

Ppeak_PD is not mentioned for class 6-8

SuggestedRemedy

Clarify how the peak power requirement should be applied for class 6 and 8 and define it accordingly for class 5 and 7, as well as for class 6 and 8.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment 12

Cl 33 SC 33.3.7.3 P 271 L 41 # 149
 Yseboodt, Lennart Philips

Comment Type TR Comment Status D PD Power

"After T Inrush-2P min, the PD shall meet P Class_PD as specified in Table 33-18." Disallows extended power.

SuggestedRemedy

"After T Inrush-2P min, Class 6 or Class 8 PDs shall meet Pclass at the PSE PI, all other PDs shall meet P Class_PD as specified in Table 33-18."

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 33 SC 33.3.7.3 P 271 L 41 # 29
 Darshan, Yair Microsemi

Comment Type TR Comment Status D PD Inrush

The objective of this comment is to restore some of the text used in IEEE802.3-2012 clause 33.3.7.3 in IEEE802.3bt clause 33.3.7.3 (same location) lines 39-41.

The reason for text changes in 802.3bt was the concern that PD vendors will consume power above type 1 power while PD is still in POWER-UP mode which will cause unsuccessful startup.

It will be shown that the new version in 802.3bt:

- 1.Includes incorrect description of linrush process ending point while in 2012 version the text describing the ending point is correct.
- 2.The concern was already resolved in existing text in two locations

The text in the PD spec in 802.3bt clause 33.3.7.3 page 271 lines 39-50 separated to 4 parts e.g. [Part A]:

33.3.7.3 Input inrush current

[Part A] Inrush current per pairset is drawn beginning with the application of input voltage at the pairset compliant with Vport_PD-2P requirements as defined in Table 33-18,

[Part B] and ending before TInrush-2P min per Table 33-11.

[Part C] After TInrush-2P min, the PD shall meet PClass_PD as specified in Table 33-18.

Part D] Type 2, Type 3 and Type 4 PDs with pse_power_leveltype state variable set to 2, 3 and 4 respectively prior to power-on shall behave like a Type 1 PD for at least Tdelay-2P min. Tdelay-2P for each pairset starts when VPD-2P crosses the PD power supply turn on voltage, VOn_PD. This delay is required so that the Type 2, Type3 and Type 4 PD does not enter a high power state before the PSE has had time to switch current limits on each pairset from lInrush-2P to lLIM-2P.

[Part A] is correct description of the starting point of linrush process in the PD.

[Part B] is incorrect description of the ending point of linrush process in the PD. The end point of inrush process depends only on PD physics and not anything else e.g. PSE linrush timer.

It is true that Inrush need to be ended before TInrush-2P min per Table 33-11 but it needs to be in separate sentence and not as part of the description of the end point of the Inrush process.

The end point of the inrush process can be only when Cport is get to steady state by having Cport to be charged to 99% of its final value.

The end point and the requirements for the linrush duration are described accurately in IEEE802.3-2012 version:

"and ending when CPort is charged to 99 % of its final value. This period should be less than TInrush min per Table 33-11."

[Part C] This part resolves the concern by requiring PD to meet PClass_PD as specified in Table 33-18 only after TInrush-2P min.

[Part D] This part also resolves the concern for Type 2 and above by waiting Tdelay before PD can consume more than Type 1 power.

Summary: The only problem with the current text of 802.3bt is the mixing between the

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Inrush end point process description and the requirement that the process will be ended within Tinrush minimum.

See detailed analysis in darshan_01_0915.pdf, titled: "Only PD affects PD POWERUP Tinrush max (Not the PSE Tinrush Timer).

SuggestedRemedy

1) Change lines 26-27 from:
 33.3.7.3 Input inrush current
 Inrush current per pairset is drawn beginning with the application of input voltage at the pairset compliant with Vport_PD-2P requirements as defined in Table 33-18, and ending before Tinrush-2P min per Table 33-11.
 After Tinrush-2P min, the PD shall meet PClass_PD as specified in Table 33-18.

To:
 Inrush current is drawn during the startup period beginning with the application of input voltage at the PI compliant with VPort_PD-2P requirements as defined in Table 33-18, and ending when CPort has reached a steady state and is charged to 99 % of its final value. This period shall be less than Tinrush min per Table 33-11.
 After Tinrush-2P min, the PD shall meet PClass_PD as specified in Table 33-18.

(2) To consider to add the following note after line 50 that address the concerns in details and supply design guide lines.
 Note: For successful startup, a PSE supplying linrush-2P minimum value and a PD not drawing more than Type 1 maximum DC current results in stable voltage ramping across the PD input capacitor which is important for successful POWER UP. In addition, Cport value and PD load current may be time dependent. As a result PD implementers need to ensure that for any combinations of Cport and Type 1 maximum DC current during POWERUP, the PD inrush period does not exceed 50msec and that higher PD load power is used only after Tdelay.

Proposed Response *Response Status* **W**
 PROPOSED ACCEPT IN PRINCIPLE.

Accept changes in suggested remedy for (1).

Cl 33 **SC 33.3.7.4** **P 273** **L 23** # **245**
 Picard, Jean Texas Instruments

Comment Type **TR** *Comment Status* **X** *PD Power*
 The peak power definition for class 6 and 8 is not consistent with statement of page 272 line 20 (referring to PSE Pclass).

SuggestedRemedy

Clarify how the peak power definition should be applied for class 6 and 8.

Proposed Response *Response Status* **W**
 I don't understand the suggested remedy.

Cl 33 **SC 33.3.7.5** **P 273** **L 33** # **183**
 Zimmerman, George CME Consulting

Comment Type **TR** *Comment Status* **X** *PD Power*

"When the input voltage at the PI is static and in the range of VPort_PD defined by Table 33-18, the transient current drawn by the PD shall not exceed 4.70 mA/Is in either polarity. A dual-signature PD shall not exceed 4.70 mA/us in either polarity per pairset in the same conditions."

First, now that we have 4 pairs, this leaves the reader to have to assume whether for single signature PDs the 4.70 mA/us applies to the sum of the 2 pairsets or per pairset. In the below, I assume it is to the sum of the 2 pairsets.
 Second, it is worded awkwardly.

SuggestedRemedy

Change "When the input voltage at the PI is static and in the range of VPort_PD defined by Table 33-18, the transient current drawn by the PD shall not exceed 4.70 mA/us in either polarity. A dual-signature PD shall not exceed 4.70 mA/us in either polarity per pairset in the same conditions."
 to "When the input voltage at the PI is static and in the range of VPort_PD defined by Table 33-18, the transient current drawn by the PD shall not exceed 4.70 mA/us in either polarity. For a single-signature PD, this requirement applies to the sum of the current on both pairsets, for a dual-signature PD this requirement applies to the current on a per-pairset basis."

Proposed Response *Response Status* **W**
 Task Force to discuss

Cl 33 **SC 33.3.7.6** **P 275** **L 5** # **232**
 Schindler, Fred Seen Simply

Comment Type **TR** *Comment Status* **X** *Pres: Fred1*

New PD Types need to have their current demands constrained.

SuggestedRemedy

A presentation will be provided that cover why this section exists and why new PD Types should have the same constrains placed on them. Baseline text may also be proposed.

This section is based on work done in IEEE 802.3at see

http://www.ieee802.org/3/at/public/2007/05/avetteth_0507.pdf

http://www.ieee802.org/3/at/public/2007/03/schindler_1_0307.pdf

Proposed Response *Response Status* **W**
 Wait for presentation

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

CI 33 SC 33.3.7.6 P 275 L 16 # 203
 Dwelley, David Linear Technology

Comment Type E Comment Status D Cport

New text needs improving:
 "Type 1, Type 2, and single-signature Type 3 PDs with classes 0 to 4 shall meet the requirement for Cport as defined in Table 33–18 item 9. Type 3 dual-signature PDs with class 0 to 4 shall meet the requirement for Cport as defined in Table 33–18 item 9 for each pairset. For class 5 and 6 single-signature PDs, if CPort_min = 10µF, transient behavior has no further requirements. For dual-signature class 5 PDs, this recommendation applies to each pairset. For class 7 and 8 single signature PDs, if CPort_min = 20µF, transient behavior has no further requirements. See 33.2.7.2 (TBD) or the transient conditions"

SuggestedRemedy

Change to:
 "A PD shall continue to operate normally in the presence of transients at the PSE PI as defined in 33.2.7.2. A single-signature PD shall include Cport >= Cport_min as defined in Table 33–18 item 9. A dual-signature PD shall meet this requirement for each pairset. For Class 0-4 PDs, no further considerations are required to maintain operation during PSE transients.

PDs with power draw greater than Class 4 may require extra capacitance to maintain operation during PSE transients. Class 5 and 6 single-signature PDs can typically meet the requirement with CPort_min = 10µF. Class 5 dual-signature PDs should include these Cport values at each pairset. Class 7 and 8 single signature PDs can typically meet this requirement with CPort_min = 20µF."

Proposed Response Response Status W

PROPOSED ACCEPT.

CI 33 SC 33.3.7.6 P 275 L 16 # 179
 Zimmerman, George CME Consulting

Comment Type TR Comment Status X Cport

"Type 1, Type 2, and single-signature Type 3 PDs with classes 0 to 4 shall meet the requirement for Cport as defined in Table 33–18 item 9. Type 3 dual-signature PDs with class 0 to 4 shall meet the requirement for Cport as defined in Table 33–18 item 9 for each pairset."

These belong as notes to Table 33-18 item 9, and not in the section called "PD behavior during transients" (yes, they relate to transients, but are not a specification of behavior"

SuggestedRemedy

Delete first 2 sentences of first paragraph of 33.3.7.6, and add them as either as Note 1 to item 9 of Table 33-18, OR, split Item 9 of Table 33-18 into 3 rows, one for Type 1, 2 and Type 3/SS PDs Class 0-4, and one for Type 3/DS PDs. (if Type 4 is to be added, it should be added in Table 33-18 and not 33.3.7.6 as well)

Proposed Response Response Status W

Task Force to discuss.

Could OBE 203.

CI 33 SC 33.3.7.6 P 275 L 18 # 180
 Zimmerman, George CME Consulting

Comment Type TR Comment Status X Cport

Statements excluding PDs with CPort_min values greater than certain values are confusing, and do not appear to apply to any existing requirements, since the only requirements currently in the section are for TYpe 1 and Type 2.

"For class 5 and 6 single-signature PDs, if CPort_min >10uF, transient behavior has no further requirements. For dual-signature class 5 PDs, this recommendation applies to each pairset. For class 7 and 8 single signature PDs, if CPort_min >20uF, transient behavior has no further requirements. See 33.2.7.2 (TBD) or the transient conditions"

SuggestedRemedy

move statements to an editor's note, and explicitly state the requirements that these PDs are being excluded from, including what needs to be done to make those requirements (is it the referenced 'drop out' specification?)

Proposed Response Response Status W

Task Force to discuss

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 33 SC 33.3.7.6 P 275 L 29 # 39
 Darshan, Yair Microsemi

Comment Type **TR** Comment Status **X** PD Power

There is some confusion in this text (lines 28-29):
 - A Type 1 PD input current shall not exceed the PD upperbound template (see Figure 33-18) after TLIM min (see Table 33-11 for a Type 1 PSE)

 The text refer to Figure 33-18 which specifies Tcut_min but talks about the current not to be exceed after Tlim_min so is it Tcut_min or Tlim_min?
 I believe that it should be Tcut_min both in the text and in Figure 33-18 due to the fact that It is related to Figure 33-18 that talks about not crossing Ppeak_PD which is the overload condition for 50msec.

SuggestedRemedy

I suggest changing from Tlim_min to Tcut_min in line 29 to sync with Figure 33-18.
 To be discussed by the group.

Proposed Response Response Status **W**

Task Force to discuss

Cl 33 SC 33.3.7.6 P 275 L 34 # 124
 Yseboodt, Lennart Philips

Comment Type **T** Comment Status **D** PD Power

"A Type 2 PD shall meet both of the following:
 a) The PD input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template (see Figure 33-18) within 4 ms. During this test, the PD PI voltage is driven from 50 V to 52.5 V at greater than 3.5 V/ms, a source impedance of 1.5 , and a source that supports a current greater than 2.5 A.\

b) The PD shall not exceed the PD upperbound template beyond T LIM min under worst-case current draw under the following conditions. The input voltage source drives V PD from V Port_PSE min to 56 V at 2250 V/s, the source impedance is R Ch (see Table 33-1), and the voltage source limits the current to MDI I LIM per Equation (33-14)."

Does not support new Types.

SuggestedRemedy

"A Type 2, Type 3 or Type 4 PD shall meet both of the following:
 a) The PD input current spike shall not exceed 2.5 A ****per pairset**** and shall settle below the PD upperbound template (see Figure 33-18) within 4 ms. During this test, the PD PI voltage is driven from 50 V to 52.5 V at greater than 3.5 V/ms, a source impedance of 1.5 ohm ****divided by the number of pairsets****, and a source that supports a current greater than 2.5 A ****per pairset****.

b) The PD shall not exceed the PD upperbound template beyond T LIM min under worst-case current draw under the following conditions. The input voltage source drives V PD from V Port_PSE min to 56 V at 2250 V/s, the source impedance is R Ch **** per pairset**** (see Table 33-1), and the voltage source limits the current to MDI I LIM per Equation (33-14)."

Proposed Response Response Status **W**

PROPOSED ACCEPT.

Cl 33 SC 33.3.7.6 P 275 L 49 # 125
 Yseboodt, Lennart Philips

Comment Type **T** Comment Status **D**

Equation 33-14 has the constant 5.00 in without mentioning the dimension.
 Is that 5mA or 5 A ?

SuggestedRemedy

Add correct dimension to this equation.

Proposed Response Response Status **W**

PROPOSED ACCEPT IN PRINCIPLE.

I believe that is mA

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Cl 33 SC 33.3.7.6 P 275 L 54 # 171
 Zimmerman, George CME Consulting

Comment Type ER Comment Status X PD Power

"is the per pairset current limit at the MDI (MDI I_LIM)"
 the preceding text says this is MDI I_LIM-2P.

SuggestedRemedy

Either: remove the -2P notation for MDI I_LIM-2P (preferred)
 or change line 54 to read MDI I_LIM-2P

Proposed Response Response Status W

Task Force to discuss.

Why are we repeating the parameter name in its definition?

Cl 33 SC 33.3.7.6 P 275 L 1622 # 7
 Darshan, Yair Microsemi

Comment Type E Comment Status X Cport

This text applies to different scenarios and for easy reading each scenario may need to
 start in new row.

SuggestedRemedy

Change the editing from:
 Type 1, Type 2, and single-signature Type 3 PDs with classes 0 to 4 shall meet the
 requirement for Cport as defined in Table 33.18 item 9. Type 3 dual-signature PDs with
 class 0 to 4 shall meet the requirement for Cport as defined in Table 33.18 item 9 for each
 pairset. For class 5 and 6 single-signature PDs, if CPort_min >=10uf, transient behavior
 has no further requirements. For dual-signature class 5 PDs, this recommendation applies
 to each pairset. For class 7 and 8 single signature PDs, if CPort_min >=20uf, transient
 behavior has no further requirements. See 33.2.7.2 (TBD) or the transient conditions

To:
 Type 1, Type 2, and single-signature Type 3 PDs with classes 0 to 4 shall meet the
 requirement for Cport as defined in Table 33.18 item 9.
 Type 3 dual-signature PDs with class 0 to 4 shall meet the requirement for Cport as
 defined in Table 33.18 item 9 for each pairset.
 For class 5 and 6 single-signature PDs, if CPort_min >=10uf, transient behavior has no
 further requirements.
 For class 5 and 6 dual-signature PDs, if CPort_min >=10uf for each pairset, transient
 behavior has no further requirements.
 For class 7 and 8 single signature PDs, if CPort_min >=20uf, transient behavior has no
 further requirements.
 See 33.2.7.2 (TBD) or the transient conditions

Proposed Response Response Status W

Task Force to discuss.

Cl 33 SC 33.3.7.10 P 276 L 37 # 248
 Picard, Jean Texas Instruments

Comment Type TR Comment Status X PD Power

ICON_2P max for class 5 and 6 may be too tight to pass the test described (using only
 2.5m cable) due to diode mismatch (including temperature differences). To avoid later
 interoperability problems in the field related to diode selection.

SuggestedRemedy

If test conditions remain the same, need to verify and confirm if ICON-2P for class 6 allows
 sufficient margin. If not the case, increase its value accordingly.

Proposed Response Response Status W

What is the suggested remedy? Add editor's note?

Cl 33 SC 33.3.7.10 P 276 L 38 # 34
 Darshan, Yair Microsemi

Comment Type TR Comment Status D PD Power

Referring to the text:
 All Class 5 and higher PDs shall not exceed Icon-2P-unb (Table 33-11, item 4a) on either
 pairset when tested according to section 33.3.7.10.1.

-
- 1. PDs need to meet Icon-2P_unb for all classes above class 5 including for extended
 power mode.
- 2. In addition Ipeak-2P need to be met for extended power mode as well.
 Meeting (1) ensures meeting (2) as regard to E2EP2PRunb effect.

SuggestedRemedy

1. Change from:
 All Class 5 and higher PDs shall not exceed Icon-2P-unb (Table 33-11, item 4a) on either
 pairset when tested according to section 33.3.7.10.1.

To:
 All Class 5 and higher PDs operating in non extended power mode or extended power
 mode, shall not exceed Icon-2P-unb (Table 33-11, item 4a) on either pairset when tested
 according to section 33.3.7.10.1.

2. After this text, to Add Editor Note:
 Editor Note: To update Rmin/Rmax and test setups for PD PI for meeting Icon-2P_unb
 and Ipeak-2P when PD is using extended power mode

Proposed Response Response Status W

PROPOSED REJECT.

Extended power is not mentioned anywhere in the standard. Also, the change does not
 add anything as all Class 5 and higher PDs includes those using extended power.

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Cl 33 SC 33.3.8 P 279 L 23 # 126
 Yseboodt, Lennart Philips

Comment Type T Comment Status D PD MPS

In Table 33-19a under 'Conditions' the contracts
 - "If no long first class event"
 - "If long first class event (T_LCF)" a
 are used.

This can be replaced by using the PD variable 'short_mps' returned by the do_class_timing function.

SuggestedRemedy

Replace "If no long first class event" by "short_mps = FALSE"
 Replace "If long first class event (T_LCF)" by "short_mps = TRUE"

Proposed Response Response Status W

PROPOSED ACCEPT.

Is this reflected in state diagram.

Cl 33 SC 33.4. P 281 L 37 # 162
 Zimmerman, George CME Consulting

Comment Type TR Comment Status D AES

Equation 33-16 ..."for a 100 Mb/s or greater PHY".
 While this is the spec for MDI impedance balance for 100BASE-T and 1000BASE-T, it is not consistent with the spec for 10GBASE-T in Clause 55.8.2.2.
 (it is unclear yet what the 2.5G/5G PHYs will be here)

SuggestedRemedy

Insert after line 43, (eqn 55-55 in 802.3bx d3p2)
 "Bal(f) >= 48 dB (1<=f<30 MHz)
 >= 44 - 19.2 log10(f/50) (30<= f < 500 MHz)
 for a 10GBASE-T PHY."

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 33 SC 33.5.1.1 P 292 L 52 # 265
 Dove, Daniel Dove Networking Solut

Comment Type TR Comment Status X Management

We need bits in the PSE Control Register that control the state of each pairset independently from the overall PSE configuration. For instance, one pairset could be disabled while the other enabled or in forced-power mode.

SuggestedRemedy

Insert row for bit 11.9 PS Disable A
 Insert row for bit 11.8 PS Disable B

These bits identify whether the PSE Enable bits apply to the pairset A or B. If 0, the PSE Enable bits apply and default behavior is to follow the order of bits 1:0. If 1, the PSE Enable bits do not apply and the pairset is disabled. Note: I chose this polarity to keep consistent with existing implementations where those bits would naturally be zero yet pairset operation functions based upon the bits in values 1:0. Additional note: For Type 3 and Type 4 PSEs, one would expect the bits 1:0 to control both pairsets the same way when attached to a Type 3/4 SS PD This can be done by setting bits3:2 to '11' An alternative approach to this would be to define separate registers for PS_AltA and PS_AltB or identify them as local registers per pairset.

Proposed Response Response Status W

Task Force to discuss

Cl 33 SC 33.5.1.1 P 293 L 8 # 233
 Schindler, Fred Seen Simply

Comment Type TR Comment Status X Management

Changes in Table 33-21 are not correct and text is missing below the table.

SuggestedRemedy

On line 8 change table column one, "11.15.8" to "11.15.7".

On line 12 last table column add, "R/W".

After line 43 insert text,
 33.5.1.1.x Force Power Test Mode Pairset Selection (11.7:6)
 Bits 11.7:6 determine which PSE Alternative or Alternatives are enabled when Force Power Test Mode is enabled.

Proposed Response Response Status W

I don't understand the suggested remedy. Task Force to discuss.

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Cl 33 SC 33.6.3.2 P 299 L 16 # 215

Schindler, Fred

Seen Simply

Comment Type TR Comment Status X Management

It does not appear to be worthwhile providing class 6 and 7 if they are within 3% of eachother.

SuggestedRemedy

Have the Task Force discuss whether Class 7 PD power should be increased. Provide an Editor's note for the decision if the value changes so that participants provide corrections for the text for the next Draft.

Proposed Response Response Status W

class 6 is only that high because of extended power.

Task force to discuss

Cl 33 SC 33A.5 P 330 L 12 # 28

Darshan, Yair

Microsemi

Comment Type T Comment Status X Pres: YairB

1. The constants in Annex 33A.5 needs to be replaced with numbers.
2. In addition some of existing constants need to be slightly modified due to the changes made to D1.1.

SuggestedRemedy

Propose to implement darshan_08_0915.pdf

Proposed Response Response Status W

Wait for presentation

Cl 33 SC 33A.6 P 330 L 21 # 31

Darshan, Yair

Microsemi

Comment Type TR Comment Status D Annex

Marked for reference as YD_002_PSEP2P)

In D1.1 we have approved darshan_06_0715.pdf in http://www.ieee802.org/3/bt/public/jul15/darshan_06_0715-REV008.docx. It was requested specifically to use Annex B (and not Annex C and not Annex A) to the PSE PI material in 33.2.7.4.1 and 33.2.7.4.2 that links to a Normative Annex Named Annex B in the above link. Currently the editor named the original Annex B as Annex 33A.6 to Annex 33A.10 which is informative Annex and the intent was that this part will be separate NORMATIVE Annex B. In addition It is not clear that all parts of original Annex B that are now Annex 33A.6 to Annex 33A.10 are related to each other as in original Annex B and not independent parts We need to implement the relevant comment from D1.1 and others as approved.

Summary:

PSE PI Material from the above link is Normative Annex B.
The Autoclass material is Annex C.

The following remedy is identical to adopt Annex B in the above approved document while correcting the relevant instances were Annex A, B and C are mentioned.

SuggestedRemedy

Make the following changes without editorial licensing to do otherwise:

1. In Annex 33A.6 page 330 line 21: Change title to: Annex 33B [Normative]PSE PI pair-to-pair resistance/current unbalance.
 - 1.1 In page 330 line 27: Change table Yuval_1 to Table 33B-1.
 - 1.2 In page 330 line 28: Change <> to Annex F.
 - 1.3 In page 330 line 51: Change Figure number from 33A-4 to 33B-1.
 - 1.4 In page 331 line 17: Change Table 33A-1 to Table 33B-1
2. In Annex 33A.7 page 331 line 35: Change title to: 33B.1 direct measurements of Rpse_max and Rpse_min
 - 2.1 in page 331 line 43: Change from 33A.8 and 33A.9 to 33B.2 and 33B.3
 - 2.1 In page 332 line 17: Change Figure number from 33A-5 to 33B-2.
3. in Annex 33A.8 page 332 line 21: Change title to: 33B.2 Effective Resistance Measurement Method by measurement of current unbalance under worst case pair-to-pair load conditions
 - 3.1 in page 332 line 41: Change Figure number from 33A-6 to 33B-3.
 - 3.2 in page 333 line 17: Change from 33A.9 to 33B.3
4. in Annex 33A.9 page 333 line 20: Change title to: 33B.3 Current Unbalance Measurement Method
 - 4.1 in page 333 line 22: change Table 33A-1 TO 33B-1
 - 4.2 in page 333 line 24: change Figure 33A-7 to 33B-4.

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4.3 in page 333 line 41: change Figure 33A-7 to 33B-4.
 5. in Annex 33A.10 page 334 line 9: Change title to: 33B.4 Channel resistance with less than 0.1 ohm
 6: Add Annex F (informative) - Derivation of Rload_max and Rload_min.
 Editor Note (to be removed prior to publication): To consider the value of adding informative Annex F to present Rload_max and Rload_min equation derivation and values.
 7: in Annex 33B page 335 line 2: Change to Annex C.

Proposed Response *Response Status* **W**
 PROPOSED ACCEPT IN PRINCIPLE.
 Make changes in suggested remedy with editorial lisencc to combine with other accepted comments (fixing table and figure numbers, etc.).

Cl **33** *SC* **33A.6** *P* **330** *L* **28** # **85**
 Yseboodt, Lennart Philips
Comment Type **E** *Comment Status* **D** *Editorial*
 reference is missing instead <>
SuggestedRemedy
 Yair, where does this refer to ?
Proposed Response *Response Status* **W**
 Good question.

Cl **33** *SC* **33A.6** *P* **331** *L* **4** # **87**
 Yseboodt, Lennart Philips
Comment Type **E** *Comment Status* **D** *Annex*
 There is suspicion that the addition needs to get priority. Otherwise the units are likely to add up as "ohms + dimensionless" rather than Ohms.
 Note sure due to missing description of Kpse.
SuggestedRemedy
 Replace formula by
 $R_{pair_max} \leq R_{pair_min} * (U + K_{pse})$
 Yair, correct ?
Proposed Response *Response Status* **W**
 PROPOSED ACCEPT.

Cl **33** *SC* **33A.6** *P* **331** *L* **12** # **88**
 Yseboodt, Lennart Philips
Comment Type **E** *Comment Status* **D** *Editorial*
 Kpse is not specified
SuggestedRemedy
 Yair, please specify Kpse
Proposed Response *Response Status* **W**
 PROPOSED ACCEPT.

Cl **33** *SC* **33A.6** *P* **331** *L* **21** # **15**
 Darshan, Yair Microsemi
Comment Type **T** *Comment Status* **X** *Pres: Yair4*
 Table 33A.1 in draft D1.2 (will be Table 33B-1 in D1.3 due to wrong implementation of darshan_06_0715.pdf in http://www.ieee802.org/3/bt/public/jul15/darshan_06_0715-REV008.docx.)
 1. To update values per changes made in D1.1.
 2. To replace TBDs with numbers
 3. To add two additional columns to support extended power mode.
SuggestedRemedy
 1. Update TBDs in page 331 lines 20-26 Table 33B-1 (was Table 33A-1 in D1.2).
 PSE Class=5,Rload_min=0.739,Rload_max=0.1562
 PSE Class=6,Rload_min=0.635.
 PSE Class=7,Rload_min=0.577,Rload_max=1.094
 PSE Class=8,Rload_min=0.533,Rload_max=0.979
 2. Modify the table to include two additional columns for Extebded Power mode.
 See updated details in page 3 of darshan_04_0915.pdf
Proposed Response *Response Status* **W**
 Wait for presentation

IEEE P802.3bt D1.2 4P PoE 5th Task Force review comments

Cl 79 SC 79.3.2.4 P 341 L 2 # 234
Schindler, Fred Seen Simply

Comment Type TR Comment Status D DLL

The new sentence,
"A Type 3 or Type 4 device shall set the bits in power type to TBD."

Could be implementation specific but a preferred solution is provided below, which permits legacy Types to respond to new Types with the highest power levels possible.

SuggestedRemedy

Replace the referenced sentence with,
"A Type 3 or Type 4 device shall set the bits in power type to the highest Type the TLV generating device supports."

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 79 SC 79.3.2.4.1 P 341 L 33 # 151
Yseboodt, Lennart Philips

Comment Type TR Comment Status D DLL

"This field shall be set according to Table 79-4."
Unfortunately the 'power type' field only supports Type 1/2 PDs and PSEs.
How should a Type 3/4 device set this field ?

SuggestedRemedy

Replace by
"This field shall be set according to Table 79-4.
Type 3 or Type 4 PSEs shall set this field to the value corresponding with Type 2 PSEs.
Type 3 or Type 4 PDs shall set this field to the value corresponding with Type 2 PDs."

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 79 SC 79.3.2.6a P 342 L 52 # 235
Schindler, Fred Seen Simply

Comment Type TR Comment Status D DLL

Replace the Editor's note on line 52 with the requested text.

SuggestedRemedy

Replace the Editor's note on line 52 with,
"The PSE power status value field shall contain the PSE's bit-map of the PSE power pair,
and PSE power class, defined in Table 79-6a and is reported for the device generating the TLV."

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 79 SC 79.3.2.61.1 P 343 L 32 # 216
Schindler, Fred Seen Simply

Comment Type TR Comment Status D DLL

Clarify what a PD places in a PSE field.

SuggestedRemedy

Add after line 32,
"A TLV generated by a PD shall set the field to 00."

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 79 SC 79.3.2.6a.2 P 343 L 36 # 217
Schindler, Fred Seen Simply

Comment Type TR Comment Status D DLL

Clarify what a PD places in a PSE field.

SuggestedRemedy

Add after line 36,
"A TLV generated by a PD shall set the field to 0000."

Proposed Response Response Status W

PROPOSED ACCEPT.

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Cl 79 SC 79.3.2.6b P 343 L 40 # 236

Schindler, Fred Seen Simply

Comment Type TR Comment Status D DLL

Replace the Editor's note on line 40 with the requested text.

Suggested Remedy

Replace the Editor's note on line 40 with,
"The System setup value field shall contain the device bit-map of the Power type, PD 4P-ID, and PD PI defined in Table 79-6b and is reported for the device generating the TLV."

Proposed Response Response Status W

PROPOSED ACCEPT.